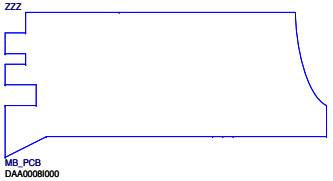
**MODEL NAME :** *ZAZ00*
**PCB NO :** *LA-B441P*
**BOM P/N :** *TBD*




# Dell/Compal Confidential

## Schematic Document

## Dino (Broadwell ULT)

**2014-10-16**

**Rev: 1.0**

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2013/07/04 | Deciphered Date | 2013/10/28 |

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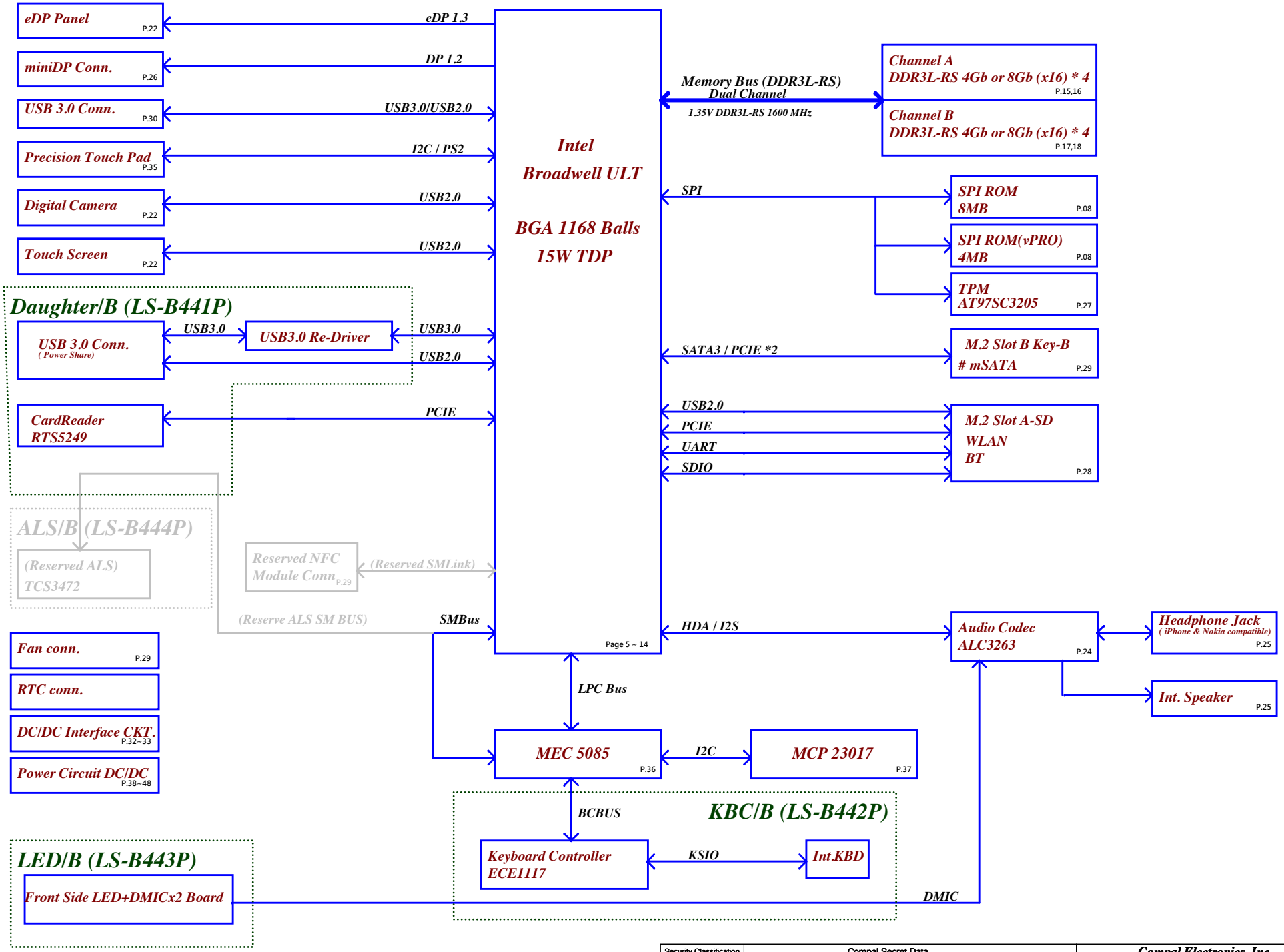
Title: *P01-Cover Page*

| Size | Document Number | Rev |
|---|---|---|
| | *LA-B441P* | 1.0 |

Date: Thursday, October 16, 2014 Sheet 1 of 50




| | | | |
|---|---|---|---|
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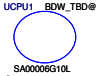
Title: P02-Block Diagram

| Size | Document Number | Rev |
|---|---|---|
| | LA-B441P | 1.0 |

Date: Saturday, October 04, 2014 Sheet 2 of 50

## CPU Option

UCPU1 BDW_TBD@



SA00006G10L
CL8064701325204 QDJ9

## DRAM Option

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Micron 4G | UD28 Micron_4G@ SA00005TH0L MT41K256M16HA-125M:E | UD29 Micron_4G@ SA00005TH0L MT41K256M16HA-125M:E | UD31 Micron_4G@ SA00005TH0L MT41K256M16HA-125M:E | UD32 Micron_4G@ SA00005TH0L MT41K256M16HA-125M:E | UD1 Micron_4G@ SA00005TH0L MT41K256M16HA-125M:E | UD7 Micron_4G@ SA00005TH0L MT41K256M16HA-125M:E | UD3 Micron_4G@ SA00005TH0L MT41K256M16HA-125M:E | UD4 Micron_4G@ SA00005TH0L MT41K256M16HA-125M:E |
| Micron 8G | UD28 Micron_8G@ SA00006FB0L MT41K512M16TNA-125M:E | UD29 Micron_8G@ SA00006FB0L MT41K512M16TNA-125M:E | UD31 Micron_8G@ SA00006FB0L MT41K512M16TNA-125M:E | UD32 Micron_8G@ SA00006FB0L MT41K512M16TNA-125M:E | UD1 Micron_8G@ SA00006FB0L MT41K512M16TNA-125M:E | UD7 Micron_8G@ SA00006FB0L MT41K512M16TNA-125M:E | UD3 Micron_8G@ SA00006FB0L MT41K512M16TNA-125M:E | UD4 Micron_8G@ SA00006FB0L MT41K512M16TNA-125M:E |
| Hynix 4G | UD28 Hynix_4G@ SA00006JF0L H5TC4G63AFR-PBR | UD29 Hynix_4G@ SA00006JF0L H5TC4G63AFR-PBR | UD31 Hynix_4G@ SA00006JF0L H5TC4G63AFR-PBR | UD32 Hynix_4G@ SA00006JF0L H5TC4G63AFR-PBR | UD1 Hynix_4G@ SA00006JF0L H5TC4G63AFR-PBR | UD7 Hynix_4G@ SA00006JF0L H5TC4G63AFR-PBR | UD3 Hynix_4G@ SA00006JF0L H5TC4G63AFR-PBR | UD4 Hynix_4G@ SA00006JF0L H5TC4G63AFR-PBR |
| Hynix 8G | UD28 Hynix_8G@ SA00006Q90L H5TC8G63AMR-PBR | UD29 Hynix_8G@ SA00006Q90L H5TC8G63AMR-PBR | UD31 Hynix_8G@ SA00006Q90L H5TC8G63AMR-PBR | UD32 Hynix_8G@ SA00006Q90L H5TC8G63AMR-PBR | UD1 Hynix_8G@ SA00006Q90L H5TC8G63AMR-PBR | UD7 Hynix_8G@ SA00006Q90L H5TC8G63AMR-PBR | UD3 Hynix_8G@ SA00006Q90L H5TC8G63AMR-PBR | UD4 Hynix_8G@ SA00006Q90L H5TC8G63AMR-PBR |
| Elpida 4G | UD28 Elpida_4G@ SA00005HT0L K4B4G1646B-HKK0 | UD29 Elpida_4G@ SA00005HT0L K4B4G1646B-HKK0 | UD31 Elpida_4G@ SA00005HT0L K4B4G1646B-HKK0 | UD32 Elpida_4G@ SA00005HT0L K4B4G1646B-HKK0 | UD1 Elpida_4G@ SA00005HT0L K4B4G1646B-HKK0 | UD7 Elpida_4G@ SA00005HT0L K4B4G1646B-HKK0 | UD3 Elpida_4G@ SA00005HT0L K4B4G1646B-HKK0 | UD4 Elpida_4G@ SA00005HT0L K4B4G1646B-HKK0 |
| Elpida 8G | UD28 Elpida_8G@ SA00006Q90L K4B8G1646B-MKK0 | UD29 Elpida_8G@ SA00006Q90L K4B8G1646B-MKK0 | UD31 Elpida_8G@ SA00006Q90L K4B8G1646B-MKK0 | UD32 Elpida_8G@ SA00006Q90L K4B8G1646B-MKK0 | UD1 Elpida_8G@ SA00006Q90L K4B8G1646B-MKK0 | UD7 Elpida_8G@ SA00006Q90L K4B8G1646B-MKK0 | UD3 Elpida_8G@ SA00006Q90L K4B8G1646B-MKK0 | UD4 Elpida_8G@ SA00006Q90L K4B8G1646B-MKK0 |

## DRAM Config Option

| MEM_CONFIG2 | MEM_CONFIG1 | MEM_CONFIG0 |
|---|---|---|
| RH314 Micron_4G@ SD028100280 10K_0402_5%~D | RH315 Micron_4G@ SD028100280 10K_0402_5%~D | RH316 Micron_4G@ SD028100280 10K_0402_5%~D |
| RH314 Micron_8G@ SD028100280 10K_0402_5%~D | RH315 Micron_8G@ SD028100280 10K_0402_5%~D | RH303 Micron_8G@ SD028100280 10K_0402_5%~D |
| RH314 Hynix_4G@ SD028100280 10K_0402_5%~D | RH180 Hynix_4G@ SD028100280 10K_0402_5%~D | RH316 Hynix_4G@ SD028100280 10K_0402_5%~D |
| RH314 Hynix_8G@ SD028100280 10K_0402_5%~D | RH180 Hynix_8G@ SD028100280 10K_0402_5%~D | RH303 Hynix_8G@ SD028100280 10K_0402_5%~D |
| RH271 Elpida_4G@ SD028100280 10K_0402_5%~D | RH315 Elpida_4G@ SD028100280 10K_0402_5%~D | RH316 Elpida_4G@ SD028100280 10K_0402_5%~D |
| RH271 Elpida_8G@ SD028100280 10K_0402_5%~D | RH315 Elpida_8G@ SD028100280 10K_0402_5%~D | RH303 Elpida_8G@ SD028100280 10K_0402_5%~D |

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| Issued Date | 2013/07/04 | Deciphered Date | 2013/10/28 |
| Title | P03-BoM Option | | |
| Size | Document Number | | Rev 1.0 |
| Date: Saturday, October 04, 2014 | Sheet 3 of 50 | | |

## Board ID Table for AD channel

| RE79 | CE54 | REV |
|---|---|---|
| 130K | 4700p | X01 |
| 62K | 4700p | X02 |
| 33K | 4700p | X03 |
| 8.2K | 4700p | X04 |
| 4.3K | 4700p | A00 |
| 2K | 4700p | |
| 1K | 4700p | |
| | | |

BOARD_ID rise time is measured from 5%~68%.

| PCH USB Port Mapping | USB PORT# | DESTINATION |
|---|---|---|
| | 0 | External USB3(On IOB) |
| | 1 | External USB3(On MB) |
| | 2 | NGFF CARD WLAN |
| | 3 | Touch Panel |
| | 4 | Camera |
| | 5 | |
| | 6 | |
| | 7 | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |

| PCH DDI Port Mapping | DDI PORT# | DESTINATION |
|---|---|---|
| | 1 | mini-DP |
| | 2 | |
| | | |

SMBUS Control Table

Reserve ALS SMBUS

| | SOURCE | BATTERY | ALS | Charger | NFC | XDP | Touch Pad |
|---|---|---|---|---|---|---|---|
| I2C1C_CLK<br>I2C1C_DATA | MEC5085 | V | | | | | |
| I2C1D_CLK<br>I2C1D_DATA | MEC5085 | | | | | | |
| I2C1G_CLK<br>I2C1G_DATA | MEC5085 | | V | V | | | |
| PCH_SML0CLK<br>PCH_SML0DATA | PCH | | | | V | | |
| PCH_SML1CLK<br>PCH_SML1DATA | PCH | | | | | | |
| SMBCLK<br>SMBDATA | PCH | | | | | V | |
| I2C1_CLK<br>I2C1_DATA | PCH | | | | | | V |

Link

| CLK | DIFFERENTIAL CLK# | DESTINATION | PCI EXPRESS PORT# | DESTINATION |
|---|---|---|---|---|
| | CLKOUT_PCIE0 | Card Reader | Lane 1 | Card Reader |
| | CLKOUT_PCIE1 | | Lane 2 | |
| | CLKOUT_PCIE2 | | Lane 3 | |
| | CLKOUT_PCIE3 | NGFF CARD WLAN | Lane 4 | NGFF CARD WLAN |
| | CLKOUT_PCIE4 | | Lane 5 | |
| | CLKOUT_PCIE5 | mSATA/ PCIe | Lane 6 | mSATA/ PCIe(Port0+Port1) |
| | FLEX CLK# | DESTINATION | | |
| | CLKOUT_LPC_0 | EC LPC | | |
| | CLKOUT_LPC_1 | TPM | | |

| SATA PORT# | DESTINATION |
|---|---|
| SATA0 | |
| SATA1 | |
| SATA2 | |
| SATA3 | m-SATA |
| | |
| | |

Symbol Note :

: means Digital Ground

: means Analog Ground


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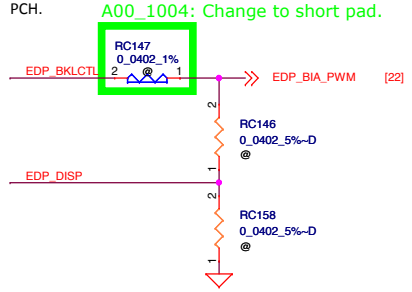
Title: P04-Notes List

Size | Document Number: LA-B441P | Rev: 1.0

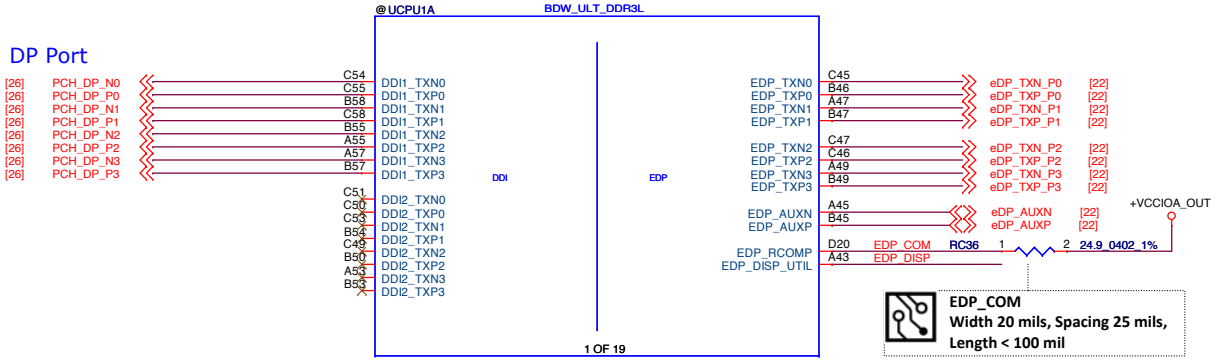
Date: Saturday, October 04, 2014 | Sheet 4 of 50

Low voltage multipurpose DISP_UTIL pin on the processor for backlight modulation control of embedded panels and S3D device control for active shutter glasses. This pin will co-exist with functionality similar to existing BKLTCTL pin on the PCH.

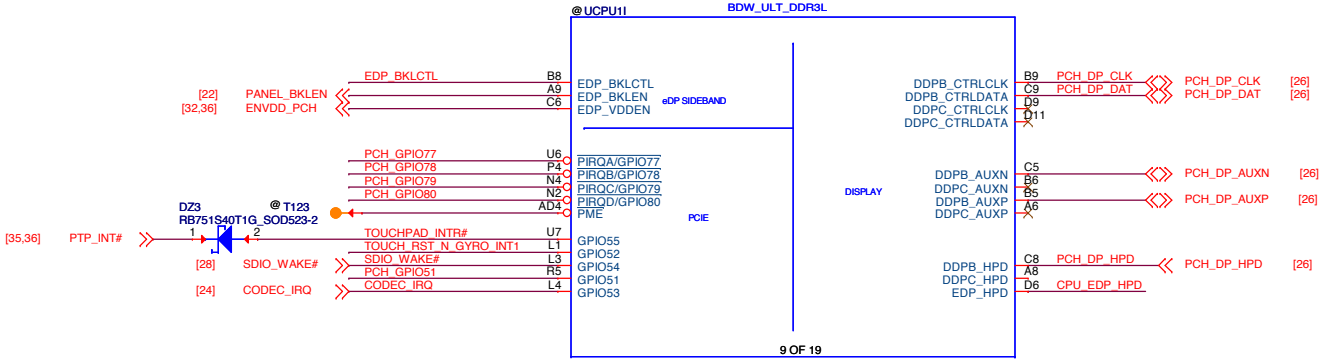
A00_1004: Change to short pad.

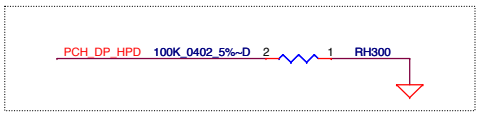



## DP Port

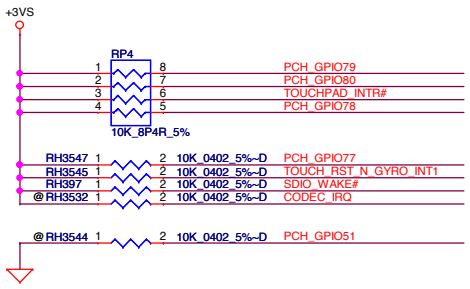


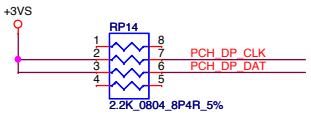

**EDP_COM**
**Width 20 mils, Spacing 25 mils, Length < 100 mil**



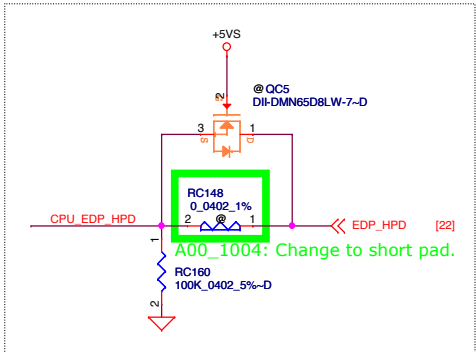

## GPIO Signals




| Functional Strap Definitions | |
|---|---|
| DDI Port 1 Disabling | |
| DDPB_CTRLDATA | Enable : Pull up to 3.3V with 2.2K+-5% ohm<br>Disable : No connect |

| Functional Strap Definitions | |
|---|---|
| DDI Port 2 Disabling | |
| DDPC_CTRLDATA | Enable : Pull up to 3.3V with 2.2K+-5% ohm<br>Disable : No connect |

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Title: P05-MCP(1/10) DDI,EDP

Size | Document Number: LA-B441P | Rev: 1.0

Date: Sunday, October 05, 2014 | Sheet 5 of 50

**H_PECI**
1. Total Length : 15 inchs
2. Resistor Value (±5%) : 43 ohm
3. Breakin/Breakout Length Max :0.4 ~ 1 inchs

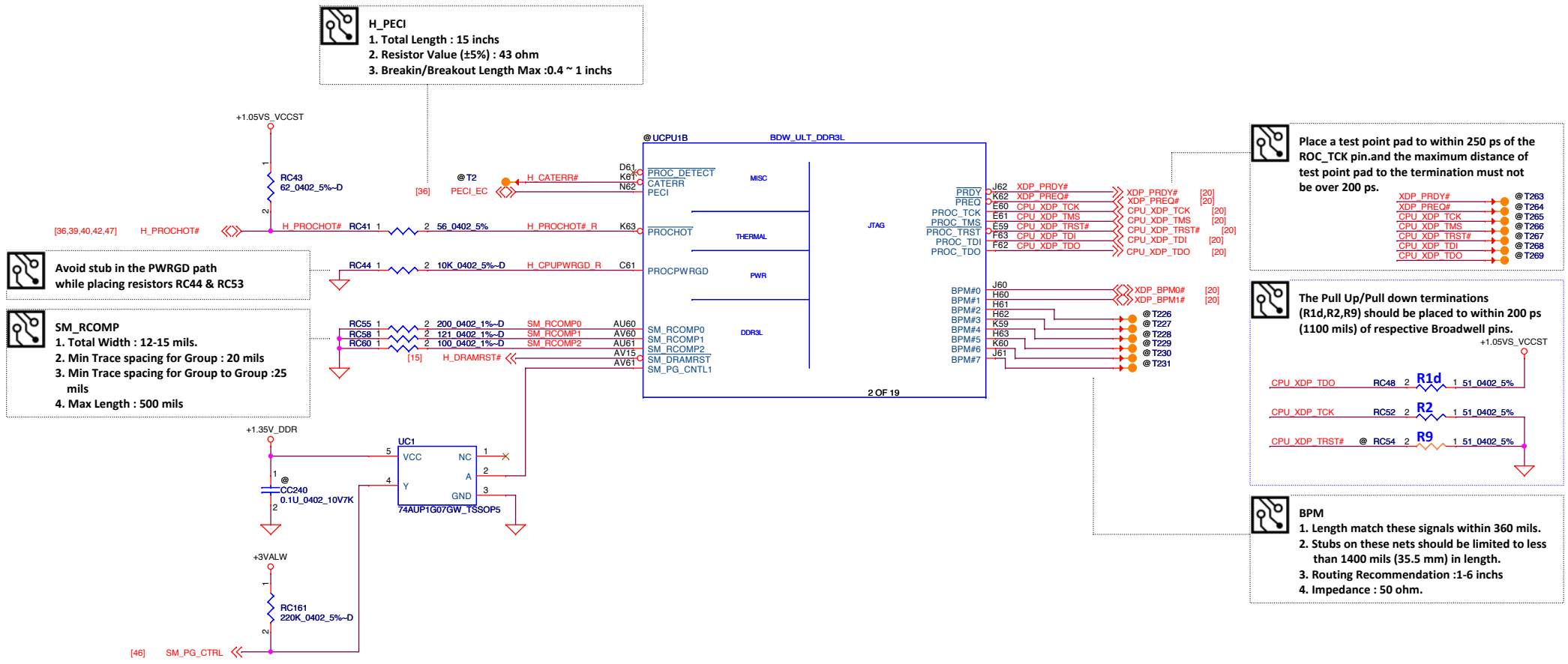
**Avoid stub in the PWRGD path while placing resistors RC44 & RC53**

**SM_RCOMP**
1. Total Width : 12-15 mils.
2. Min Trace spacing for Group : 20 mils
3. Min Trace spacing for Group to Group :25 mils
4. Max Length : 500 mils

**Place a test point pad to within 250 ps of the ROC_TCK pin.and the maximum distance of test point pad to the termination must not be over 200 ps.**

**The Pull Up/Pull down terminations (R1d,R2,R9) should be placed to within 200 ps (1100 mils) of respective Broadwell pins.**

**BPM**
1. Length match these signals within 360 mils.
2. Stubs on these nets should be limited to less than 1400 mils (35.5 mm) in length.
3. Routing Recommendation :1-6 inchs
4. Impedance : 50 ohm.




| | | | |
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| Security Classification | Compal Secret Data | | |
| Issued Date | 2013/07/04 | Deciphered Date | 2013/10/28 |

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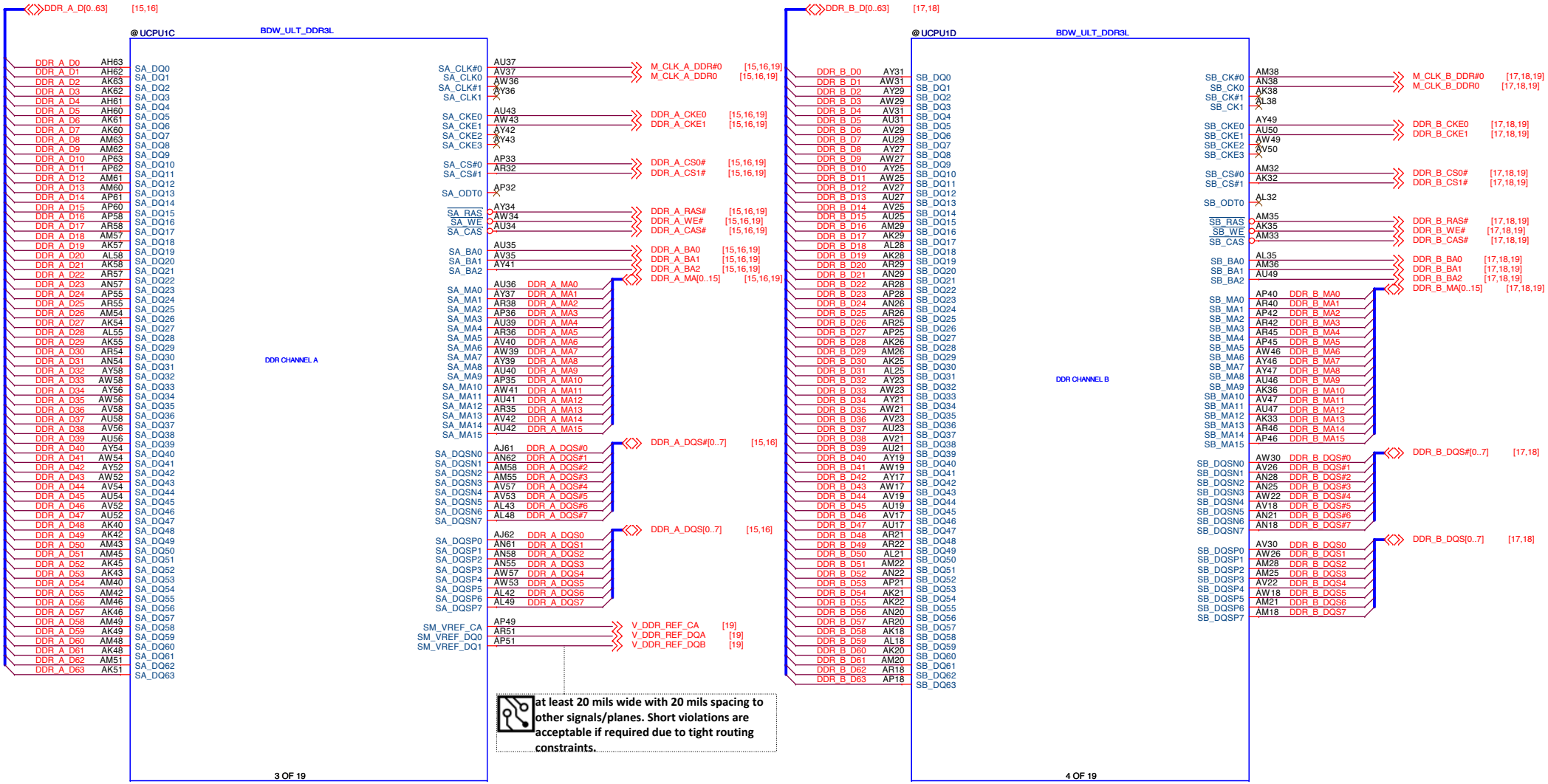
**Compal Electronics, Inc.**

Title: P06-MCP(2/10) PM,XDP

Size | Document Number: LA-B441P | Rev: 1.0

Date: Saturday, October 04, 2014 | Sheet 6 of 50




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | Compal Electronics, Inc. |
| Issued Date | 2013/07/04 | Deciphered Date 2013/10/28 | Title: P07-MCP(3/10) DDRIII |
| | | | Size: Document Number: LA-B441P Rev: 1.0 |
| | | | Date: Saturday, October 04, 2014 Sheet 7 of 50 |

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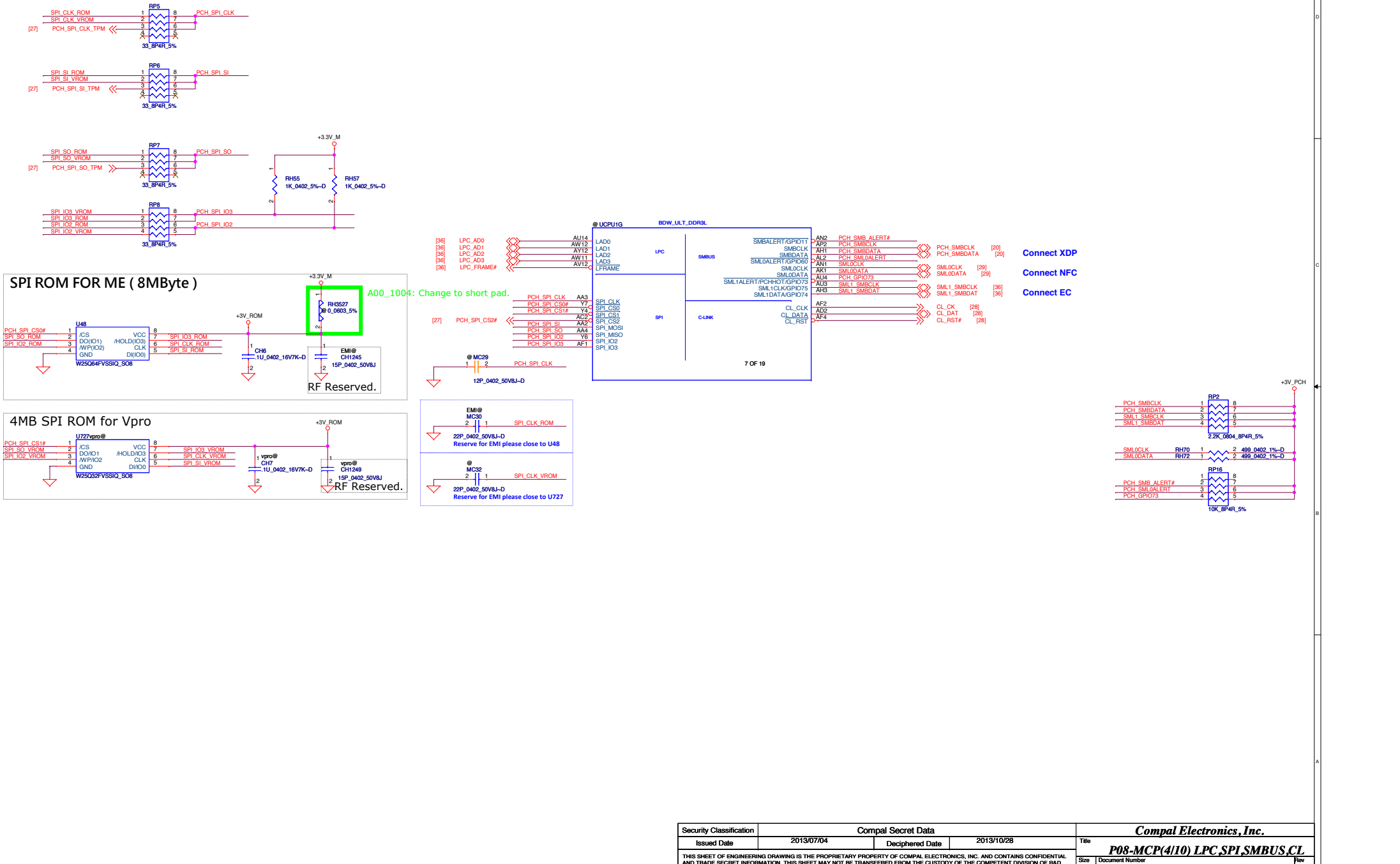


| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2013/07/04 | Deciphered Date | 2013/10/28 |

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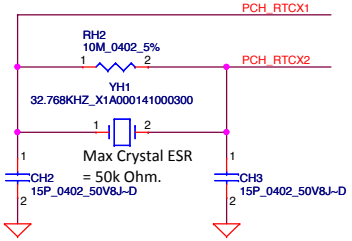
Compal Electronics, Inc.

Title: P08-MCP(4/10) LPC,SPI,SMBUS,CL

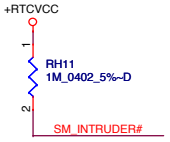
| Size | Document Number | Rev |
|---|---|---|
| | LA-B441P | 1.0 |

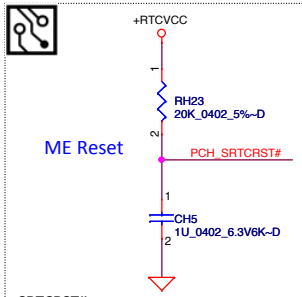
Date: Sunday, October 05, 2014 Sheet 8 of 50

**RTCX1 RTCX2**
1. Total Length : 1000 mils
2. Space > 15 mils
3. Resistor Value (±5%) : 10M

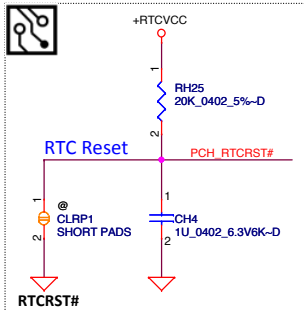



**INTRUDER#**
1. Critical Low Speed Signal
2. Space > 15 mils
3. Frequency to Avoid 32K
4. All critical signals must stay away from potential glitch or noise sources on the platform.



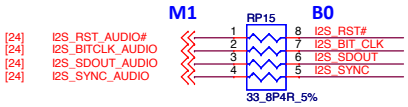

**SRTCRST#**
1. Total Length : 8000 mils
2. Space > 15 mils
3. Impedance Target 50 Ω ±15% for Microstrip.
4. RC time delay between 18 ms - 25 ms must be met.
5. There must not be a jumper for SRTCRST# pin.



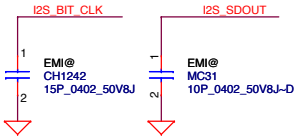

**RTCRST#**
1. Total Length : 8000 mils
2. Space > 15 mils
3. Impedance Target 50 Ω ±15% for Microstrip.
4. RC time delay between 18 ms - 25 ms must be met.

1.When SATA and PCIe are muxed, always route according to SATA design guidelines.
2. Breakout < 600 mils
3. Zdiff : 85 ohm
4. Isolation to Other Signal Groups: Breakout : 8 mils/ Main routing : 20 mils in MS, 15 mils in SL,DSL
5. Max Length : 2 via Max 8", 3 vias Max 7"
6. Within Layer Max Mismatch : 15 mils.
7. Total Length Max Mismatch : 10 mils.
8. AC capacitors to be placed as close as possible to the connector. Maximum distance from AC capacitors to connector is 500 mils.
9. Minimum breakout pair-to-pair spacing of 3.5 mils is allowed for a maximum length of 20 mils within the 600 mils breakout.
10. Design constraint: breakout routing should be non-interleaved to mitigate concerns on near-end crosstalk.

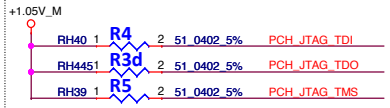
**HDA_SDIN/HDA_SDO/HDA_SYNC/HDA_BCLK/HDA_RST#**
1. BO < 500 mils
2. 1000 mils < M1 < 14000 mils.
3. Trace Length Matching (HDA_SDIO,HDA_BCLK,HDA_SDOUT)
4. Resistor Value : 33 ohm

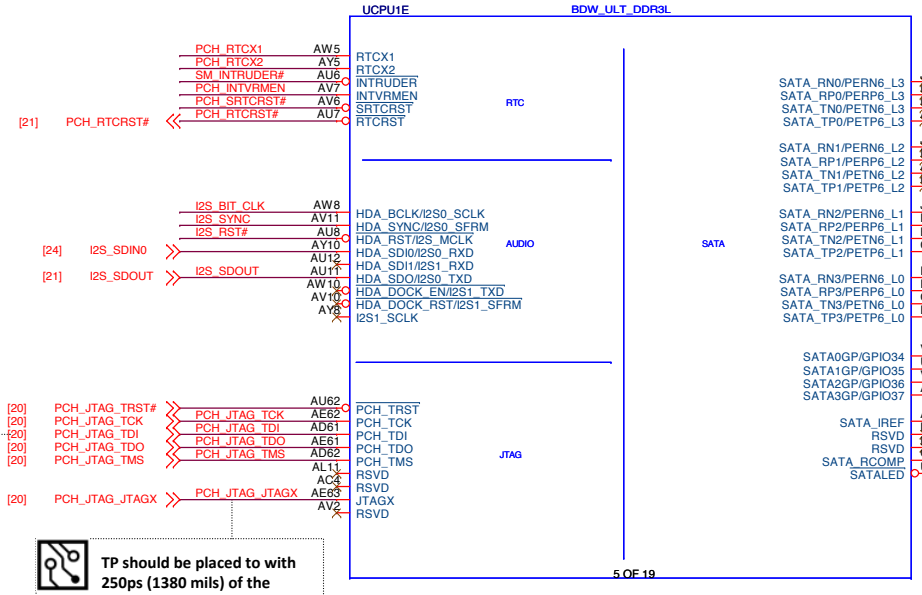


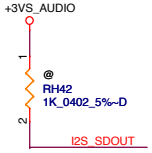

RF Reserved.




**PCH JTAG**
The Pull Up/Pull down terminations (R4,R3d,R5) should be placed to within 200ps of the respective Broadwell pin.

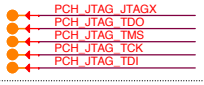


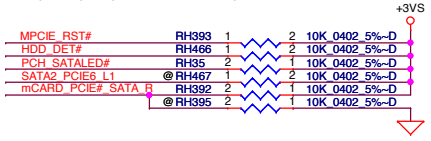




| Functional Strap Definitions | |
|---|---|
| Flash Descriptor Security Override | |
| HDA_SDO/ I2S0_TXD | 0 = Enable security measures defined in the Flash Descriptor.<br>1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. |

TP should be placed to with 250ps (1380 mils) of the respetive Haswell ULT pins, and the distance between TP and termination (if any) must be within 200ps (1100 mils).



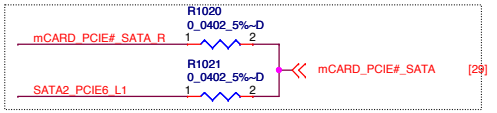

**GPIO Signals**
SATA0GP,SATA1GP,SATA2GP,SATA3GP
1. Needs a weak pull-up:10 KΩ ±10% pull-up to V3.3.
2. Unused SATA[3:0]GP pins must be terminated to either 3.3V rail or GND using 8.2–10 KΩ on the motherboard. Either pull-up or pull-down is acceptable.

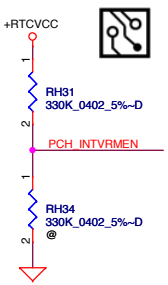



**SATA_RCOMP, SATA_IREF**
1. Break-out : 4 mils
2. 12-15 mil trace with <0.2 Ω.
3. Length total <= 500 mils.
4. Requires 12 mils isolation from all High Speed I/O and clocks.

SATA_RCOMP
1. Tied up to a clean 1.05V source (VCCASATA3PLL) with no capacitor on the net.
2. 3 KΩ ±1% precision pull-up resistor

SATA_IREF
1. Pull-up direct to 1.05V (VCCASATA3PLL).




**INTRUDER#**
1. Critical Low Speed Signal
2. Space > 15 mils
3. Frequency to Avoid 32K
4. All critical signals must stay away from potential glitch or noise sources on the platform.

| Functional Strap Definitions | |
|---|---|
| Integrated VRM | |
| INTVRMEN | 0 = DCPSUS1, DCPSUS2, DCPSUS3 and DCPSUS4 are powered from an external power source (should be connected to an external VRM).<br>1 = Integrated VRMs enabled. DCPSUS1, DCPSUS2 and DCPSUS3 can be left as No Connect. |

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | Compal Electronics, Inc. |
| Issued Date | 2013/07/04 | Deciphered Date | 2013/10/28 |
| Title | P09-MCP(4/10) RTC,AUDIO,SATA | | |
| Size | Document Number LA-B444P | | Rev 1.0 |
| Date: Saturday, October 04, 2014 | | Sheet 9 of 50 | |

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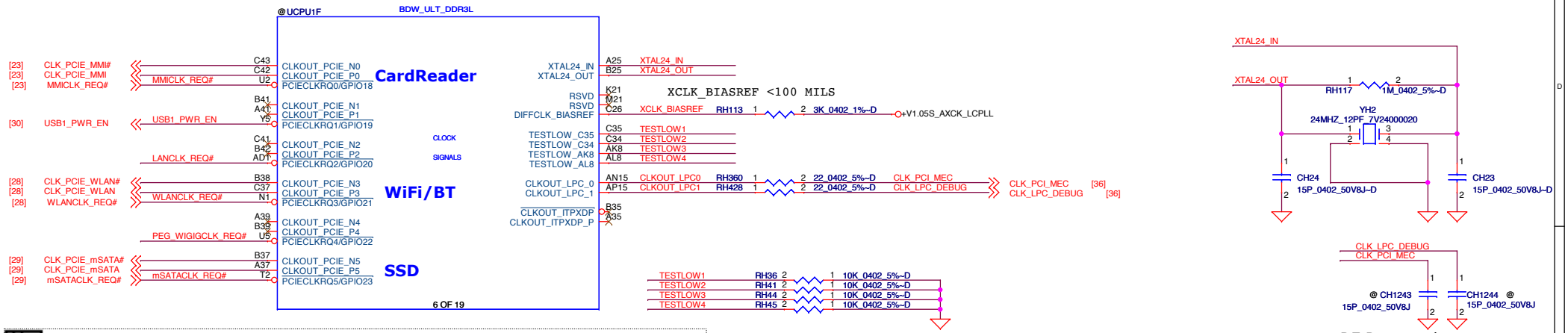
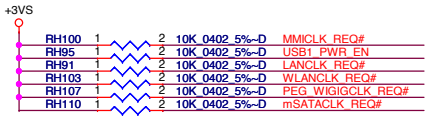






1. Breakout Routing Length Max : 500 mils.
2. Breakin Routing Length Max : 1500 mils
3. Routing Min and Max Length : 2"~9"
4. Differential Pair Length Matching. <25 mils for PCIe, <20 mils for ITP
6. Max Vias : 4
5. Stitching vias should be placed with this spacing:
   a).30-mils pitch between differential clock via and closest stitching GND-via.
   b). Every differential clock via must have at least one GND stitching via with a maximum spacing of 30 mils (0.762 mm).
6. Placement of additional stitching vias, where possible, is recommended.




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | Compal Electronics, Inc. |
| Issued Date | 2013/07/04 | Deciphered Date | 2013/10/28 |

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| | | | |
|---|---|---|---|
| Title | P10-MCP(5/10) CLOCKS | | |
| Size | Document Number LA-B444P | | Rev 1.0 |
| Date: Saturday, October 04, 2014 | Sheet 10 of 50 | | |

Deep S3 (Pop RH430)

Deep S3 support, connect to EC

NON-Deep S3 Support

A00_1004: Change to short pad.

Deep S3 support, connect to DSW power rail

PCH Strap PIN

DSWODVREN - On Die DSW VR Enable
* H : Enable
L : Disable

closed MCP 2000 mils

TLS Confidentiality

Low - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality
*High - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality

Deep S3 Support

GPIO86 have internal pull down

Boot BIOS Strap

| PCH_GPIO86 | Boot BIOS Location |
|---|---|
| * 0 | SPI |

GPIO66 have internal pull down

| A16 SWAP OVERRIDE STRAP | |
|---|---|
| STP_A16OVR | *LOW = A16 SWAP OVERRIDE<br>HIGH = NO OVERRIDE |

I2C is daisy chain routing with pull up on the last device

Width = 15 mil, Spacing = 12 mil
Close PCH within 500 mil

Reserve for RF please close to UH1

DDR Memory Configuratino Type Strap pin

| GPIO Pin | Pin Name | Micron 4G SA00005TH0L | TBD | Hynix 4G SA00006JF0L | Hynix 8G SA00006Q90L | TBD | Elpida 8G SA00006090L |
|---|---|---|---|---|---|---|---|
| PCH_GPIO70 | MEM_CONFIG0 | 0 | 1 | 0 | 1 | 0 | 1 |
| PCH_GPIO93 | MEM_CONFIG1 | 0 | 0 | 1 | 1 | 0 | 0 |
| PCH_GPIO94 | MEM_CONFIG2 | 0 | 0 | 0 | 0 | 1 | 1 |

RF Reserved.

*LOW=Default
HIGH=No Reboot

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2013/07/04 | Deciphered Date | 2013/10/28 |

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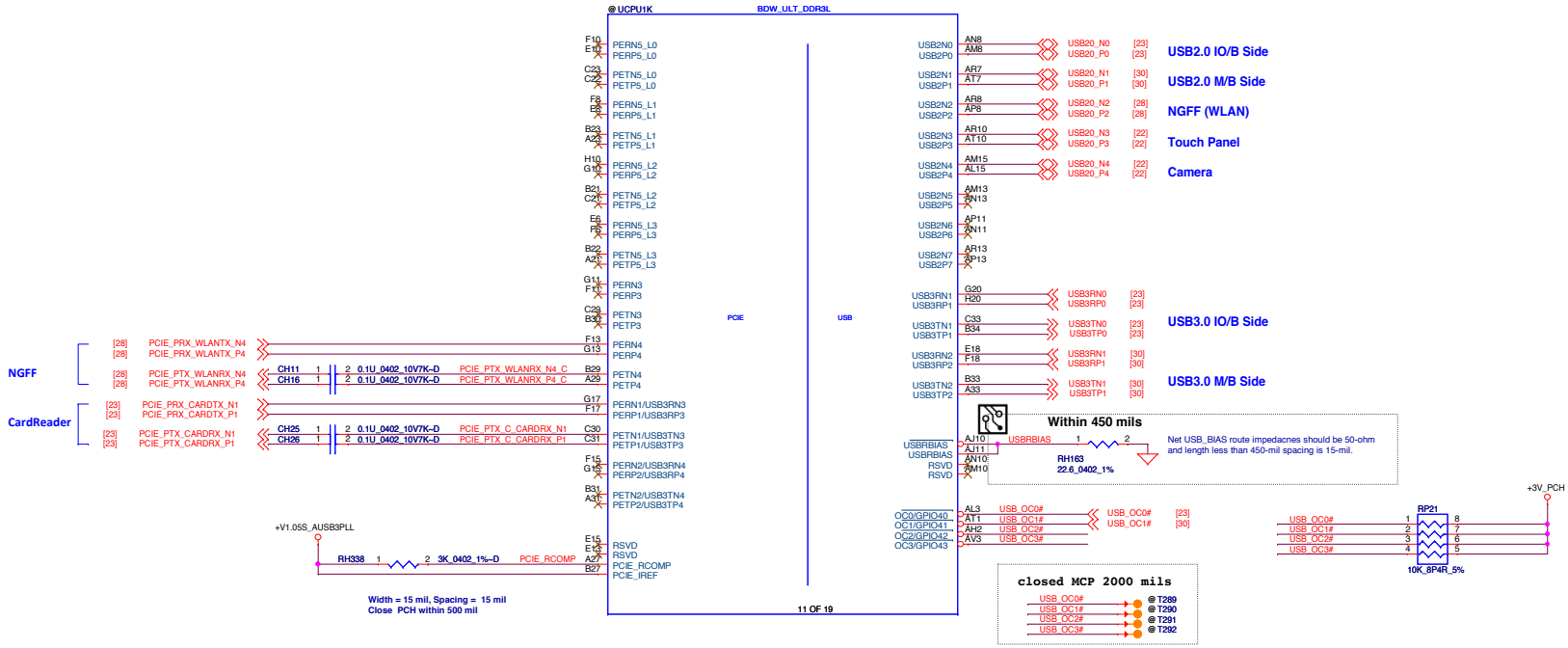
Compal Electronics, Inc.

Title: P11-MCP(7/10) PM,GPIO,LPIO,MISC

Size: | Document Number: LA-B441P | Rev: 1.0

Date: Sunday, October 05, 2014 | Sheet 11 of 50

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|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2013/07/04 | Deciphered Date | 2013/10/28 |

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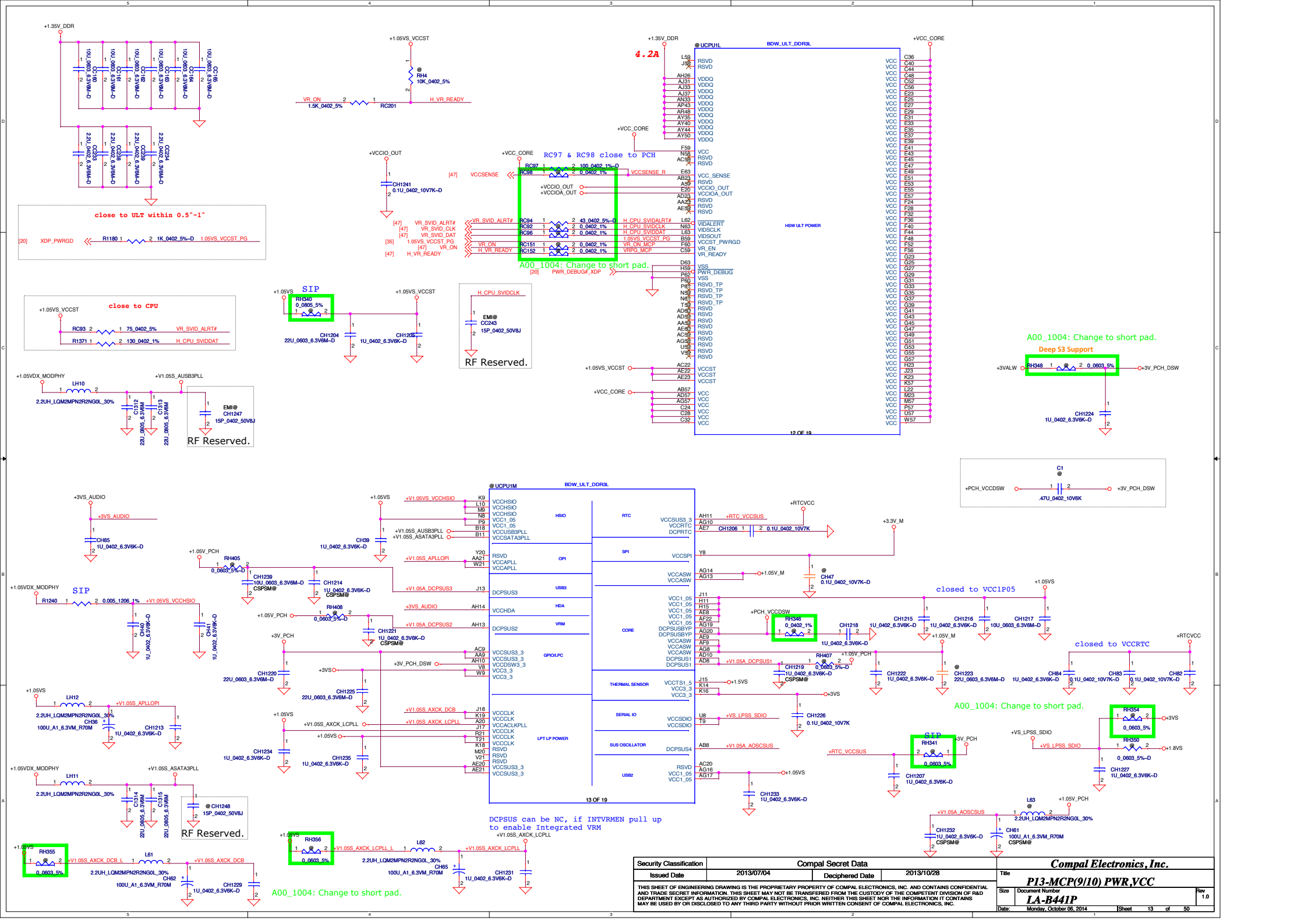
| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title | P12-MCP(8/10) PCIE,USB | | |
| Size | Document Number | | Rev |
| | LA-B441P | | 1.0 |
| Date: | Saturday, October 04, 2014 | Sheet | 12 of 50 |




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2013/07/04 | Deciphered Date | 2013/10/28 |

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**Compal Electronics, Inc.**

Title: P13-MCP(9/10) PWR,VCC

| Size | Document Number | Rev |
|---|---|---|
| | LA-B441P | 1.0 |

Date: Monday, October 06, 2014 | Sheet 13 of 50

Place a test point pad to within 250 ps of the ROC_TCK pin.and the maximum distance of test point pad to the termination must not be over 200 ps.

@T293 CFG3

2 1 CFG4
1K_0402_1%~D RC81

**eDP Strap**

| | |
|---|---|
| CFG4 | 1 : Disabled; No Physical Display Port attached to Embedded Display Port<br>* 0 : Enabled; An external Display Port device is connected to the Embedded Display Port |

8.2K_0402_1% 2 1 RC155 TD_IREF
49.9_0402_1%~D 2 1 RC153 CFG_RCOMP
49.9_0402_1%~D 2 1 RC154 PROC_OPI_COMP
Width = 15 mil, Spacing = 15 mil
Close PCH within 500 mil

@UCPU1S BDW_ULT_DDR3L

| | | | | | |
|---|---|---|---|---|---|
| [20] CFG0 | AC60 | CFG0 | RSVD_TP | AV63 | |
| [20] CFG1 | AC62 | CFG1 | RSVD_TP | AU63 | |
| [20] CFG2 | AC63 | CFG2 | | | |
| [20] CFG3 | CFG3 | AA63 | CFG3 | | |
| [20] CFG4 | CFG4 | AA60 | CFG4 | RSVD_TP | C63 |
| [20] CFG5 | | Y62 | CFG5 | RSVD_TP | C62 |
| [20] CFG6 | | Y61 | CFG6 | RSVD | B43 |
| [20] CFG7 | | Y60 | CFG7 | | |
| [20] CFG8 | | V62 | CFG8 | RSVD_TP | A51 |
| [20] CFG9 | | V61 | CFG9 | RSVD_TP | B51 |
| [20] CFG10 | | V60 | CFG10 | | |
| [20] CFG11 | | U60 | CFG11 | RSVD_TP | L60 |
| [20] CFG12 | | T63 | CFG12 | | |
| [20] CFG13 | | T62 | CFG13 | RSVD | N60 |
| [20] CFG14 | | T61 | CFG14 | | |
| [20] CFG15 | | T60 | CFG15 | RSVD | W23 |
| | | | | RSVD | Y22 |
| [20] CFG16 | AA62 | CFG16 | | RSVD | AY15 |
| [20] CFG18 | U63 | CFG18 | | PROC_OPI_RCOMP | PROC_OPI_COMP |
| [20] CFG17 | AA61 | CFG17 | | | |
| [20] CFG19 | U62 | CFG19 | | RSVD | AV62 |
| | | | | RSVD | D58 |
| CFG_RCOMP | V63 | CFG_RCOMP | | VSS | P22 |
| | A5 | RSVD | | VSS | N21 |
| | E1 | | | | |
| | D1 | RSVD | | RSVD | P20 |
| | J20 | RSVD | | RSVD | R20 |
| | H19 | RSVD | | | |
| TD_IREF | B12 | RSVD | | | |
| | | TD_IREF | | | |

RESERVED

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@UCPU1N BDW_ULT_DDR3L

| | | | |
|---|---|---|---|
| A11 | VSS | VSS | AJ35 |
| A14 | VSS | VSS | AJ39 |
| A18 | VSS | VSS | AJ41 |
| A24 | VSS | VSS | AJ43 |
| A28 | VSS | VSS | AJ45 |
| A32 | VSS | VSS | AJ47 |
| A36 | VSS | VSS | AJ50 |
| A40 | VSS | VSS | AJ52 |
| A44 | VSS | VSS | AJ54 |
| A48 | VSS | VSS | AJ56 |
| AS2 | VSS | VSS | AJ58 |
| A56 | VSS | VSS | AJ60 |
| AA1 | VSS | VSS | AJ63 |
| AA58 | VSS | VSS | AK23 |
| AB10 | VSS | VSS | AK3 |
| AB20 | VSS | VSS | AK52 |
| AB22 | VSS | VSS | AL10 |
| AB7 | VSS | VSS | AL13 |
| AC61 | VSS | VSS | AL17 |
| AD21 | VSS | VSS | AL20 |
| AD5 | VSS | VSS | AL22 |
| AD63 | VSS | VSS | AL23 |
| AE10 | VSS | VSS | AL26 |
| AE5 | VSS | VSS | AL29 |
| AE58 | VSS | VSS | AL31 |
| AF11 | VSS | VSS | AL33 |
| AF12 | VSS | VSS | AL36 |
| AF14 | VSS | VSS | AL39 |
| AF15 | VSS | VSS | AL40 |
| AF17 | VSS | VSS | AL45 |
| AF18 | VSS | VSS | AL46 |
| AG1 | VSS | VSS | AL51 |
| AG11 | VSS | VSS | AL52 |
| AG21 | VSS | VSS | AL54 |
| AG23 | VSS | VSS | AL57 |
| AG60 | VSS | VSS | AL60 |
| AG61 | VSS | VSS | AL61 |
| AG62 | VSS | VSS | AM1 |
| AG63 | VSS | VSS | AM17 |
| AH17 | VSS | VSS | AM23 |
| AH19 | VSS | VSS | AM31 |
| AH20 | VSS | VSS | AM52 |
| AH22 | VSS | VSS | AN17 |
| AH24 | VSS | VSS | AN23 |
| AH28 | VSS | VSS | AN31 |
| AH30 | VSS | VSS | AN32 |
| AH32 | VSS | VSS | AN35 |
| AH34 | VSS | VSS | AN36 |
| AH36 | VSS | VSS | AN39 |
| AH38 | VSS | VSS | AN40 |
| AH40 | VSS | VSS | AN42 |
| AH42 | VSS | VSS | AN43 |
| AH44 | VSS | VSS | AN45 |
| AH49 | VSS | VSS | AN46 |
| AH51 | VSS | VSS | AN48 |
| AH53 | VSS | VSS | AN49 |
| AH55 | VSS | VSS | AN51 |
| AH57 | VSS | VSS | AN52 |
| AJ13 | VSS | VSS | AN60 |
| AJ14 | VSS | VSS | AN63 |
| AJ23 | VSS | VSS | AN7 |
| AJ25 | VSS | VSS | AP10 |
| AJ27 | VSS | VSS | AP17 |
| AJ29 | VSS | VSS | AP20 |

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@UCPU1O BDW_ULT_DDR3L

| | | | |
|---|---|---|---|
| AP22 | VSS | VSS | AV59 |
| AP23 | VSS | VSS | AV8 |
| AP28 | VSS | VSS | AW16 |
| AP29 | VSS | VSS | AW24 |
| AP3 | VSS | VSS | AW33 |
| AP31 | VSS | VSS | AW35 |
| AP38 | VSS | VSS | AW37 |
| AP39 | VSS | VSS | AW4 |
| AP48 | VSS | VSS | AW40 |
| AP52 | VSS | VSS | AW42 |
| AP54 | VSS | VSS | AW44 |
| AP57 | VSS | VSS | AW47 |
| AR11 | VSS | VSS | AW50 |
| AR15 | VSS | VSS | AW51 |
| AR17 | VSS | VSS | AW59 |
| AR23 | VSS | VSS | AW60 |
| AR31 | VSS | VSS | AY11 |
| AR33 | VSS | VSS | AY16 |
| AR39 | VSS | VSS | AY18 |
| AR43 | VSS | VSS | AY22 |
| AR49 | VSS | VSS | AY24 |
| AR5 | VSS | VSS | AY26 |
| AR52 | VSS | VSS | AY30 |
| AT13 | VSS | VSS | AY33 |
| AT35 | VSS | VSS | AY4 |
| AT37 | VSS | VSS | AY51 |
| AT40 | VSS | VSS | AY53 |
| AT42 | VSS | VSS | AY57 |
| AT43 | VSS | VSS | AY59 |
| AT46 | VSS | VSS | AY6 |
| AT49 | VSS | VSS | B20 |
| AT61 | VSS | VSS | B24 |
| AT62 | VSS | VSS | B26 |
| AT63 | VSS | VSS | B28 |
| AU1 | VSS | VSS | B32 |
| AU16 | VSS | VSS | B36 |
| AU18 | VSS | VSS | B4 |
| AU20 | VSS | VSS | B40 |
| AU22 | VSS | VSS | B44 |
| AU24 | VSS | VSS | B48 |
| AU26 | VSS | VSS | B52 |
| AU28 | VSS | VSS | B56 |
| AU30 | VSS | VSS | B60 |
| AU33 | VSS | VSS | C11 |
| AU51 | VSS | VSS | C14 |
| AU53 | VSS | VSS | C18 |
| AU55 | VSS | VSS | C20 |
| AU57 | VSS | VSS | C25 |
| AU59 | VSS | VSS | C27 |
| AV14 | VSS | VSS | C38 |
| AV16 | VSS | VSS | C39 |
| AV20 | VSS | VSS | C57 |
| AV24 | VSS | VSS | D12 |
| AV28 | VSS | VSS | D14 |
| AV33 | VSS | VSS | D18 |
| AV34 | VSS | VSS | D2 |
| AV36 | VSS | VSS | D21 |
| AV39 | VSS | VSS | D23 |
| AV41 | VSS | VSS | D25 |
| AV43 | VSS | VSS | D26 |
| AV46 | VSS | VSS | D27 |
| AV49 | VSS | VSS | D29 |
| AV51 | VSS | VSS | D30 |
| AV55 | VSS | VSS | D31 |

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@UCPU1P BDW_ULT_DDR3L

| | | | |
|---|---|---|---|
| D33 | VSS | VSS | H17 |
| D34 | VSS | VSS | H57 |
| D35 | VSS | VSS | J10 |
| D37 | VSS | VSS | J22 |
| D38 | VSS | VSS | J59 |
| D39 | VSS | VSS | J63 |
| D41 | VSS | VSS | K1 |
| D42 | VSS | VSS | K12 |
| D43 | VSS | VSS | L13 |
| D45 | VSS | VSS | L15 |
| D46 | VSS | VSS | L17 |
| D47 | VSS | VSS | L18 |
| D49 | VSS | VSS | L20 |
| D5 | VSS | VSS | L58 |
| D50 | VSS | VSS | L61 |
| D51 | VSS | VSS | L7 |
| D53 | VSS | VSS | M22 |
| D54 | VSS | VSS | N10 |
| D55 | VSS | VSS | N3 |
| D57 | VSS | VSS | P59 |
| D59 | VSS | VSS | P63 |
| D62 | VSS | VSS | R10 |
| D8 | VSS | VSS | R22 |
| E11 | VSS | VSS | R8 |
| E17 | VSS | VSS | T1 |
| F20 | VSS | VSS | T58 |
| F26 | VSS | VSS | U20 |
| F30 | VSS | VSS | U22 |
| F34 | VSS | VSS | U61 |
| F38 | VSS | VSS | U9 |
| F42 | VSS | VSS | V10 |
| F46 | VSS | VSS | V3 |
| F50 | VSS | VSS | V7 |
| F54 | VSS | VSS | W20 |
| F58 | VSS | VSS | W22 |
| F61 | VSS | VSS | Y10 |
| G18 | VSS | VSS | Y59 |
| G22 | VSS | VSS | Y63 |
| G3 | VSS | | |
| G5 | VSS | | V58 |
| G6 | VSS | VSS | AH46 |
| G8 | VSS | VSS | V23 |
| H13 | VSS | VSS | E62 |
| | VSS | VSS_SENSE | AH16 |

16 OF 19

RC99 & RC100 close to PCH
RC100 1 2 100_0402_1%~D
VSSSENSE [47]

| | | | |
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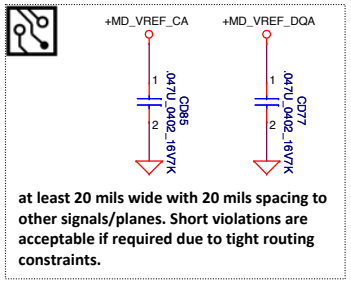
**Compal Electronics, Inc.**

Title: **P14-MCP(10/10) PWR,VSS,CFG**

| Size | Document Number | Rev |
|---|---|---|
| | LA-B441P | 1.0 |

Date: Saturday, October 04, 2014 Sheet 14 of 50

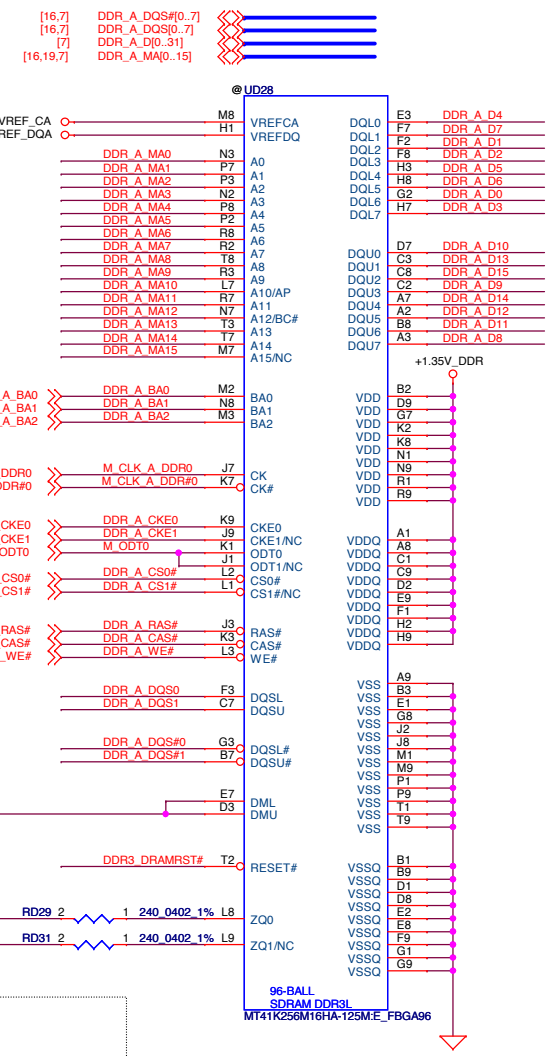
# CHA DDR3L Memory Down Lower Bits

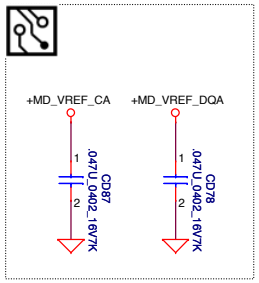


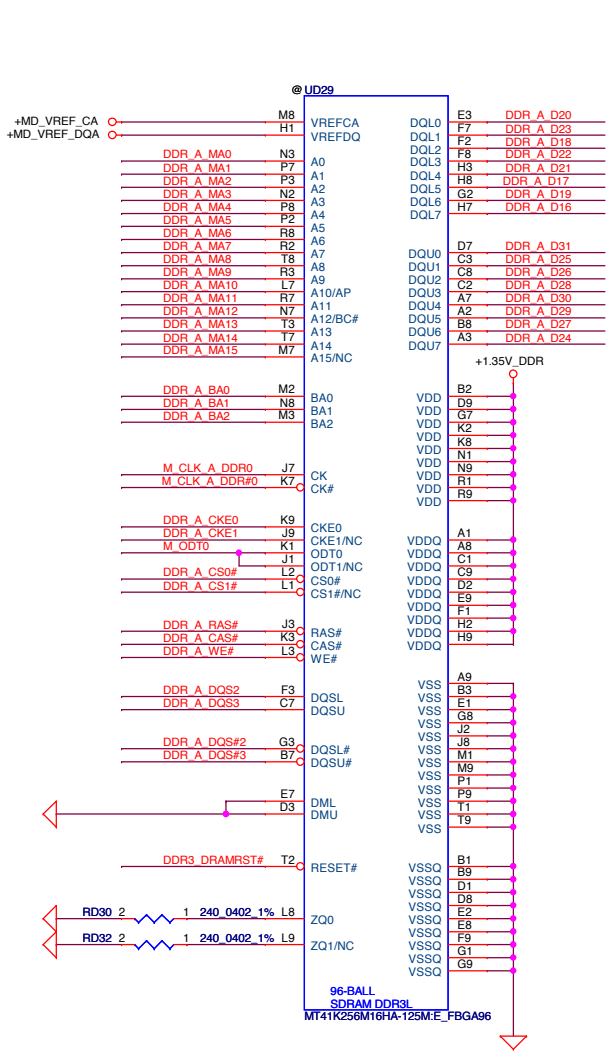

at least 20 mils wide with 20 mils spacing to other signals/planes. Short violations are acceptable if required due to tight routing constraints.

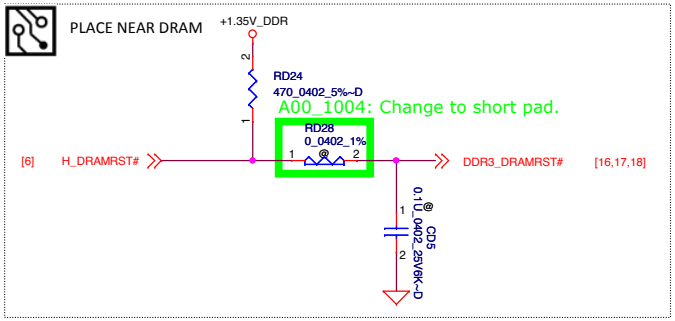
**DDR3L Package (mm^2)**

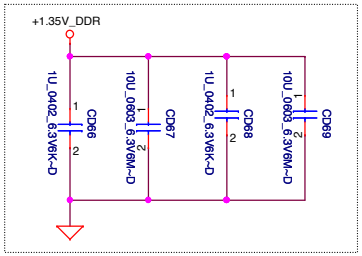
| | 4G | 8G |
|---|---|---|
| Hynix | 9 x 13 | TBD |
| Samsung | 10 x 13 | 11 x 13.3 |
| Micron | 9 x 14 | 10 x 14 |

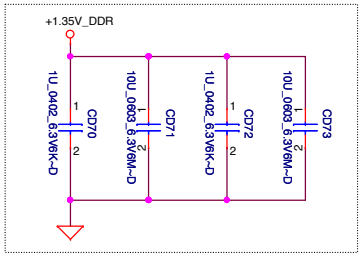



| | | | |
|---|---|---|---|
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| Issued Date | 2013/07/04 | Deciphered Date | 2013/10/28 |

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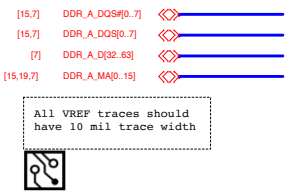
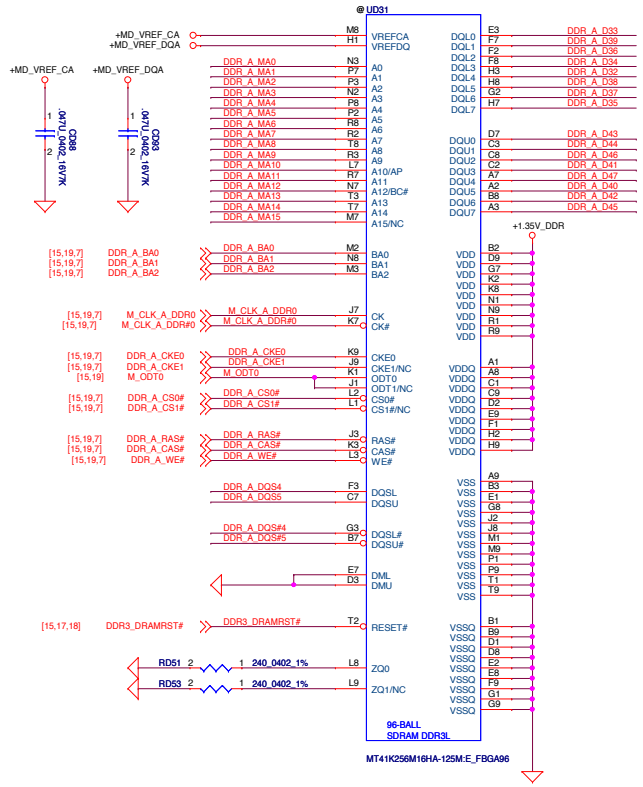
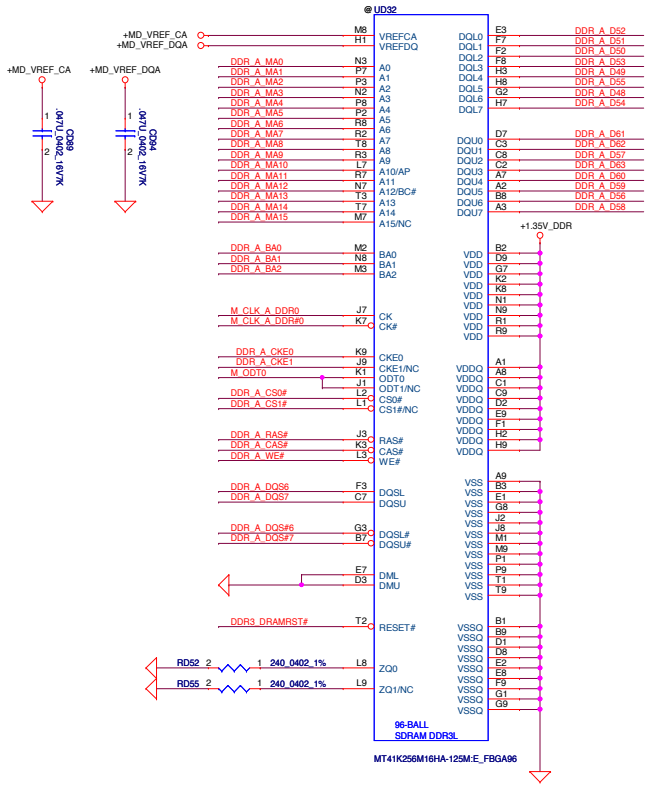
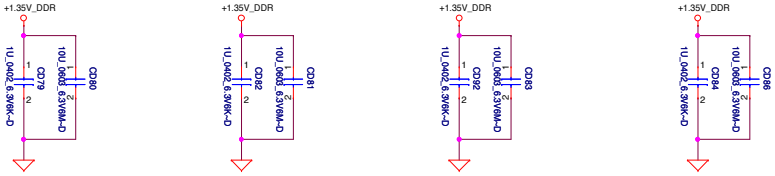
| | | | |
|---|---|---|---|
| Title | P12-DDRIII Channel A | | |
| Size | Document Number | | Rev |
| | LA-B441P | | 1.0 |
| Date: | Sunday, October 05, 2014 | Sheet | 15 of 50 |

# CHA DDR3L Memory Down Upper Bits




| | | | |
|---|---|---|---|
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| Issued Date | 2013/07/04 | Deciphered Date | 2013/10/28 |

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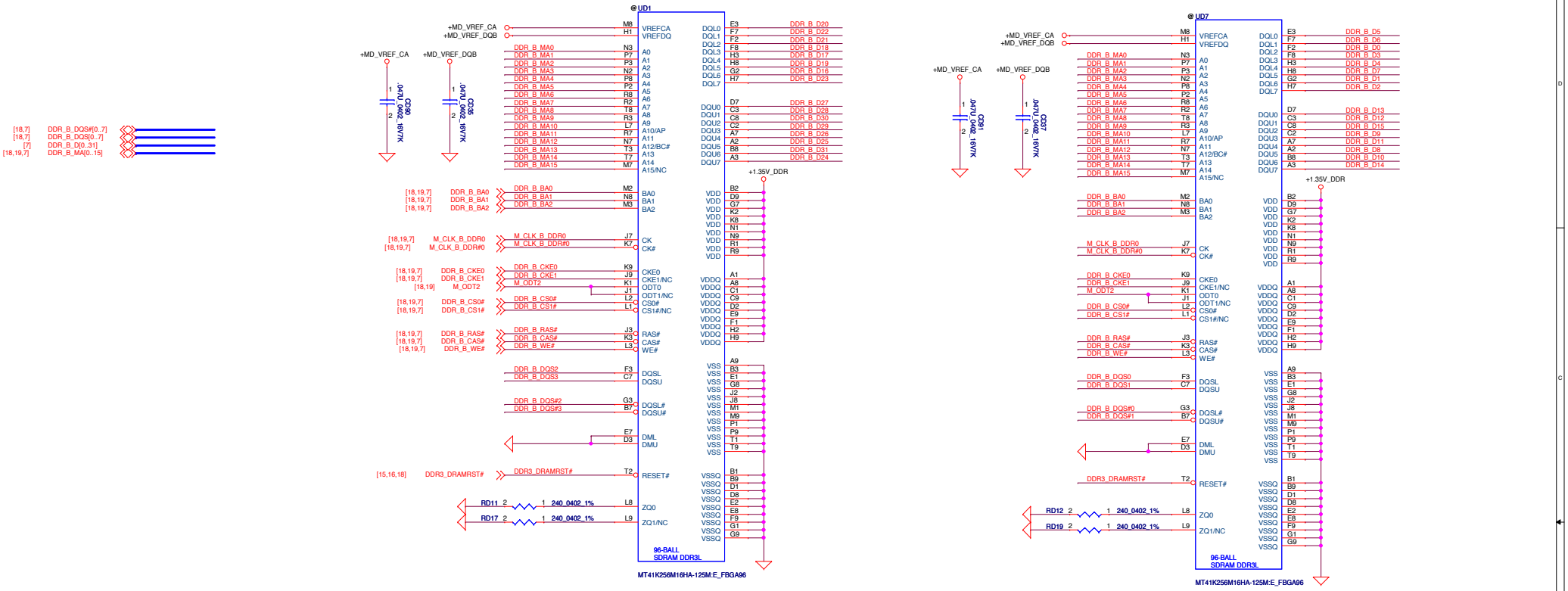
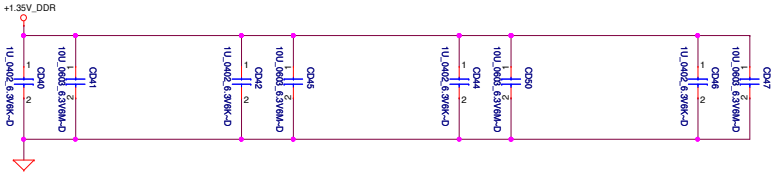
| | | | |
|---|---|---|---|
| Title | P13-DDRIII Channel A | | |
| Size | Document Number | | Rev |
| | LA-B441P | | 1.0 |
| Date: | Saturday, October 04, 2014 | Sheet | 16 of 50 |

# CHB DDR3L Memory Down Lower Bits




| | | | |
|---|---|---|---|
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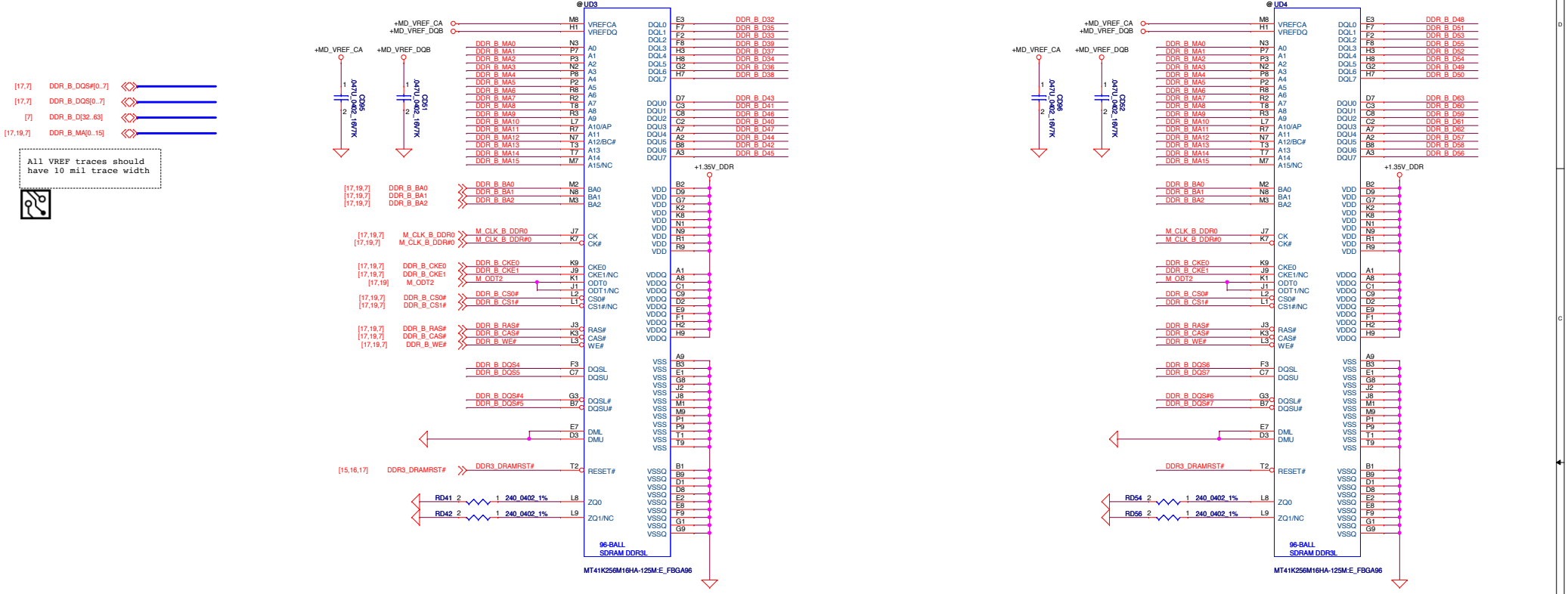
**Compal Electronics, Inc.**

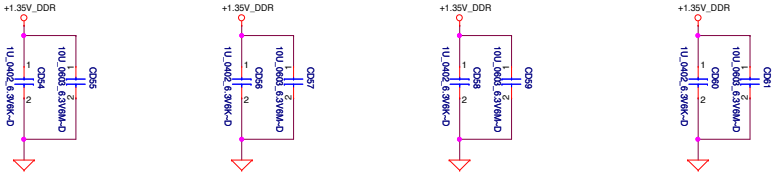
Title: **P14-DDRIII Channel B**

| Size | Document Number | Rev |
|---|---|---|
| | LA-B441P | 1.0 |

Date: Saturday, October 04, 2014 | Sheet 17 of 50

# CHB DDR3L Memory Down Upper Bits

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|---|---|---|---|
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| Issued Date | 2013/07/04 | Deciphered Date | 2013/10/28 |

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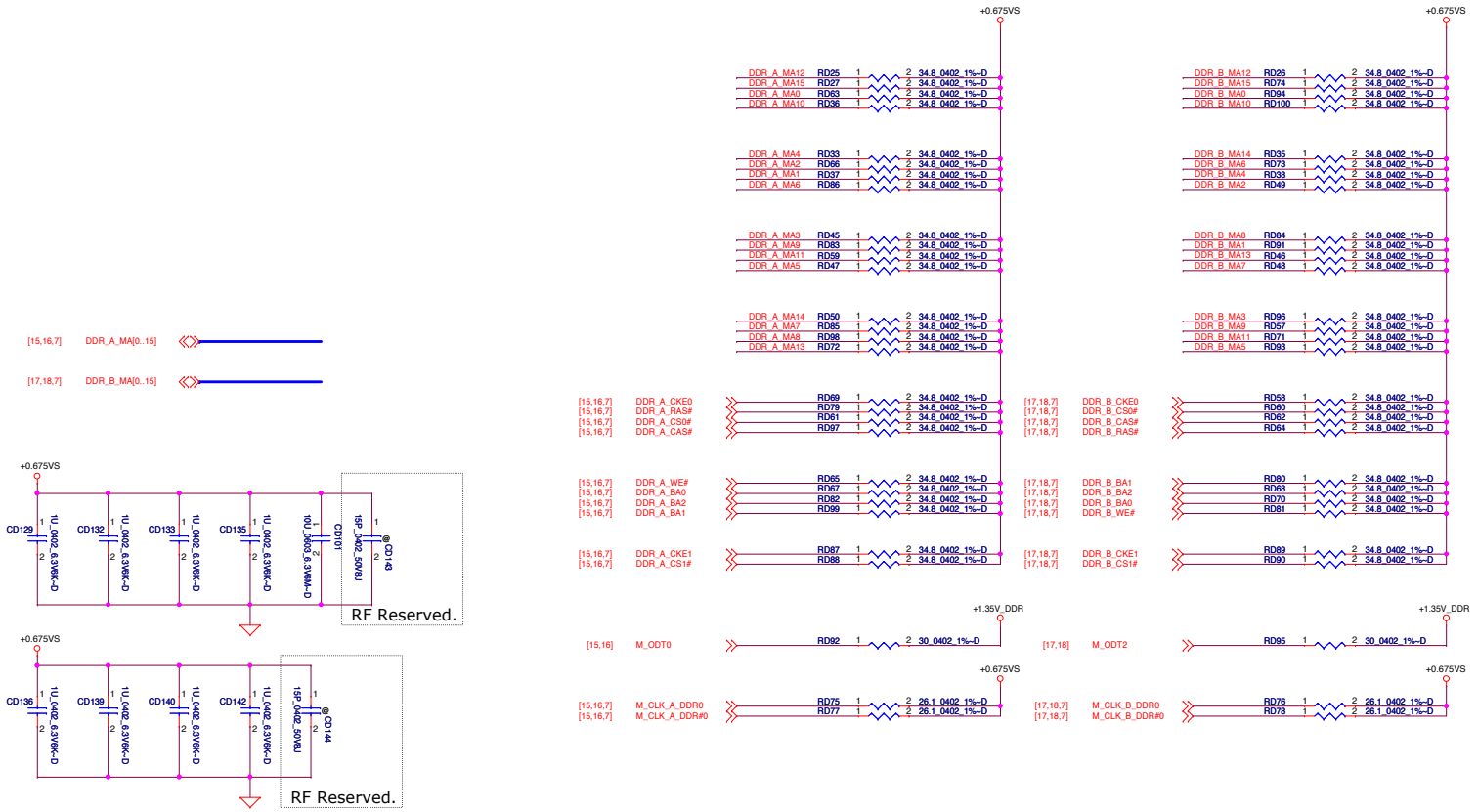
Compal Electronics, Inc.

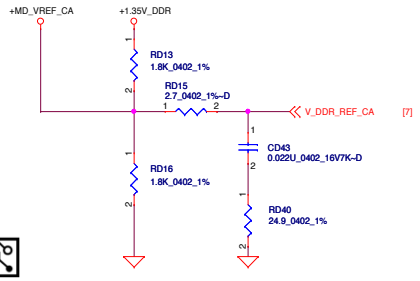
Title: P15-DDRIII Channel B

| Size | Document Number | Rev |
|---|---|---|
| | LA-B441P | 1.0 |

Date: Saturday, October 04, 2014 Sheet 18 of 50

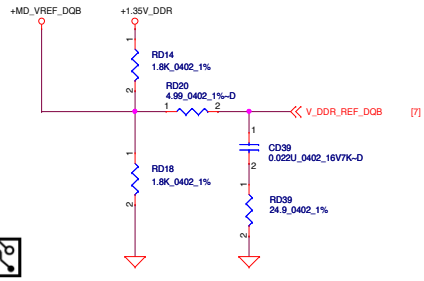



## Channel A/B CA VREF



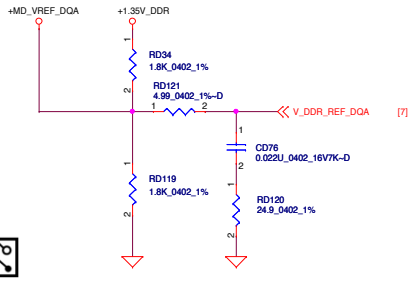

Place the VREF voltage dividers as close as possible to the SO-DIMMs or memory down DRAM devices.

## Channel B DQ VREF




Place the VREF voltage dividers as close as possible to the SO-DIMMs or memory down DRAM devices.

## Channel A DQ VREF




Place the VREF voltage dividers as close as possible to the SO-DIMMs or memory down DRAM devices.

| | | | |
|---|---|---|---|
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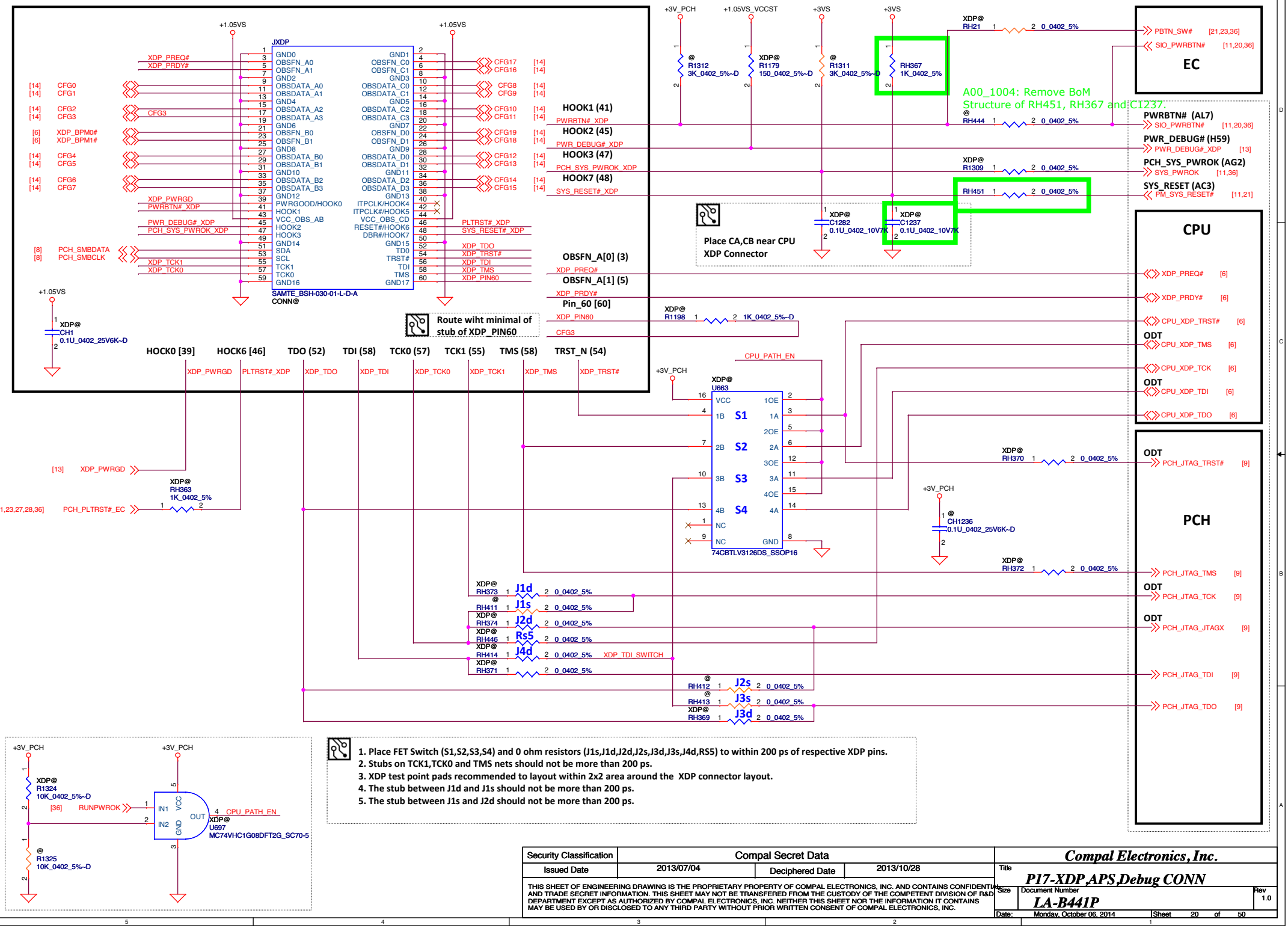
Compal Electronics, Inc.

Title: P16-DDRIII Channel B

Size | Document Number: LA-B441P | Rev: 1.0

Date: Saturday, October 04, 2014 | Sheet 19 of 50

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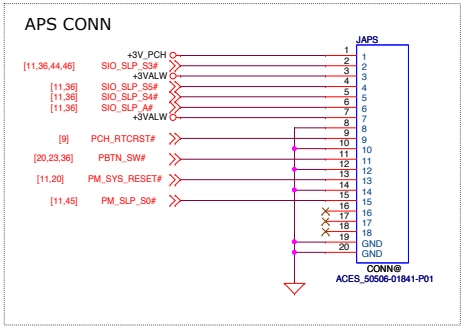
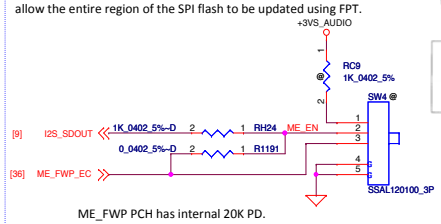
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title: P17-XDP,APS,Debug CONN | | | |
| Size | Document Number: LA-B441P | | Rev: 1.0 |
| Date: Monday, October 06, 2014 | | Sheet 20 of 50 | |

## APS CONN




A00_1004: Depop SW4, RC9; pop R1191.

Service Mode Switch:
Add a switch to ME_FWP signal to unlock the ME region and allow the entire region of the SPI flash to be updated using FPT.




ME_FWP PCH has internal 20K PD.

| FLASH DESCRIPTOR SECURITY OVERRIDE |
|---|
| Disable ME Protect (ME can be updated) ----> Pin1 & Pin2 short |
| Enable ME Protect (ME cannot be updated)-->Pin3 & Pin2 short(Default position) |

| | | | |
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| Issued Date | 2013/07/04 | Deciphered Date | 2013/10/28 |

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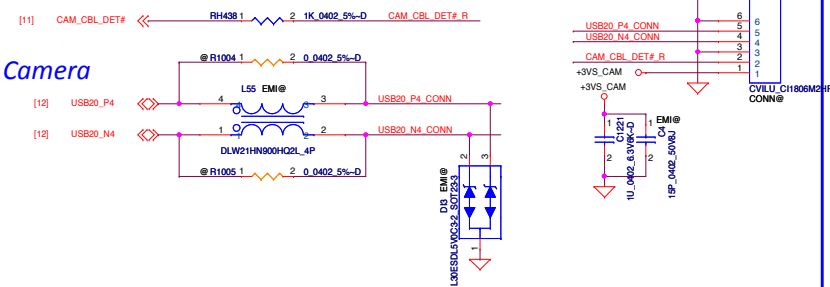
**Compal Electronics, Inc.**

Title: **P18-BLANK**

Size | Document Number: **LA-B441P** | Rev: 1.0

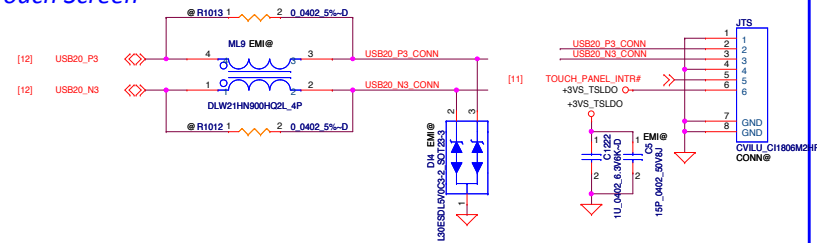
Date: Monday, October 06, 2014 | Sheet 21 of 50

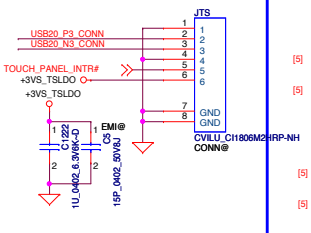
## Camera + Touch Screen



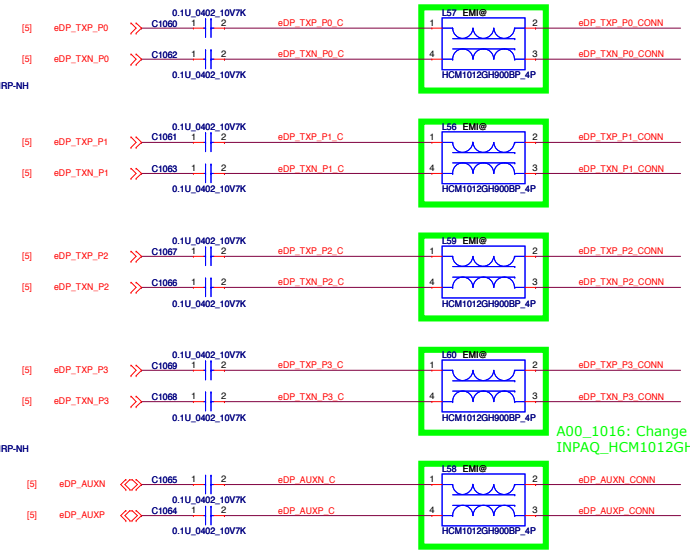

## Camera

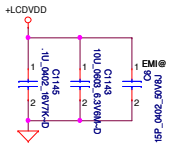
## Touch Screen

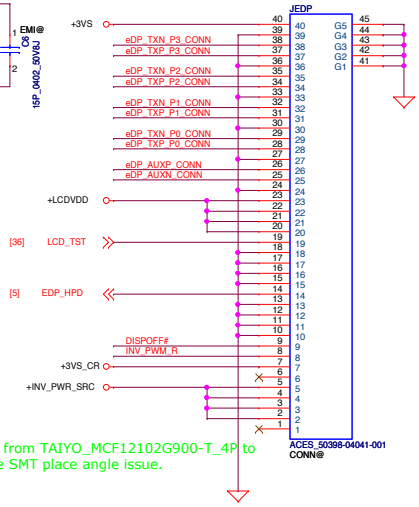



## eDP Conn

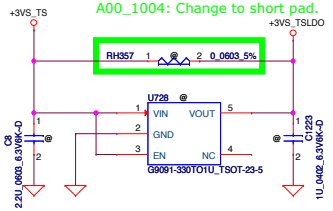


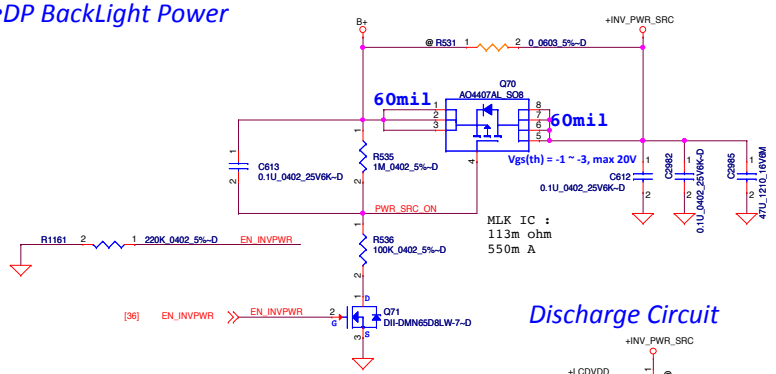

A00_1016: Change L56~L60 footprint from TAIYO_MCF12102G900-T_4P to INPAQ_HCM1012GH900BP_4P to solve SMT place angle issue.

## Touch Screen LDO

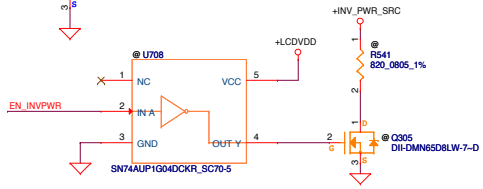



A00_1004: Change to short pad.

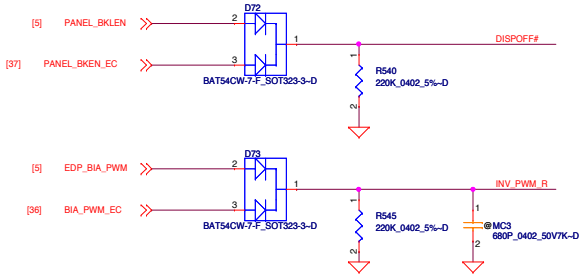
## eDP BackLight Power




## Discharge Circuit




## BackLight PWM Control

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| Security Classification | Compal Secret Data | | |
| Issued Date | 2013/07/04 | Deciphered Date | 2013/10/28 |

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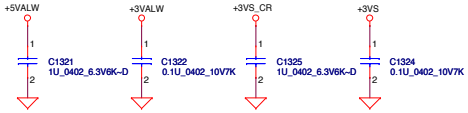
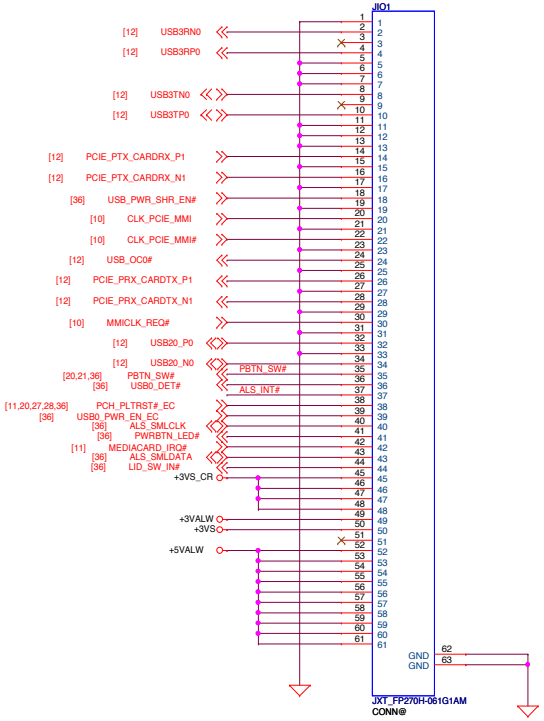
**Compal Electronics, Inc.**

Title: P19-eDP/ Camera CONN

Size: | Document Number: LA-B441P | Rev: 1.0

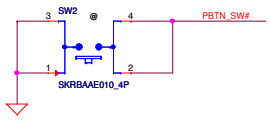
Date: Thursday, October 16, 2014 | Sheet 22 of 50

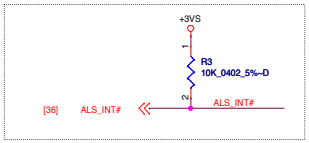



R06_0822: De-pop power switch on MB.

NPI Stage Power Switch




| | | | |
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| Security Classification | Compal Secret Data | | |
| Issued Date | 2013/07/04 | Deciphered Date | 2013/10/28 |

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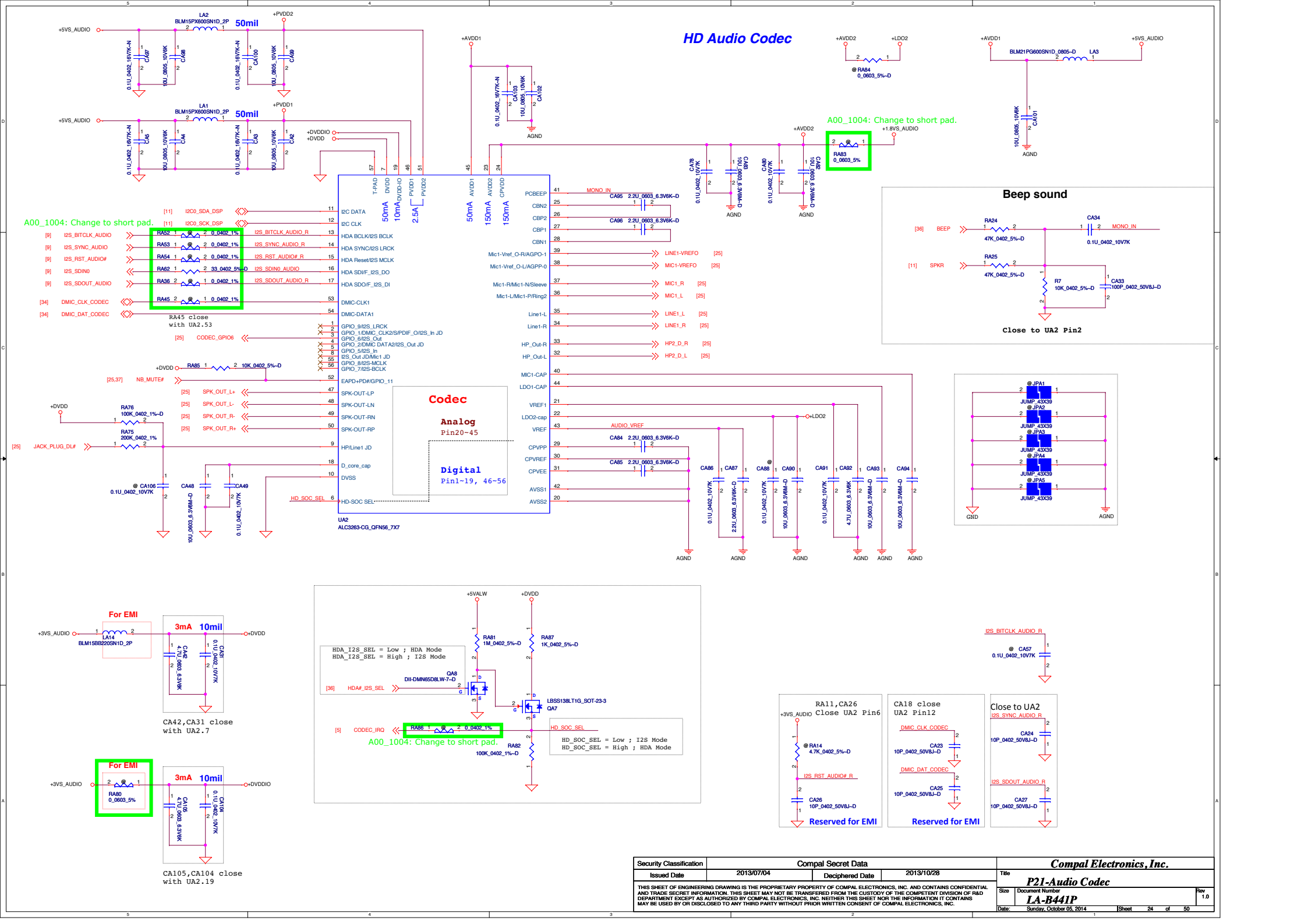
Compal Electronics, Inc.

Title: P20-BTB CONN & Battery LED

| Size | Document Number | Rev |
|---|---|---|
| | LA-B441P | 1.0 |

Date: Saturday, October 04, 2014 Sheet 23 of 50

# HD Audio Codec

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|---|---|---|---|
| Security Classification | Compal Secret Data | | Compal Electronics, Inc. |
| Issued Date | 2013/07/04 | Deciphered Date | 2013/10/28 |
| Title | P21-Audio Codec | | |
| Size | Document Number | | Rev |
| | LA-B441P | | 1.0 |
| Date: | Sunday, October 05, 2014 | Sheet | 24 of 50 |

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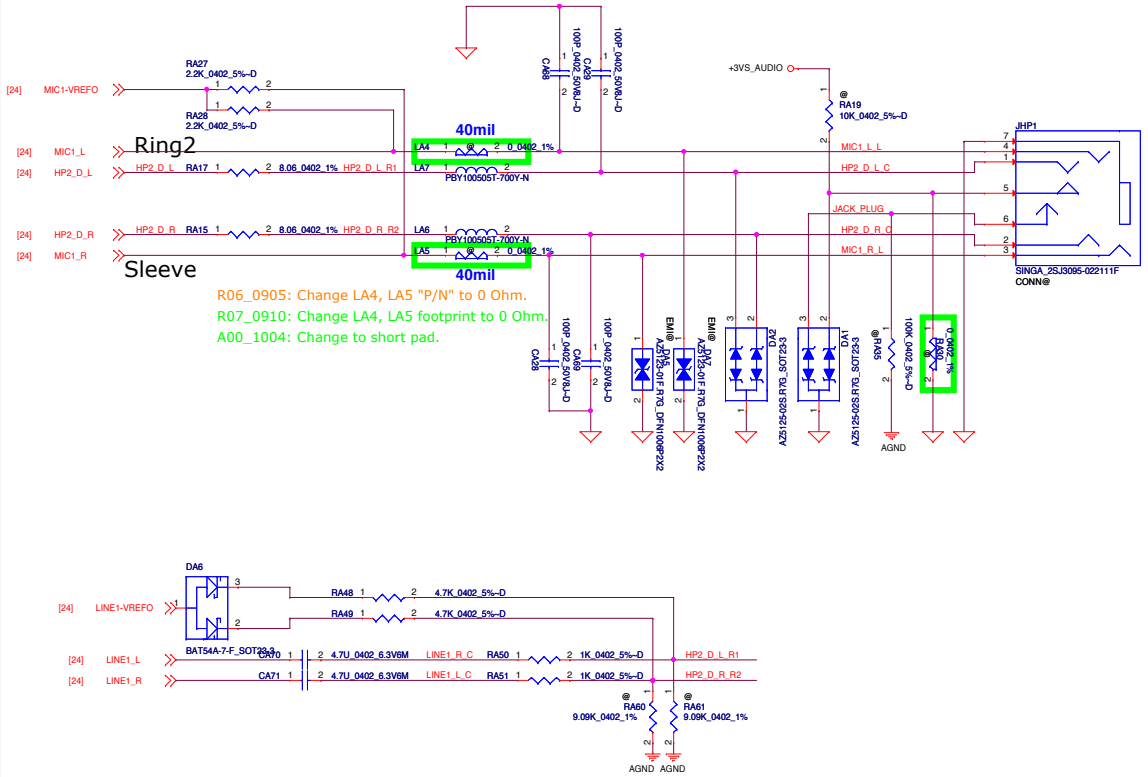
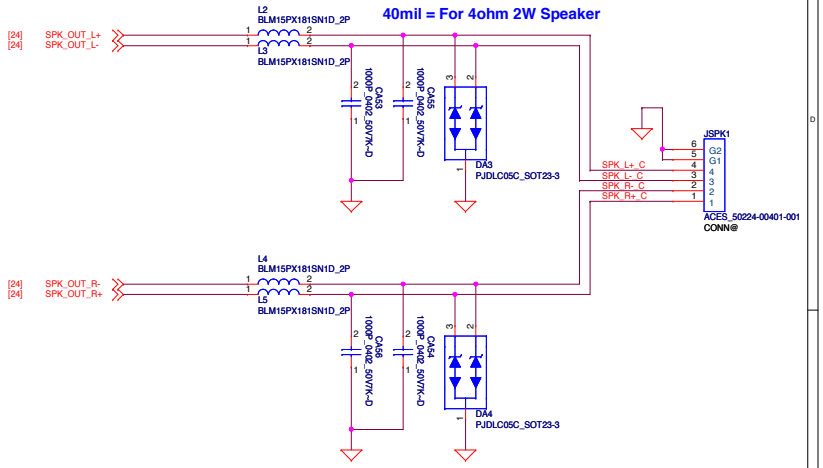
# Universal Audio Jack



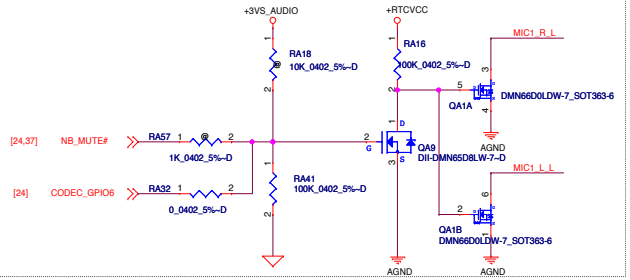

R06_0905: Change LA4, LA5 "P/N" to 0 Ohm.
R07_0910: Change LA4, LA5 footprint to 0 Ohm.
A00_1004: Change to short pad.



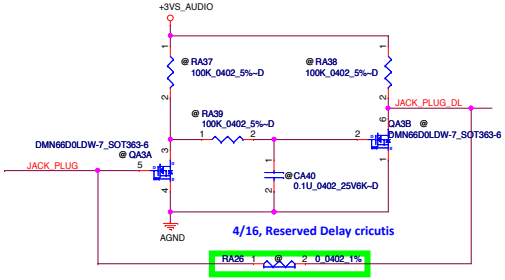

# Int. Speaker Conn.



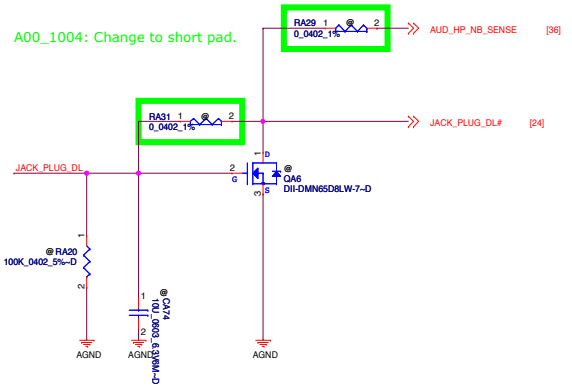

## Prevent S3/S4/S5 Background Noise.




## Reserved Delay cricutis




A00_1004: Change to short pad.

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Compal Electronics, Inc.

Title: P22-Audio Conn

| Size | Document Number | Rev |
|---|---|---|
| | LA-B441P | 1.0 |

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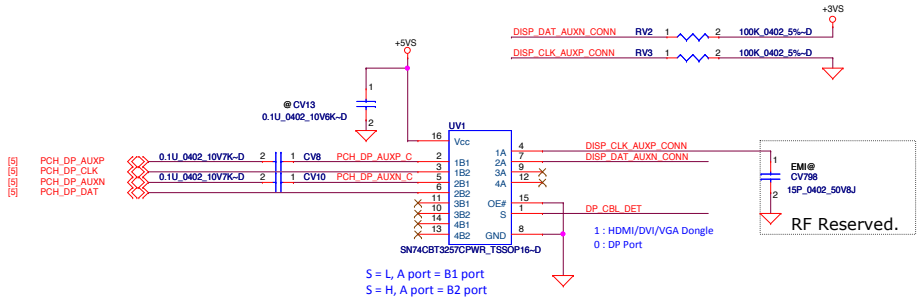
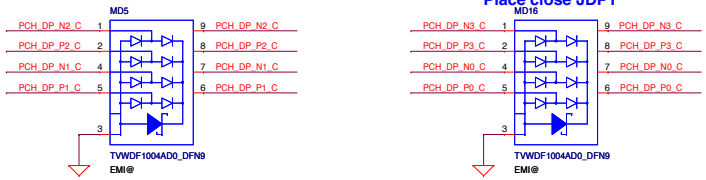


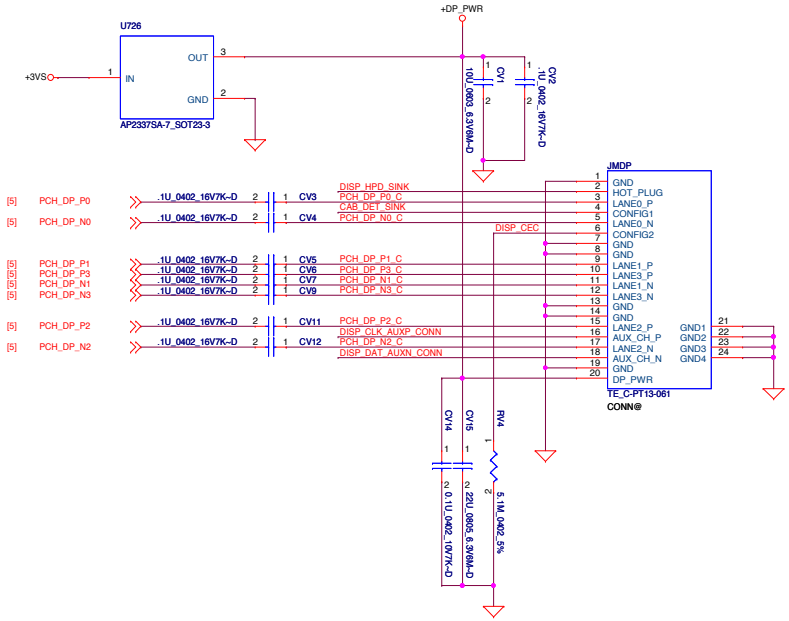

## DP Signal ESD

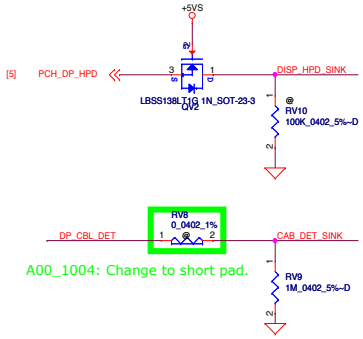



Place close JDP1




## Mini DP CONN




A00_1004: Change to short pad.

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2013/07/04 | Deciphered Date | 2013/10/28 |

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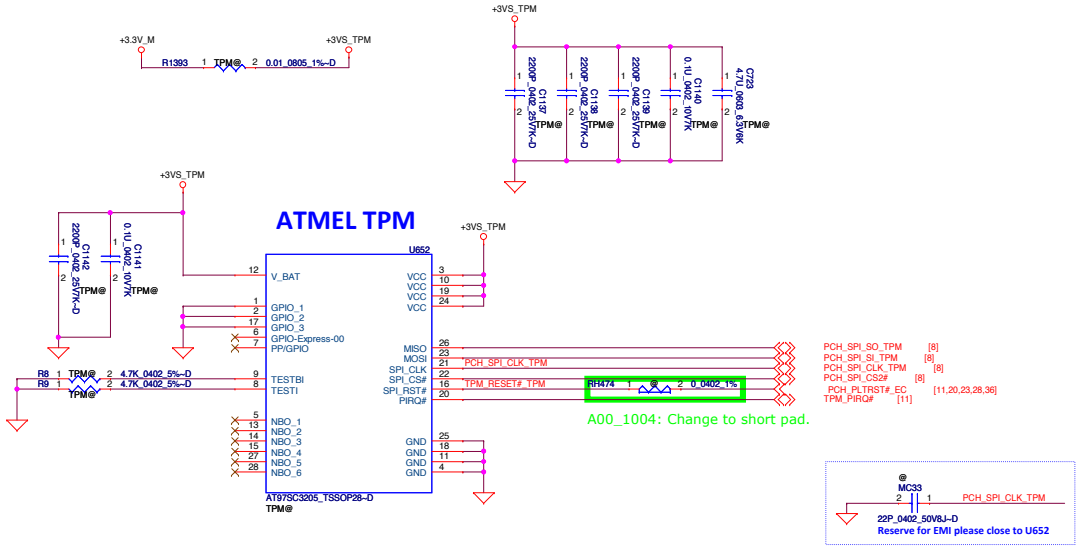
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title | P23-Mini DP CONN | | |
| Size C | Document Number LA-B441P | | Rev 1.0 |
| Date: Sunday, October 05, 2014 | Sheet 26 of 50 | | |





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|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2013/07/04 | Deciphered Date | 2013/10/28 |

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Compal Electronics, Inc.

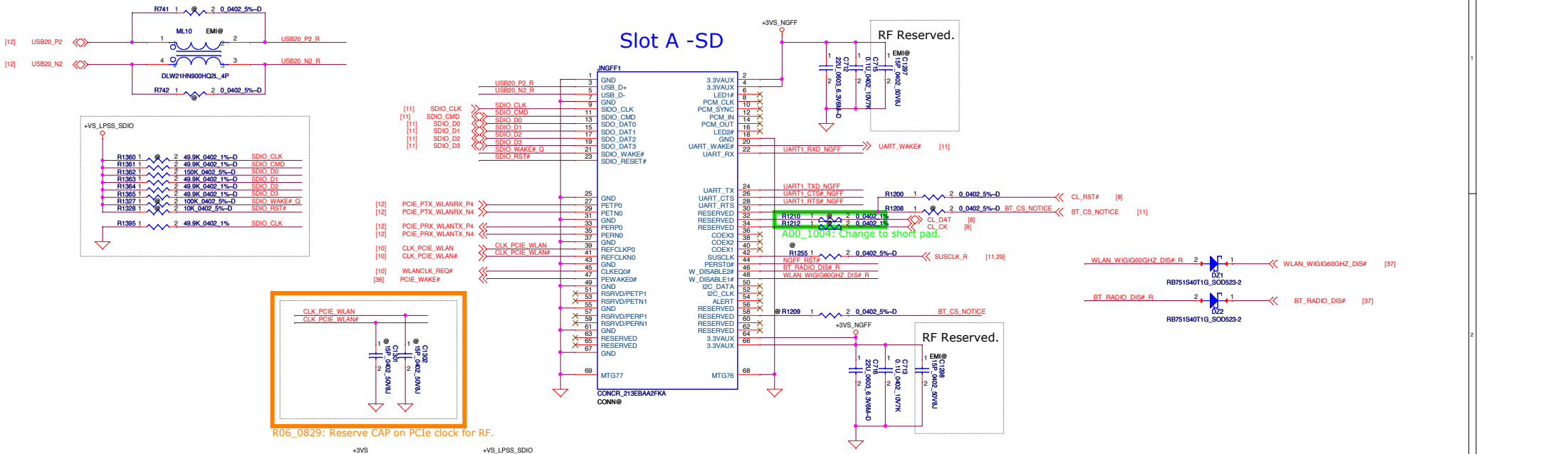
Title: P24-TPM

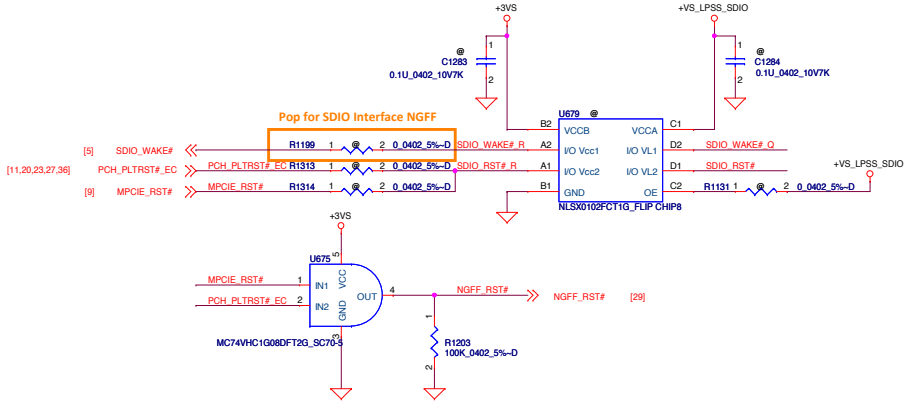
Size | Document Number: LA-B441P | Rev: 1.0

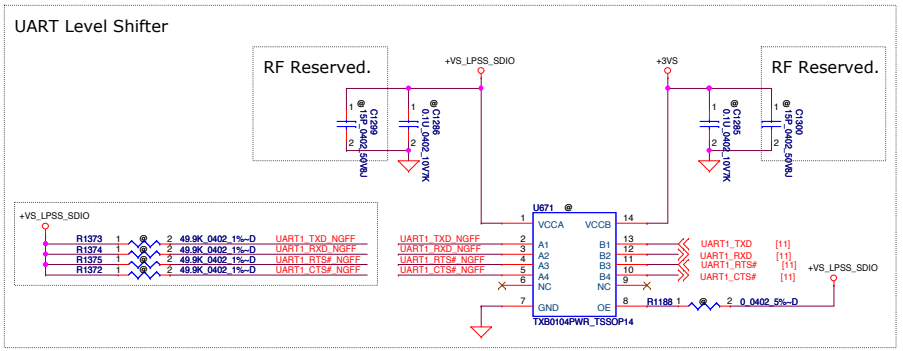
Date: Sunday, October 05, 2014 | Sheet 27 of 50

# Wireless LAN

## Slot A -SD




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2013/07/04 | Deciphered Date | 2013/10/28 |

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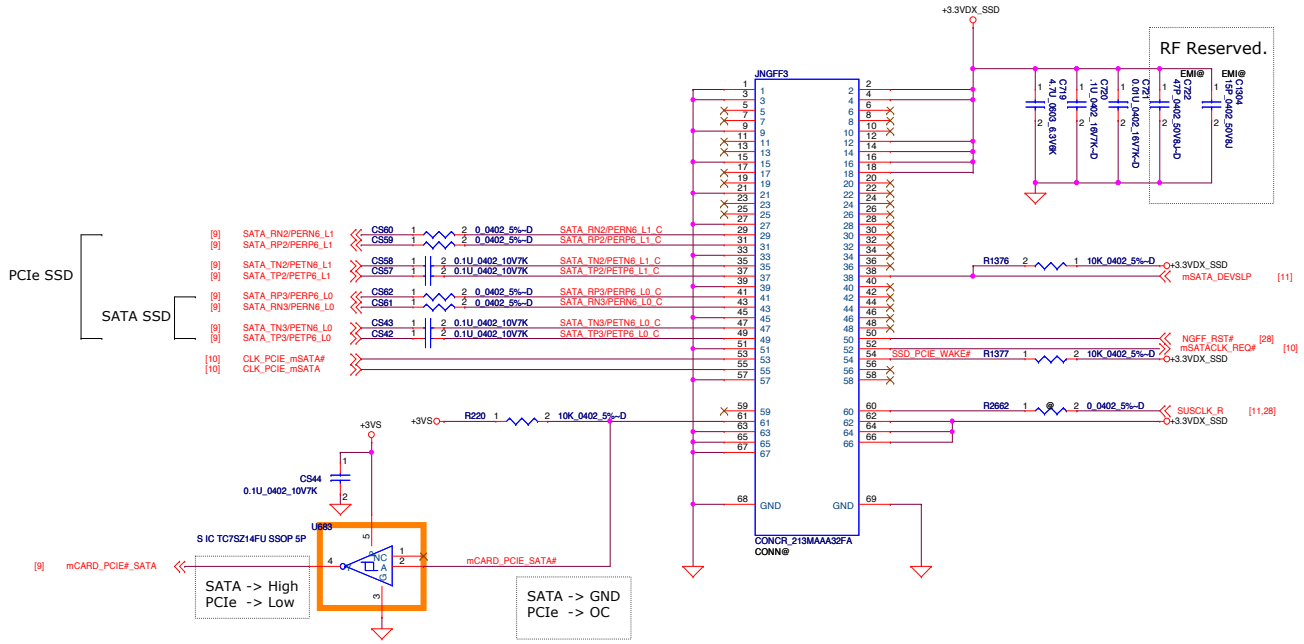
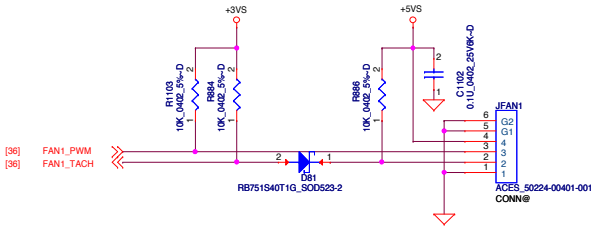
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title | P25-WLAN / BT (M.2) | | |
| Size | Document Number | | Rev |
| | LA-B441P | | 1.0 |
| Date: | Sunday, October 05, 2014 | Sheet | 28 of 50 |

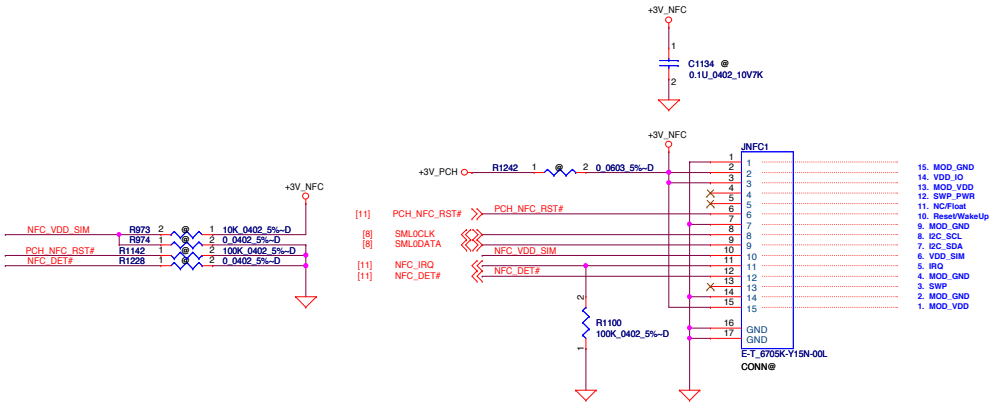
# M.2 Slot-C Key-M (SSD)




# FAN




# NFC(Reserved)

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| Issued Date | 2013/07/04 | Deciphered Date 2013/10/28 | Title: P26-mSATA / NFC / FAN Conn |
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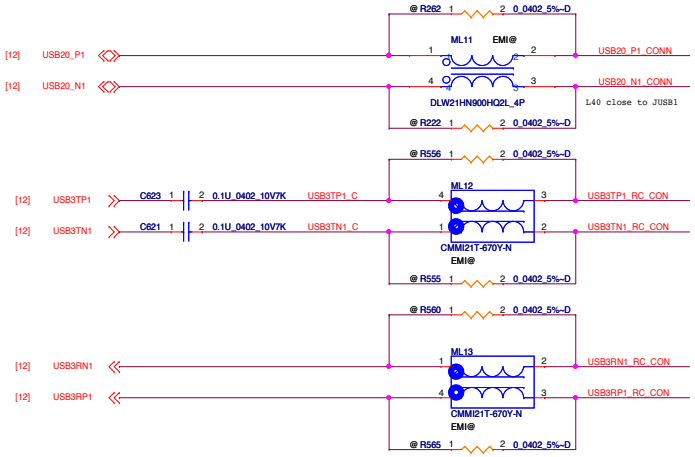
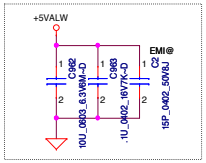
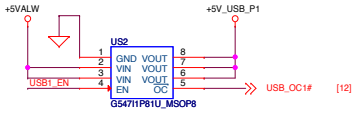
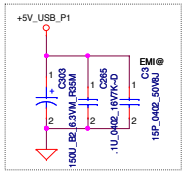
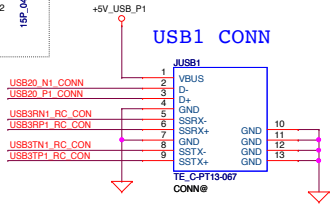
# USB IO Port



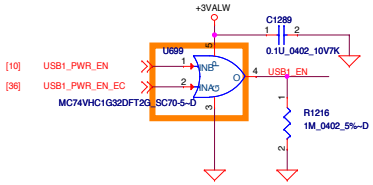



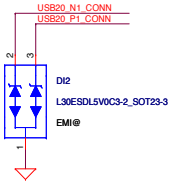



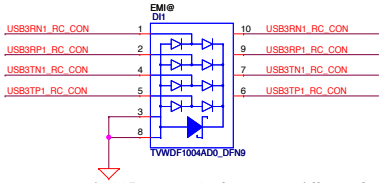




R06_0822: Change P/N to suffix '0'.

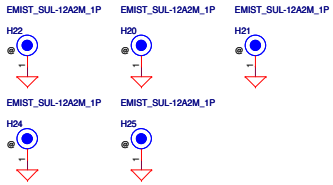



Hank0225: Note, PCB footprint is different from TVWDF1004AD0_DFN9, but it's compatible.

## USB3.0 Shielding Clip

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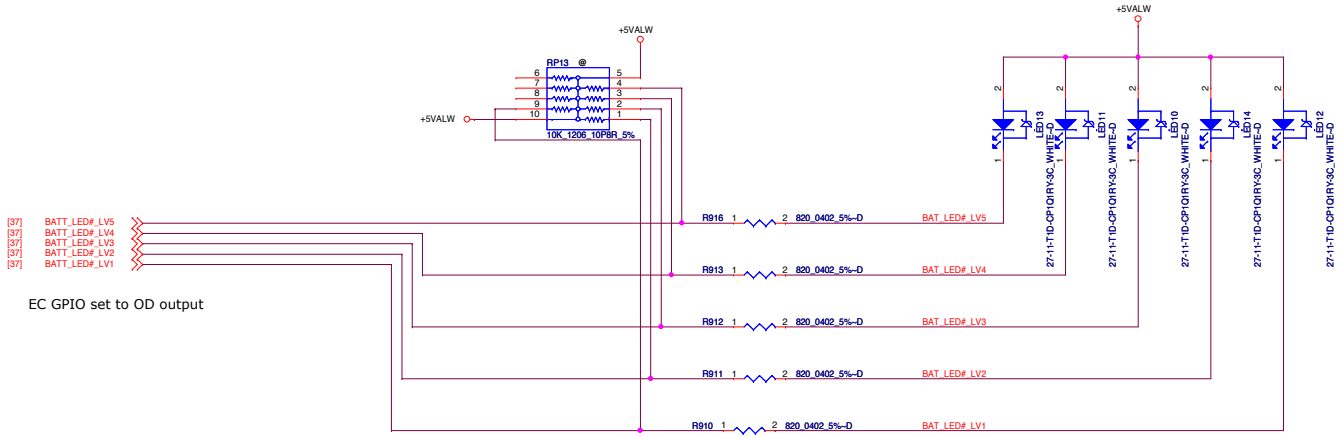
**Compal Electronics, Inc.**

Title: P27-USB 3.0 IO CONN

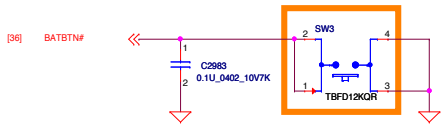
| Size | Document Number | Rev |
|---|---|---|
| | LA-B441P | 1.0 |

Date: Saturday, October 04, 2014 Sheet 30 of 50

## Battery Gauge LED




## Battery Gauge Button




R06_0825: Change P/N form SN100006P00(MISAKI) to SN100008F00 as MISAKI has been banned.

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | Compal Electronics, Inc. |
| Issued Date | 2013/07/04 | Deciphered Date | 2013/10/28 |
| Title | P28-BAT LED | | |
| Size | Document Number | | Rev |
| | LA-B441P | | 1.0 |
| Date: | Saturday, October 04, 2014 | Sheet | 31 of 50 |

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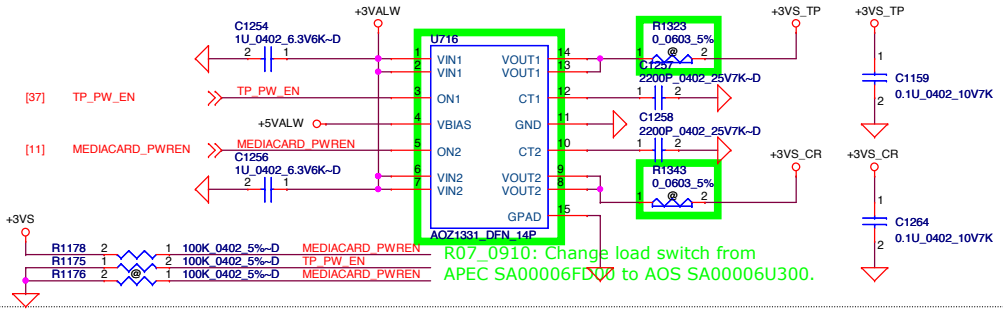
## Touch Pad, Card Reader Load Switch

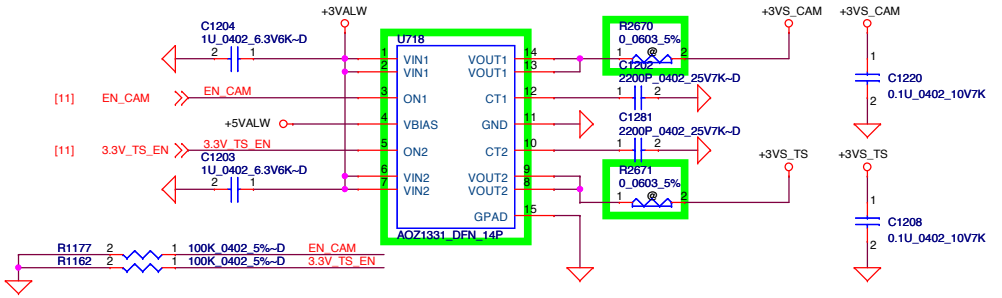
A00_1004: Change to short pad.



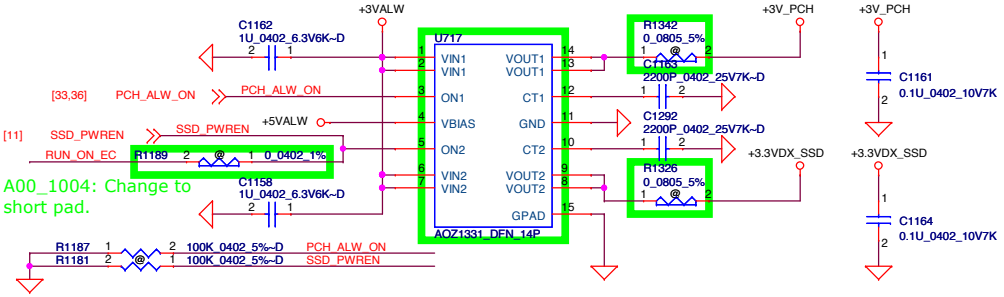

R07_0910: Change load switch from APEC SA00006FD00 to AOS SA00006U300.

## Camera, Touch Screen Load Switch

A00_1004: Change to short pad.

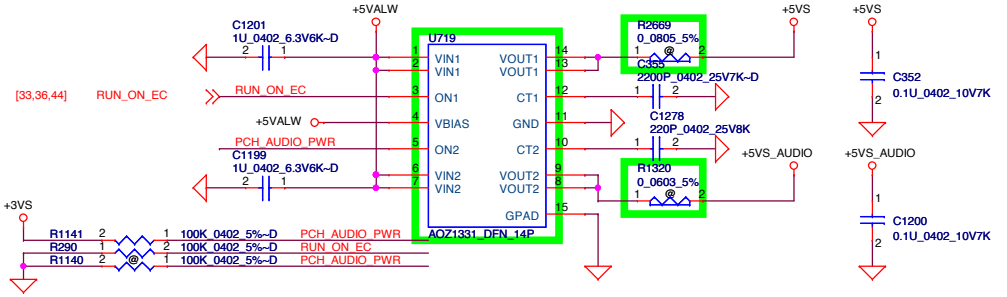



## Deeper Sleep, SSD Load Switch

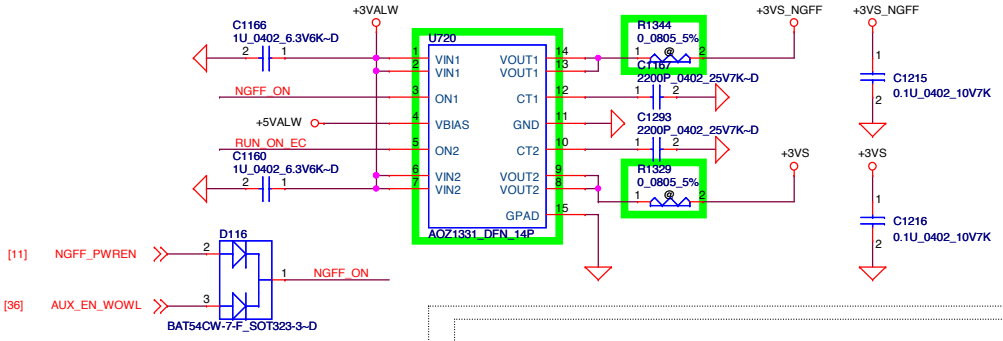



A00_1004: Change to short pad.

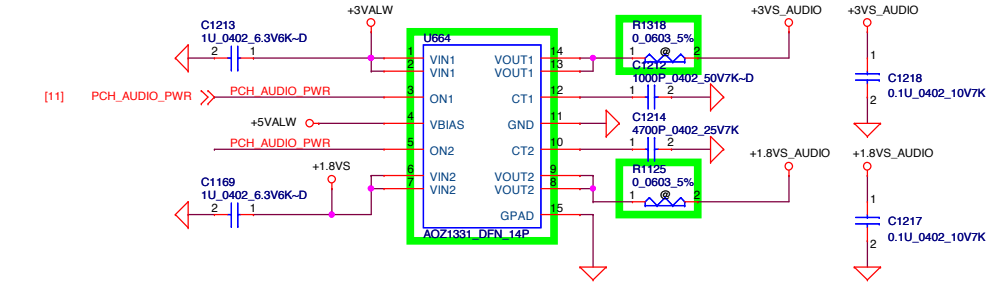
## 5V_Run, 5V_Audio Load Switch



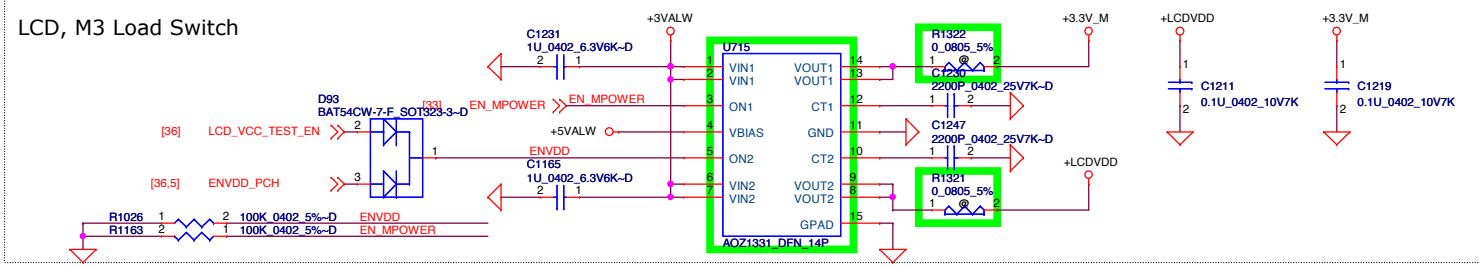

## WiFi, 3V_RUN Load Switch




## 3V_Audio, 1.8V_Audio Load Switch




## LCD, M3 Load Switch




| Security Classification | Compal Secret Data | | |
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| Issued Date | 2013/07/04 | Deciphered Date | 2013/10/28 |

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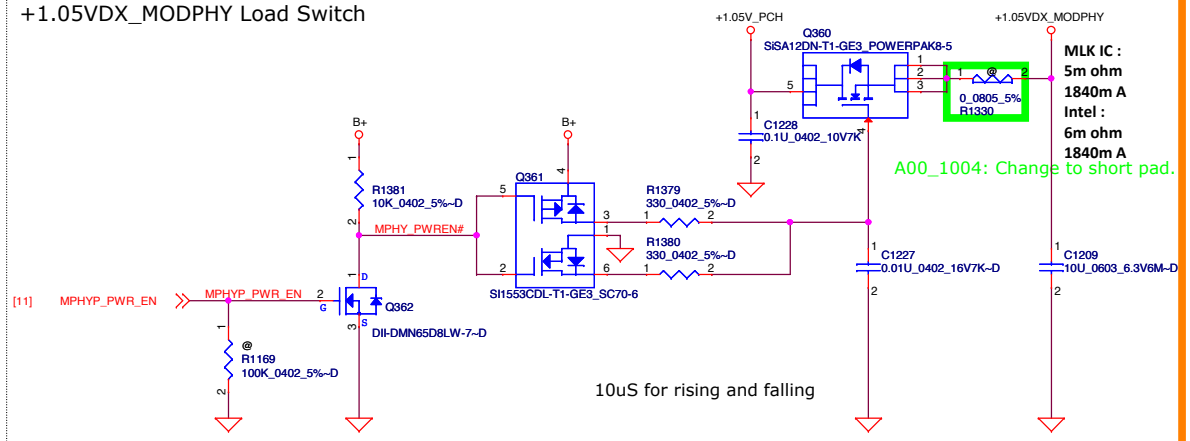
Compal Electronics, Inc.

Title: P29-DC/DC Interface

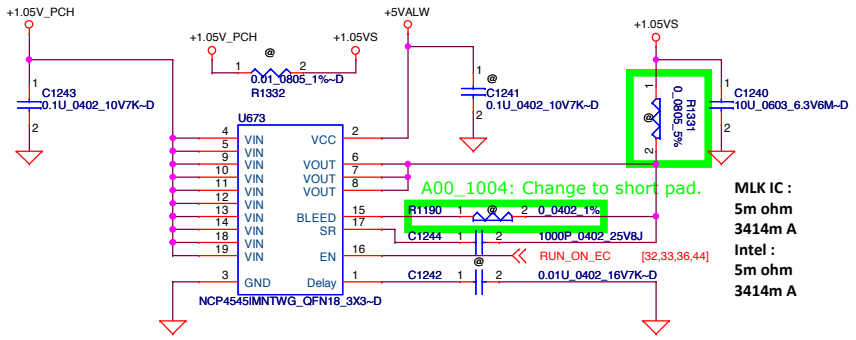
Size | Document Number: LA-B441P | Rev: 1.0

Date: Monday, October 06, 2014 | Sheet 32 of 50

## +1.05VDX_MODPHY Load Switch

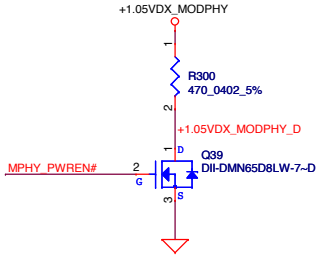


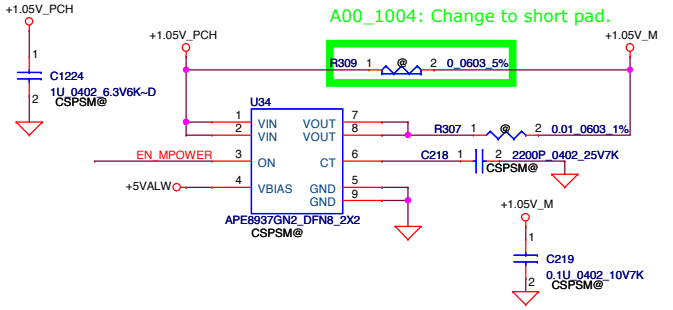

## vPro Load Switch



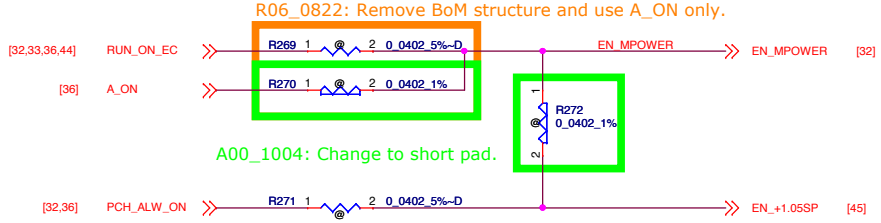

R06_1004: Remove BoM structure, both VPRO/Non-VPRO populated.

## Discharge




R06_0822: Remove BoM structure and use A_ON only.




| | | | |
|---|---|---|---|
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| Issued Date | 2013/07/04 | Deciphered Date | 2013/10/28 |

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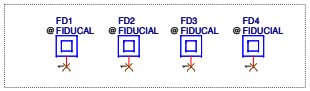
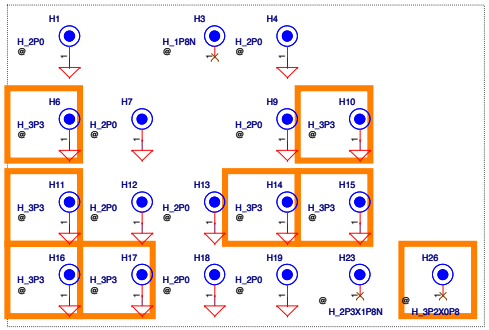
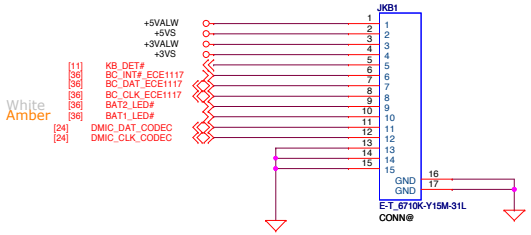
| | | | |
|---|---|---|---|
| Title | P29-DC/DC Interface | | |
| Size | Document Number | | Rev |
| | LA-B441P | | 1.0 |
| Date: | Monday, October 06, 2014 | Sheet | 33 of 50 |

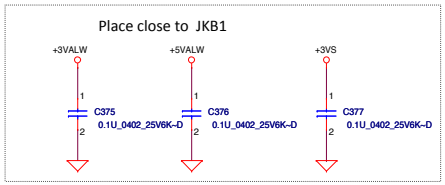



R06_0822: Stand off screw hole change form 3.2mm to 3.3 mm.
R06_0826: Add H26 for SSD bracket.

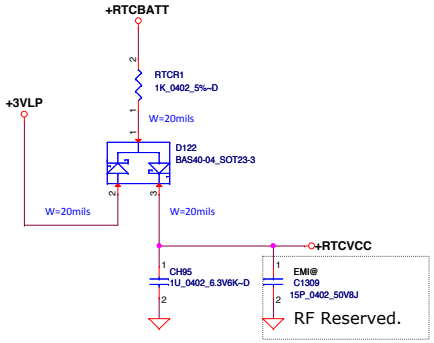
# Keyboard Controller board + DMIC

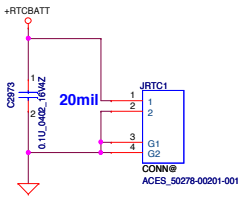


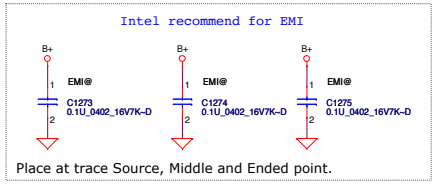




## RTC Battery With Charge Function

*RTC Battery Conn*

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| Security Classification | Compal Secret Data | | |
| Issued Date | 2013/07/04 | Deciphered Date | 2013/10/28 |

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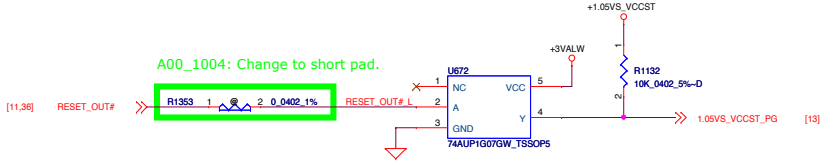
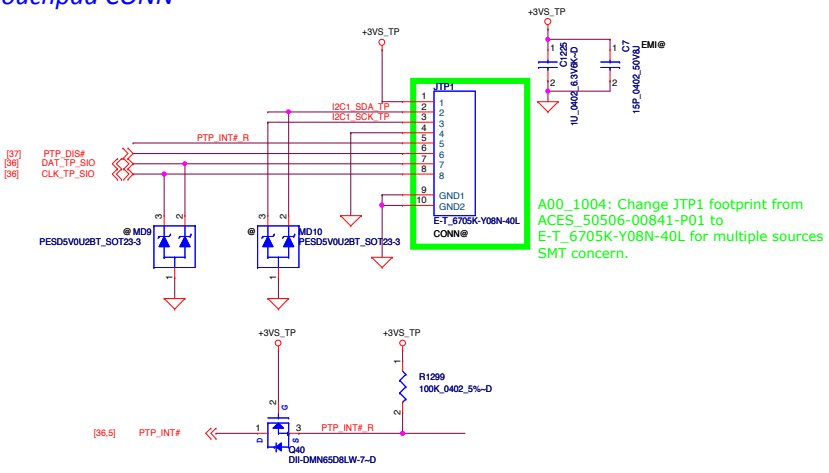
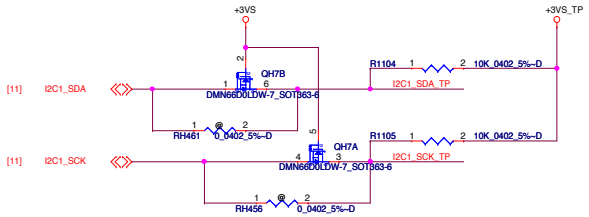
| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title | P30-SCREWH/KB/RTC | | |
| Size | Document Number | | Rev |
| | LA-B441P | | 1.0 |
| Date: | Saturday, October 04, 2014 | Sheet | 34 of 50 |




## Touchpad CONN




A00_1004: Change JTP1 footprint from ACES_50506-00841-P01 to E-T_6705K-Y08N-40L for multiple sources SMT concern.




| | | | |
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| Security Classification | Compal Secret Data | | |
| Issued Date | 2013/07/04 | Deciphered Date | 2013/10/28 |

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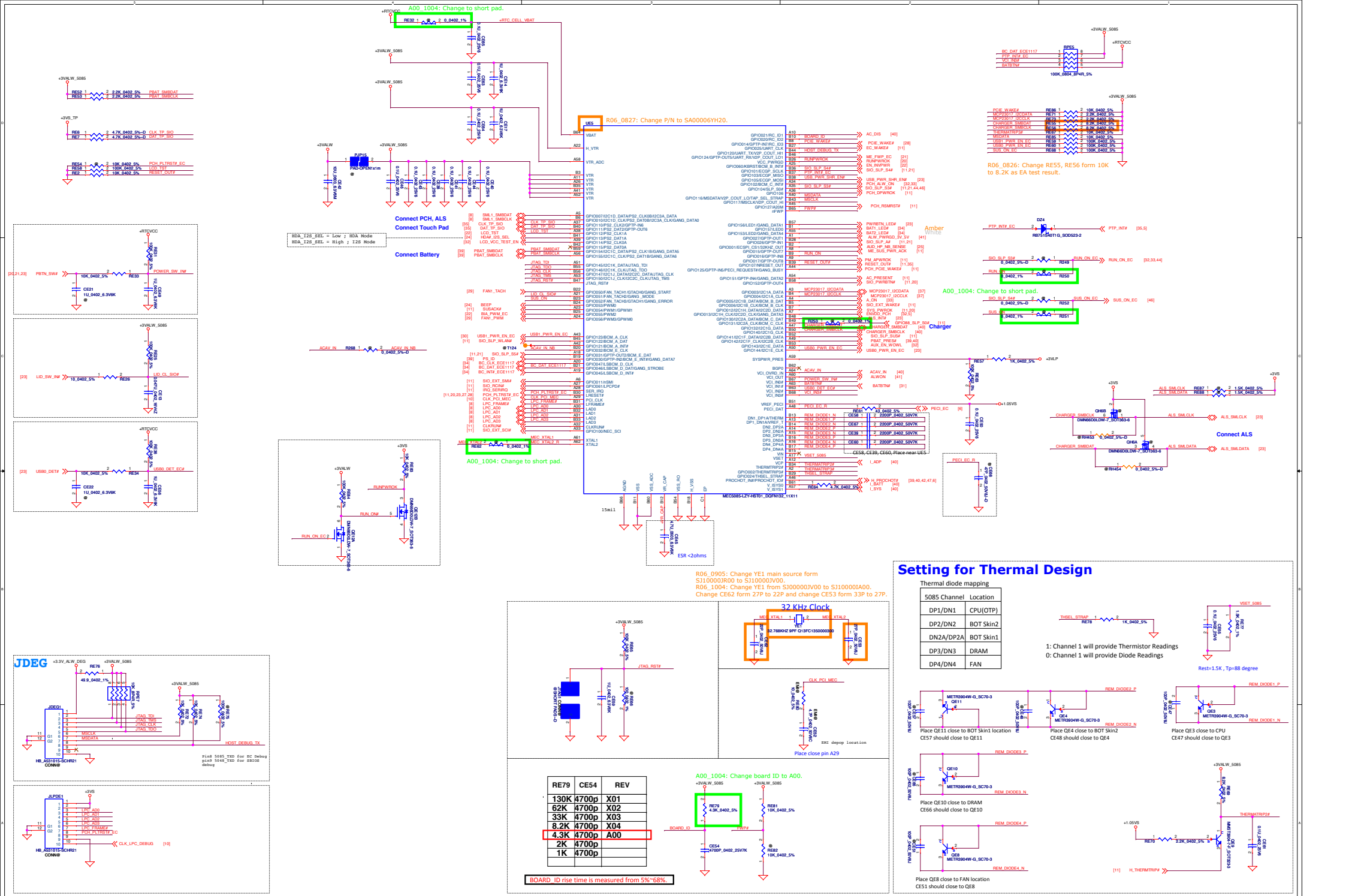
**Compal Electronics, Inc.**

Title: **P31-TP/PWERGD/LID**

| Size | Document Number | Rev |
|---|---|---|
| | LA-B441P | 1.0 |

Date: Sunday, October 05, 2014 | Sheet 35 of 50




| RE79 | CE54 | REV |
|---|---|---|
| 130K | 4700p | X01 |
| 62K | 4700p | X02 |
| 33K | 4700p | X03 |
| 8.2K | 4700p | X04 |
| 4.3K | 4700p | A00 |
| 2K | 4700p | |
| 1K | 4700p | |

## Setting for Thermal Design

Thermal diode mapping

| 5085 Channel | Location |
|---|---|
| DP1/DN1 | CPU(OTP) |
| DP2/DN2 | BOT Skin2 |
| DN2A/DP2A | BOT Skin1 |
| DP3/DN3 | DRAM |
| DP4/DN4 | FAN |

1: Channel 1 will provide Thermistor Readings
0: Channel 1 will provide Diode Readings

Rest=1.5K , Tp=88 degree

Place QE11 close to BOT Skin1 location
CE57 should close to QE11

Place QE4 close to BOT Skin2
CE48 should close to QE4

Place QE3 close to CPU
CE47 should close to QE3

Place QE10 close to DRAM
CE66 should close to QE10

Place QE8 close to FAN location
CE51 should close to QE8

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|---|---|---|---|
| Issued Date | 2013/07/04 | Deciphered Date | 2013/10/28 |

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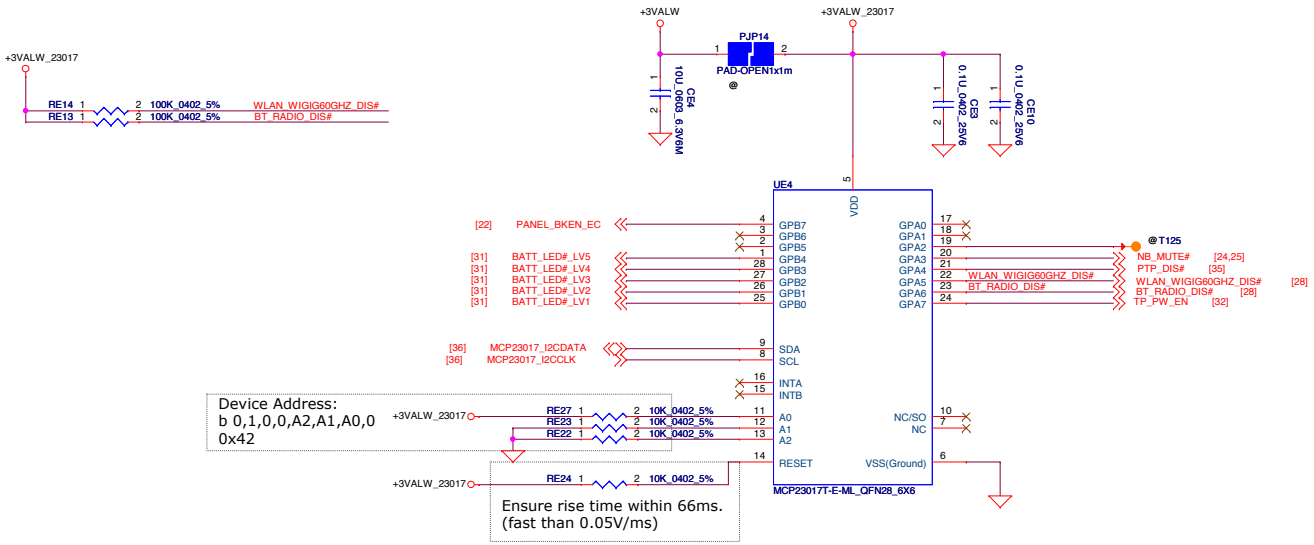
Title: P32-EC ENE-KB9012

Size: Document Number: LA-B441P

Rev: 1.0

Date: Sunday, October 05, 2014 Sheet 36 of 50

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| Issued Date | 2013/07/04 | Deciphered Date | 2013/10/28 |

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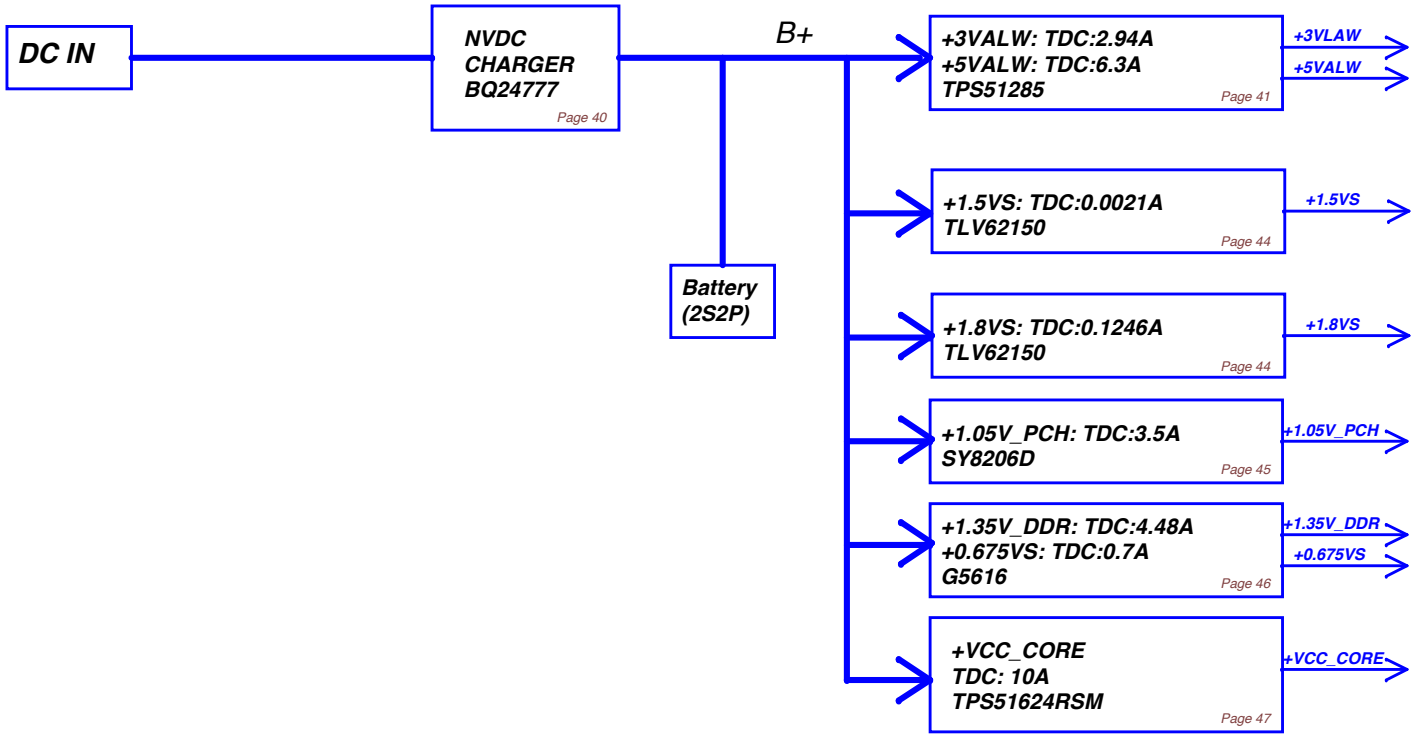
Compal Electronics, Inc.

Title: P32-MCP23017

Size: C | Document Number: LA-B441P | Rev: 1.0

Date: Saturday, October 04, 2014 | Sheet 37 of 50

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| Issued Date | 2011/06/02 | Deciphered Date | 2013/10/28 |

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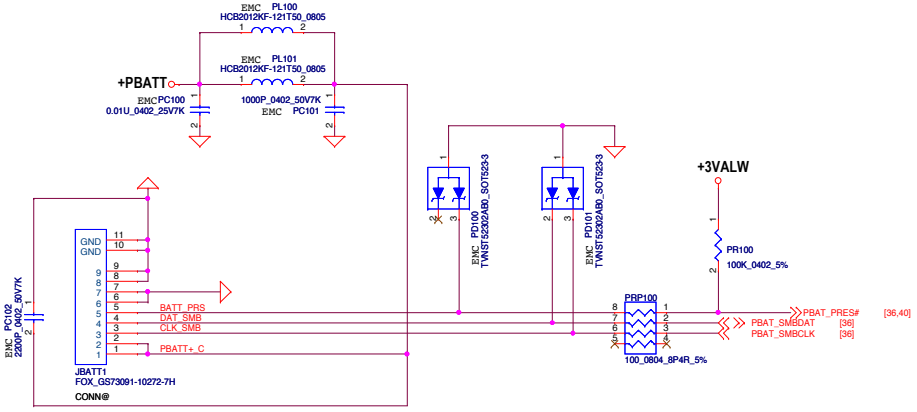
Compal Electronics, Inc.

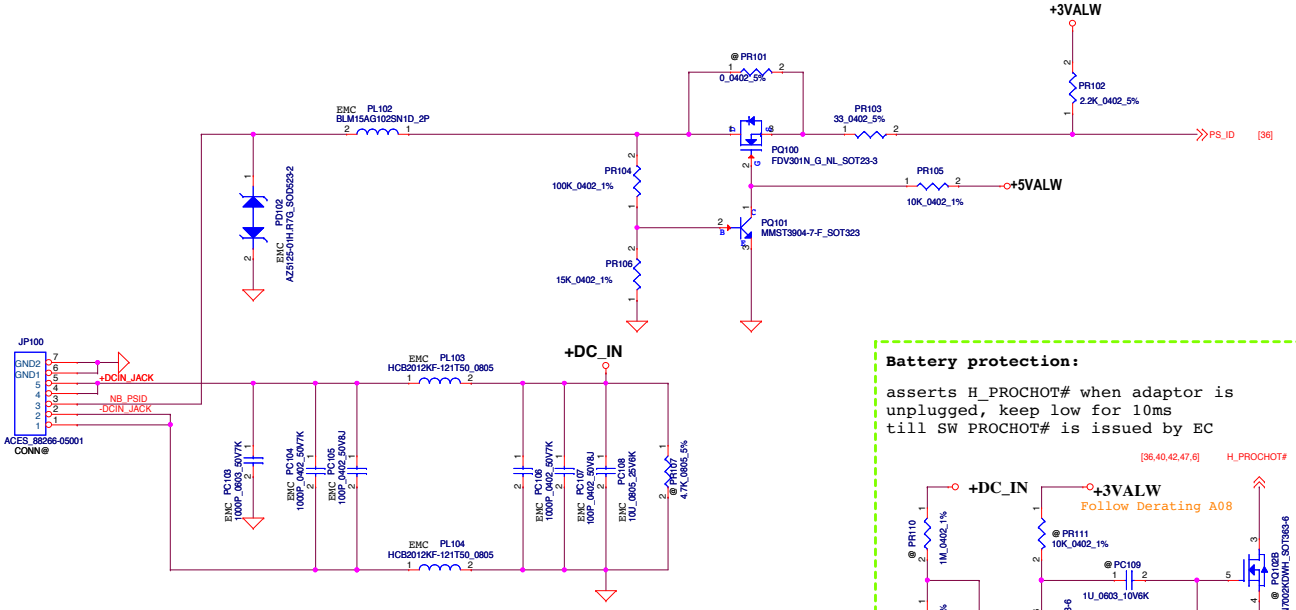
Title: P33-PWR_Block_Diagram

| Size | Document Number | Rev |
|---|---|---|
| | LA-9261P | 0.1 |

Date: Monday, October 06, 2014 Sheet 38 of 50

**PBATT1 connector**
**SMART**
**Battery:**
**1.BATT++**
**2.BATT++**
**3.CLK_SMB**
**4.DAT_SMB**
**5.BAT_PRS**
**6.SYS_PRES**
**7.BAT_ALERT**
**8.GND**
**9.GND**
**10.GND**
**11.GND**

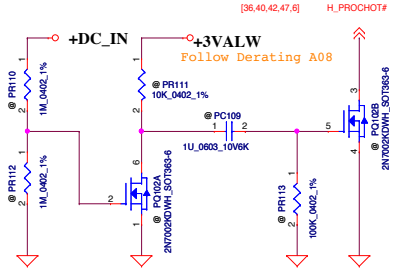


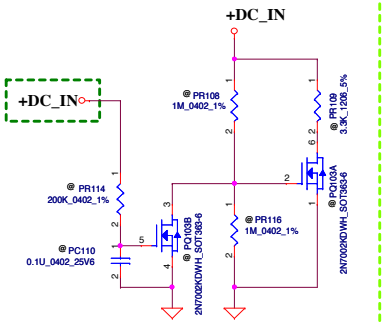

Other component(37.1)

**Battery protection:**

asserts H_PROCHOT# when adaptor is unplugged, keep low for 10ms till SW PROCHOT# is issued by EC




**Erp lot6 Circuit**

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|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2013/04/10 | Deciphered Date | 2014/05/01 |

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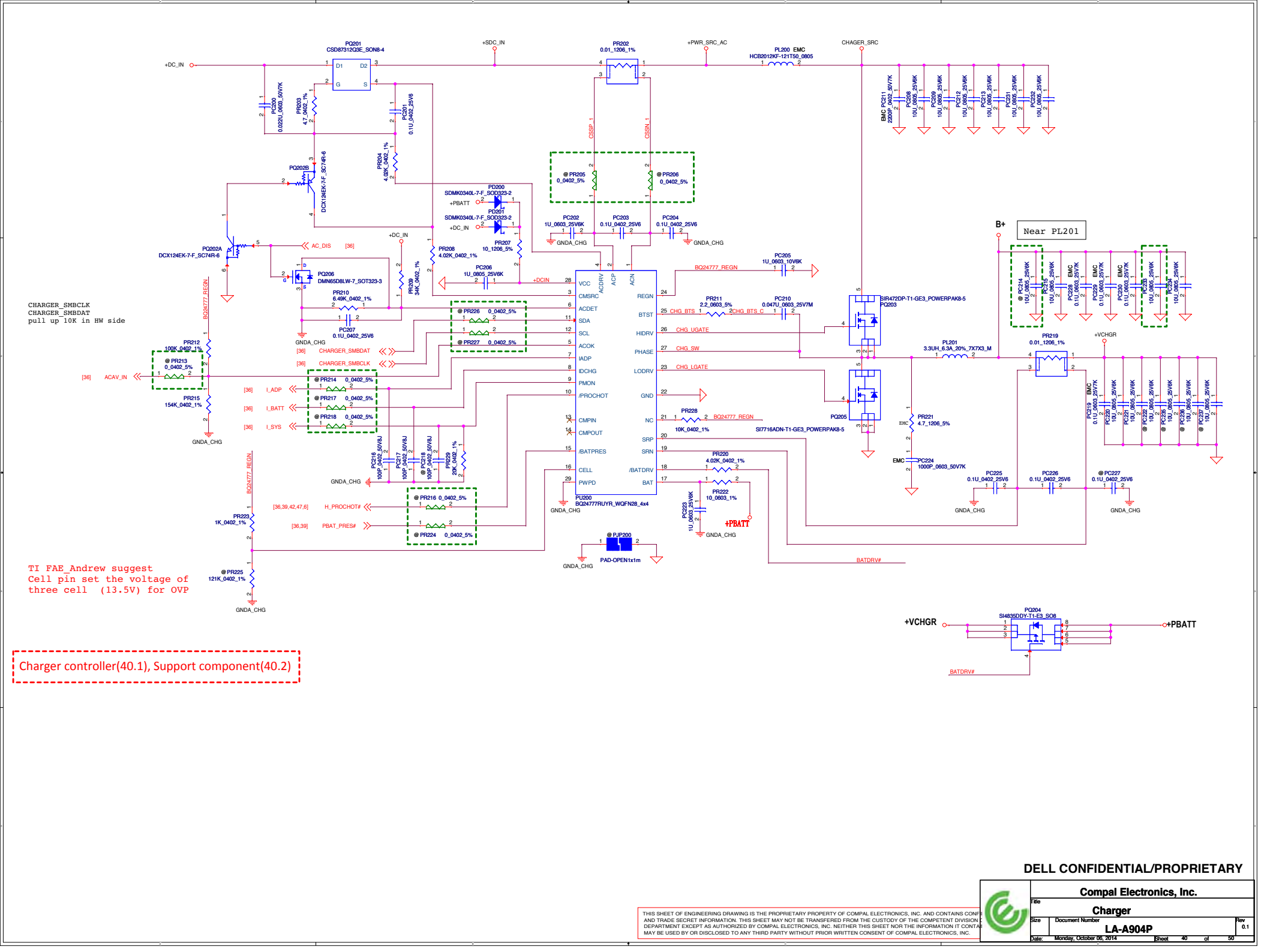
*Compal Electronics, Inc.*

Title: *PWR_DCIN/BATT CONN*

Size | Document Number: *LA-B072P* | Rev: 2.0

Date: Monday, October 06, 2014 | Sheet 39 of 50


CHARGER_SMBCLK
CHARGER_SMBDAT
pull up 10K in HW side
TI FAE_Andrew suggest
Cell pin set the voltage of
three cell (13.5V) for OVP
Charger controller(40.1), Support component(40.2)
Near PL201
+DC_IN
+SDC_IN
+PWR_SRC_AC
CHAGER_SRC
+PBATT
+VCHGR
BATDRV#
GNDA_CHG
PU200 BQ24777RUYR_WQFN28_4x4
PAD-OPEN1x1m
SI7716ADN-T1-GE3_POWERPAK8-5
SIR472DP-T1-GE3_POWERPAK8-5
SI4835DDY-T1-E3_SO8
DCX124EK-7-F_SC74R-6
DMN65D8LW-7_SOT323-3
SDMK0340L-7-F_SOD323-2
CSD87312Q3E_SON8-4
HCB2012KF-121T50_0805
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
Charger
LA-A904P
Rev 0.1
Monday, October 06, 2014
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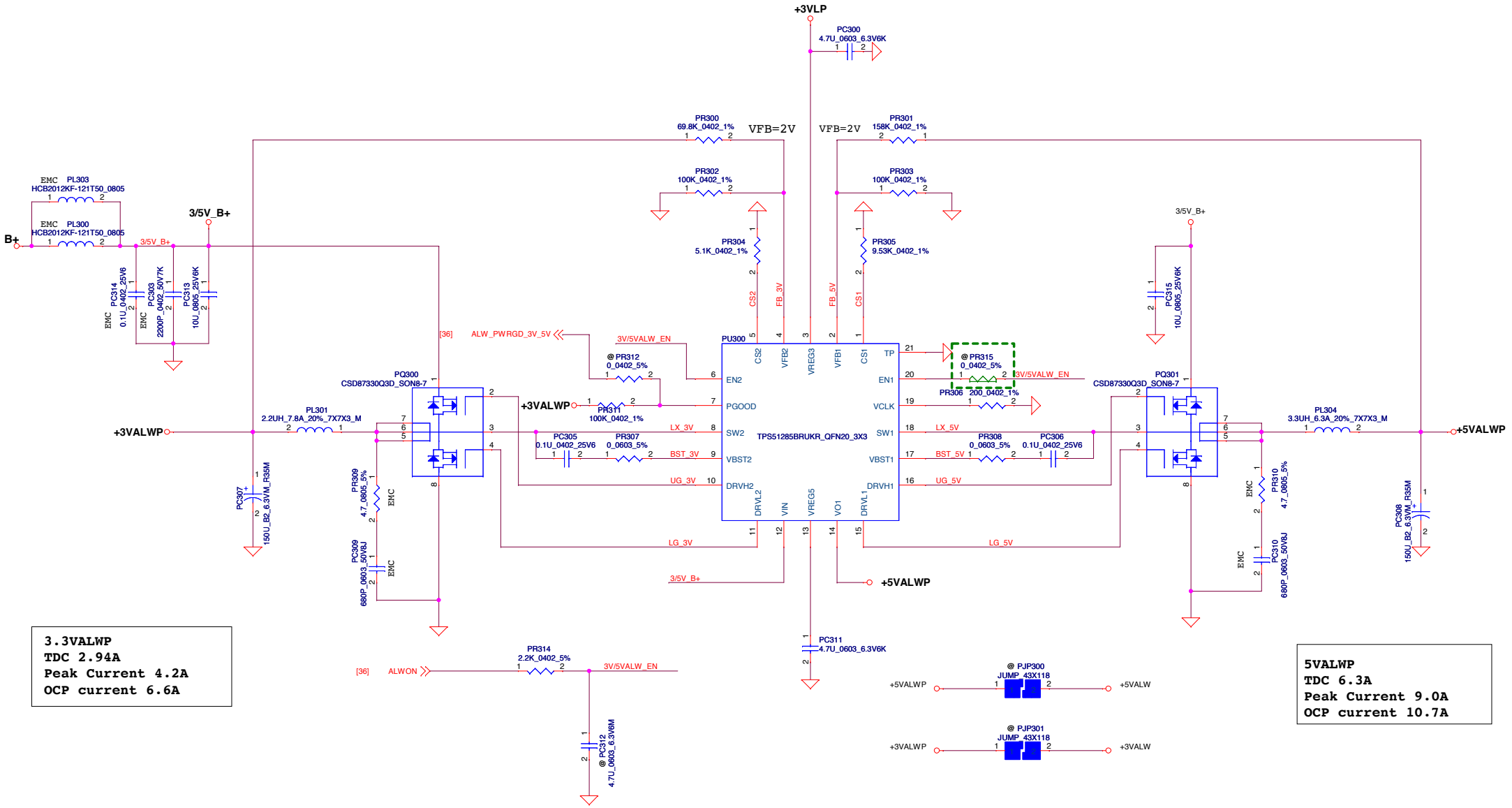


3.3VALWP
TDC 2.94A
Peak Current 4.2A
OCP current 6.6A

5VALWP
TDC 6.3A
Peak Current 9.0A
OCP current 10.7A

3V/5V controller(35.1), Support component(35.2)

| | | | |
|---|---|---|---|
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| Issued Date | 2011/06/02 | Deciphered Date | 2013/10/28 |

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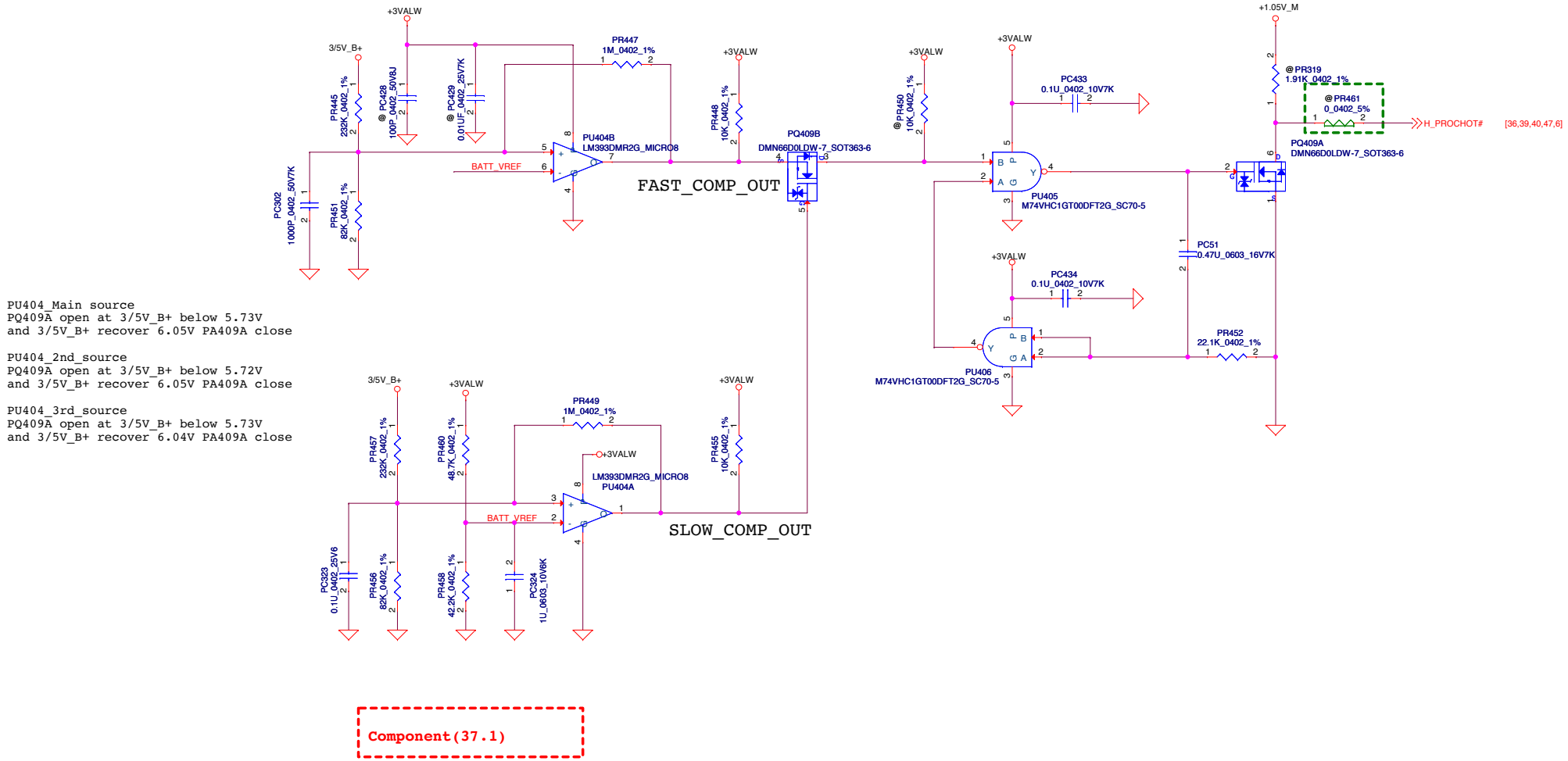
Compal Electronics, Inc.

Title: P36-PWR_+3.3/5V_VR

Size: | Document Number: LA-9261P | Rev: 0.1

Date: Monday, October 06, 2014 | Sheet 41 of 50




PU404_Main source
PQ409A open at 3/5V_B+ below 5.73V
and 3/5V_B+ recover 6.05V PA409A close

PU404_2nd_source
PQ409A open at 3/5V_B+ below 5.72V
and 3/5V_B+ recover 6.05V PA409A close

PU404_3rd_source
PQ409A open at 3/5V_B+ below 5.73V
and 3/5V_B+ recover 6.04V PA409A close

Component(37.1)

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/02 | Deciphered Date | 2013/10/28 |

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Compal Electronics, Inc.

Title: P37-Blank

Size | Document Number: LA-9261P | Rev: 0.1

Date: Monday, October 06, 2014 | Sheet 42 of 50

| | | | |
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| Issued Date | 2011/06/02 | Deciphered Date | 2013/10/28 |

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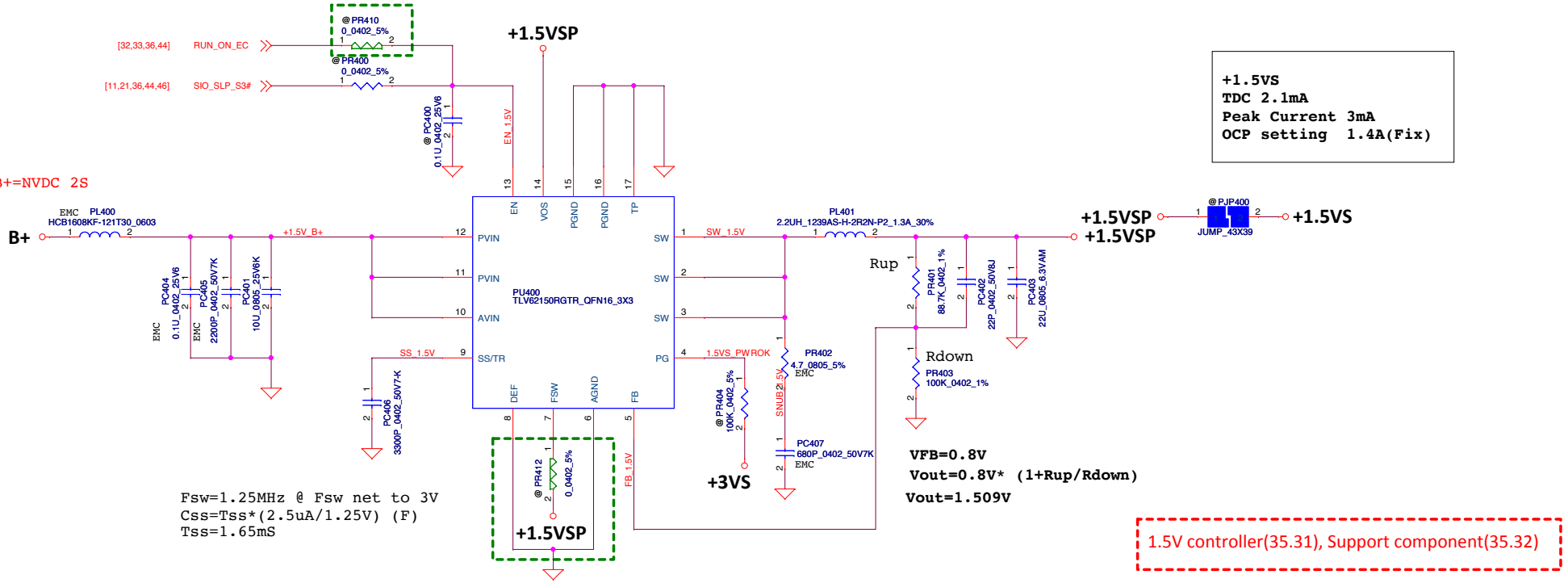
**Compal Electronics, Inc.**

Title: **P38-Blank**

Size | Document Number: **LA-9261P** | Rev: 0.1

Date: Monday, October 06, 2014 | Sheet 43 of 50




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/02 | Deciphered Date | 2013/10/28 |

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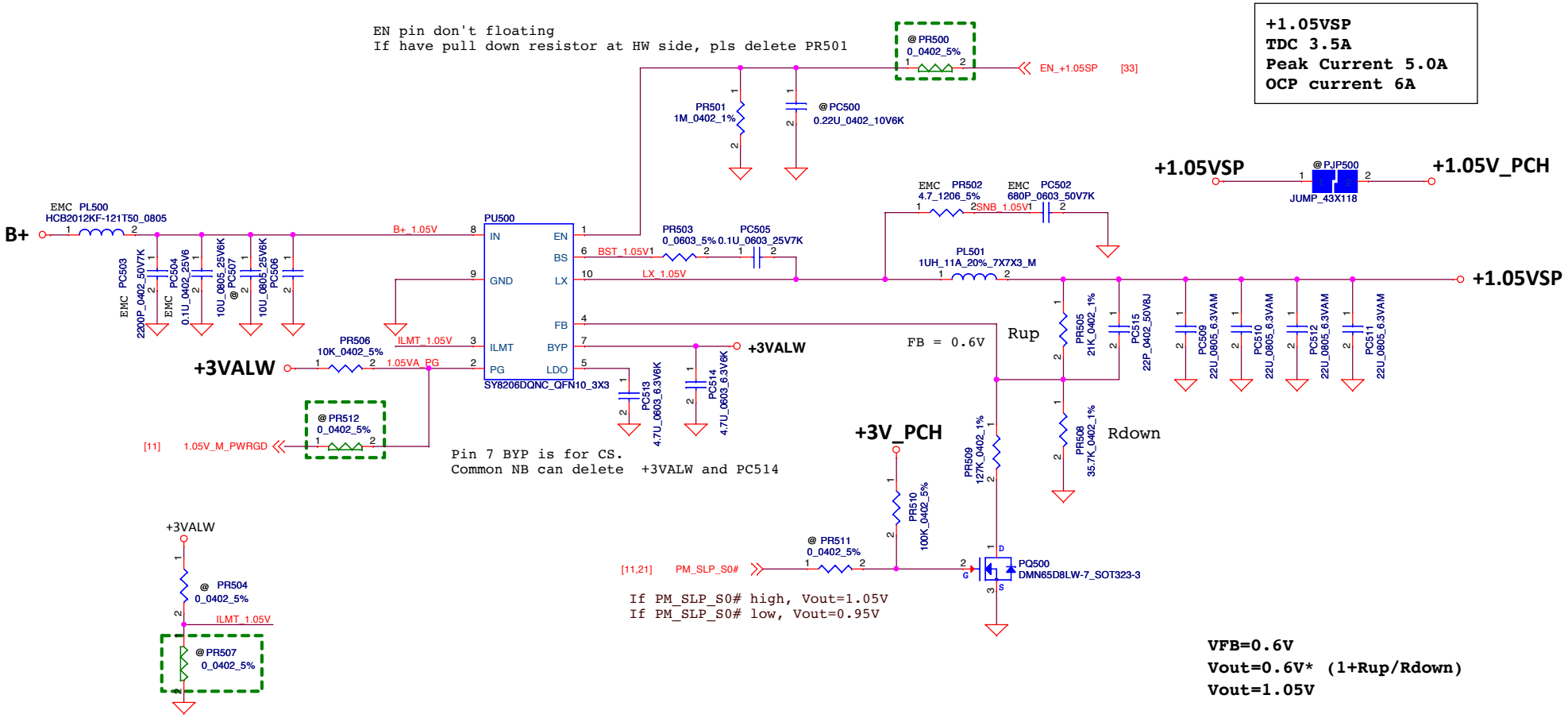
Compal Electronics, Inc.

Title: P39-PWR_+1.5VS/+1.8V_DDR

Size: | Document Number: LA-9261P | Rev: 0.1

Date: Monday, October 06, 2014 | Sheet 44 of 50




The current limit is set to 6A, 8A or 12A when this pin is pull low, floating or pull high

1.05V controller(35.5), Support component(35.6)

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/02 | Deciphered Date | 2013/10/28 |

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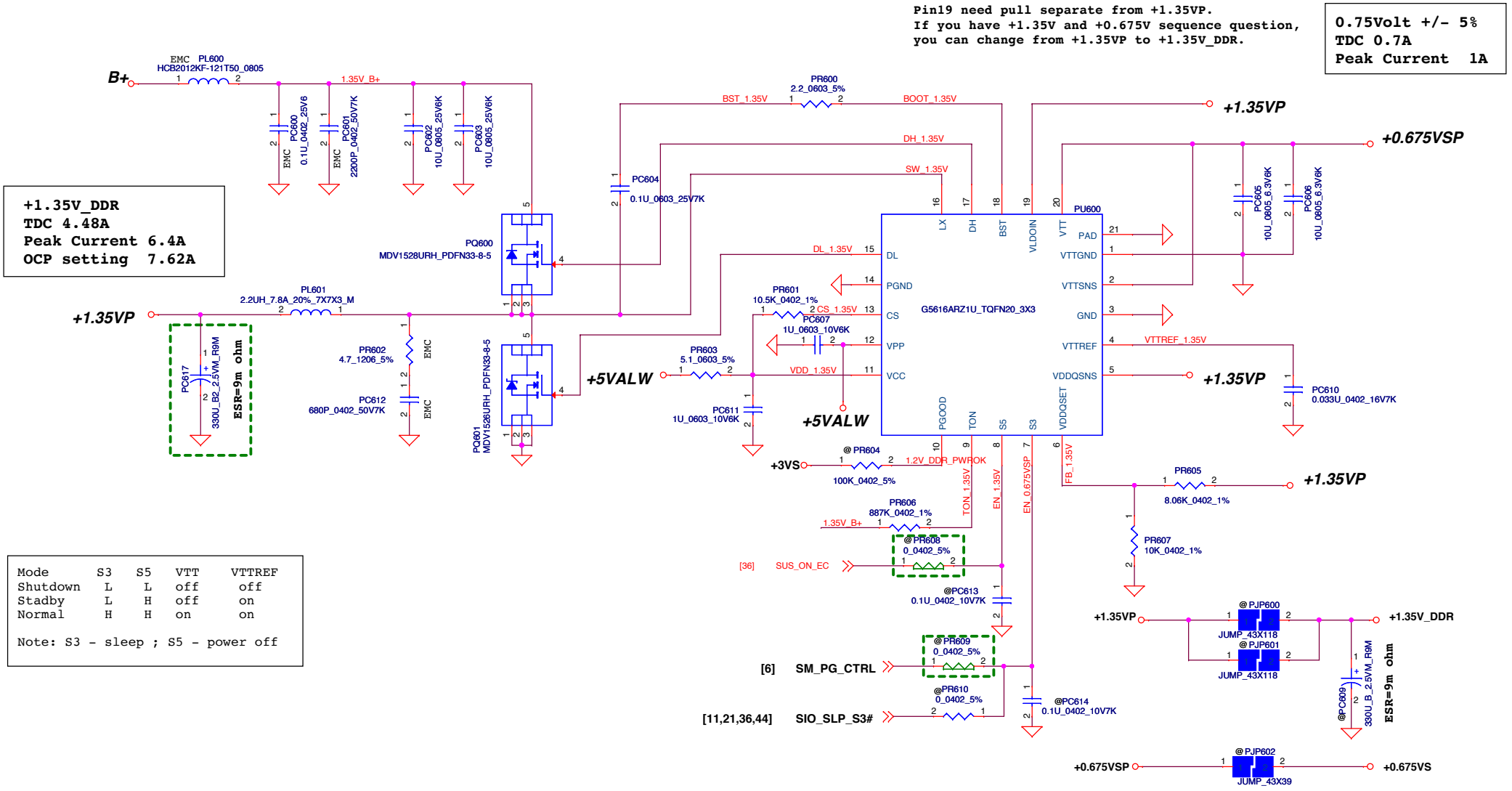
Compal Electronics, Inc.

Title: P40-PWR_+1.05VA

Size | Document Number: LA-9261P | Rev: 0.1

Date: Monday, October 06, 2014 | Sheet 45 of 50




| Mode | S3 | S5 | VTT | VTTREF |
|---|---|---|---|---|
| Shutdown | L | L | off | off |
| Stadby | L | H | off | on |
| Normal | H | H | on | on |

Note: S3 - sleep ; S5 - power off

DDR controller(35.3), Support component(35.4)

| | | | |
|---|---|---|---|
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Title: P41-PWR_+1.35V_DDR/+0.675VS

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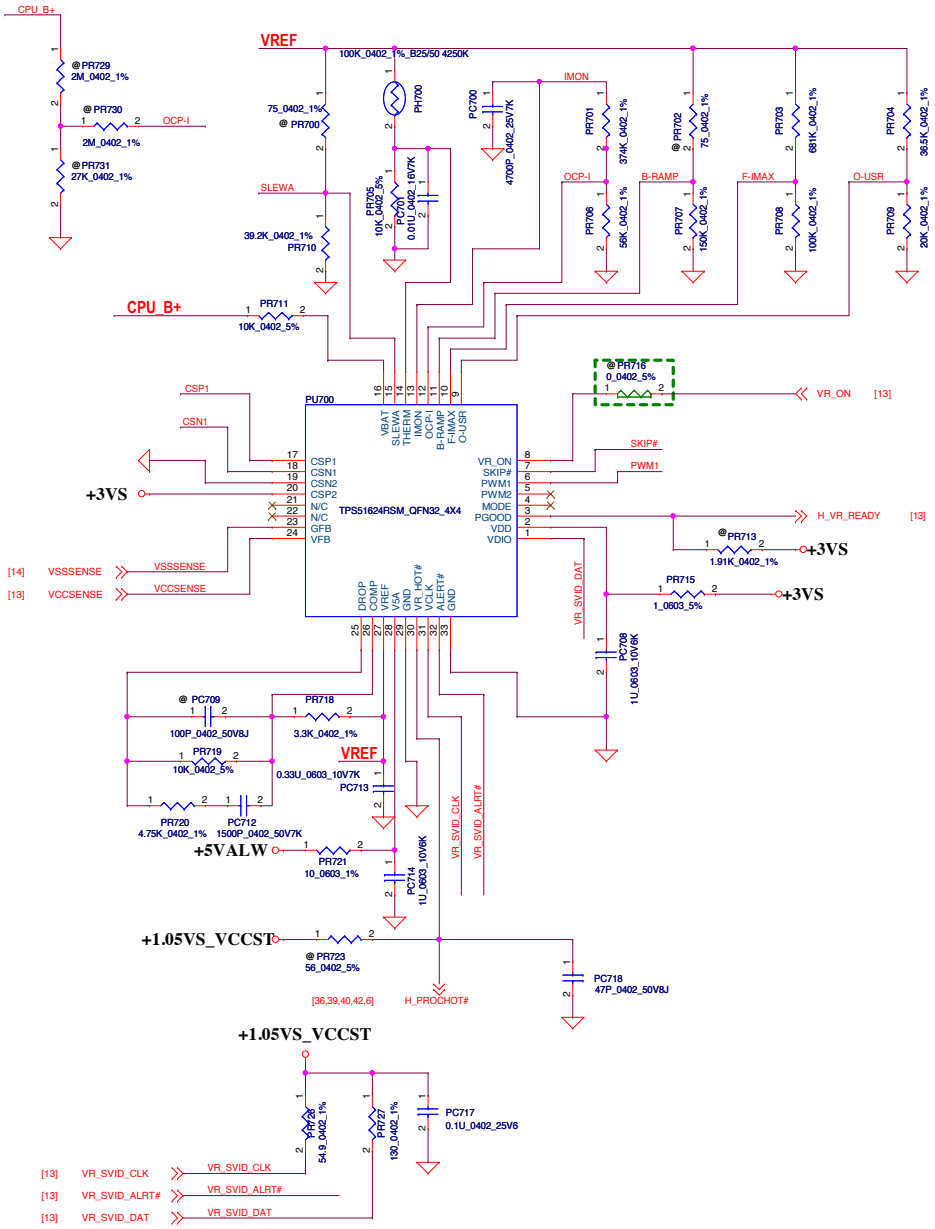
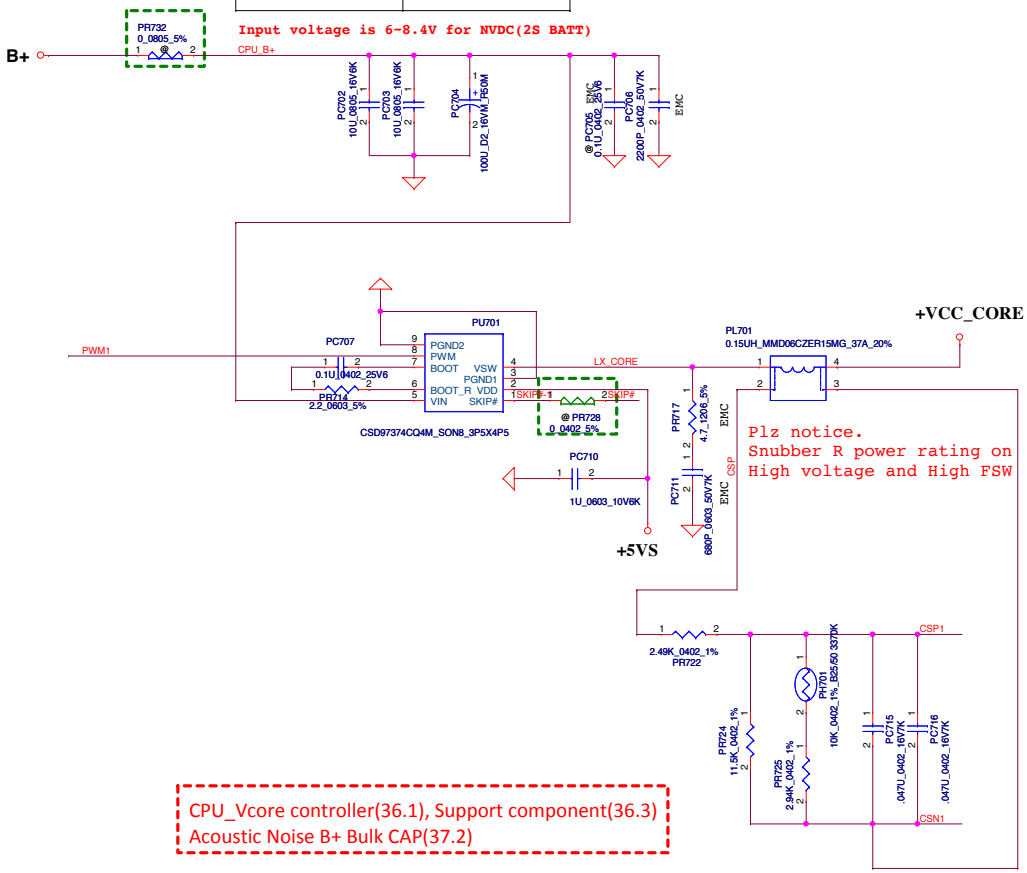
Follow Intel 514849_514849_BDW_PDG_Rev_1.0

| 15W | Specifications |
|---|---|
| Vps0 | 1.8V |
| Vboot | 1.7V |
| Icc_MAX | 32A |
| Idyn_MAX | 27A |
| Icc-TDC | 10A |
| Load-Line | 2.0mV/A |
| Fast Slew Rate | 48mV/us |

**CPU**
**Frequency = 1.2MHz**
**PL2 Current 14A**
**ICC MAX 32A**
**OCP Current 39 A**
**IC_Dyn_VID1 27A**
**DCR: 0.9mohm +-7%**
**PH700 100Kohm B value: 3370k 1%**
**PH701 10Kohm B value: 4250k 1%**




CPU_Vcore controller(36.1), Support component(36.3)
Acoustic Noise B+ Bulk CAP(37.2)

| | | | |
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Title: **P42-PWR_CPU_CORE**

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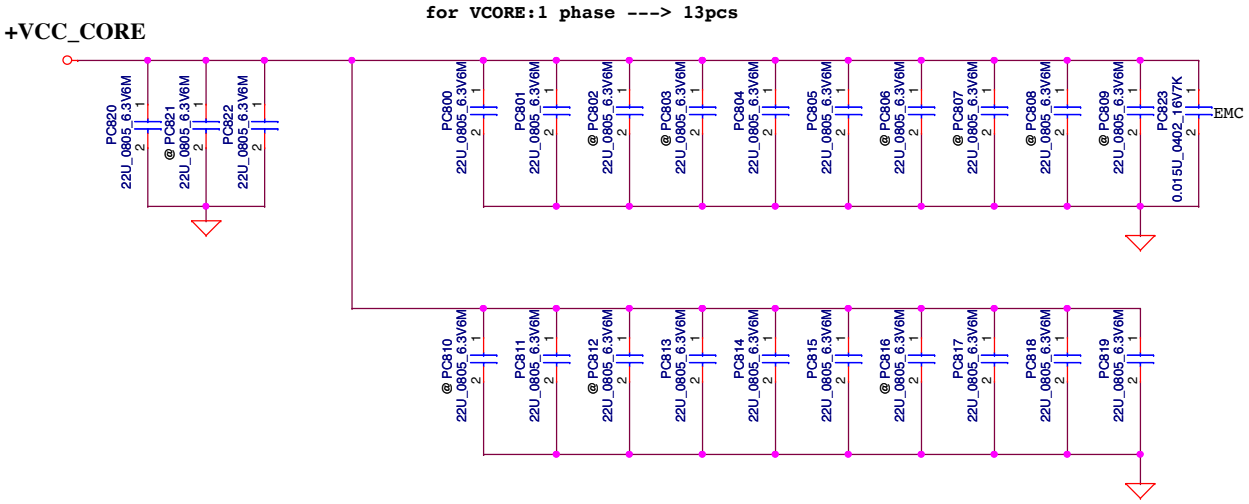
CPU_Core output CAP(36.4)

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Title: P43-PWR_PROCESSOR_DECOUPLING

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|---|---|---|---|---|---|---|---|
| 1 | P40 | PR205, PR206, PR213, PR214, PR216, PR217, PR218, PR224, PR226, PR227, | 2014'10/06 | Compal_Henry | modify schematic for A00 garber | Change 0 ohm to short pad | |
| 2 | P41 | PR315 | 2014'10/06 | Compal_Henry | modify schematic for A00 garber | Change 0 ohm to short pad | |
| 3 | P42 | PR416 | 2014'10/06 | Compal_Henry | modify schematic for A00 garber | Change 0 ohm to short pad | |
| 4 | P44 | PR410, PR411, PR412, PR413, | 2014'10/06 | Compal_Henry | modify schematic for A00 garber | Change 0 ohm to short pad | |
| 5 | P45 | PR500, PR507, PR512 | 2014'10/06 | Compal_Henry | modify schematic for A00 garber | Change 0 ohm to short pad | |
| 6 | P46 | PR608, PR609 | 2014'10/06 | Compal_Henry | modify schematic for A00 garber | Change 0 ohm to short pad | |
| 7 | P47 | PR716, PR718, PR732 | 2014'10/06 | Compal_Henry | modify schematic for A00 garber | Change 0 ohm to short pad | |

| | | | |
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