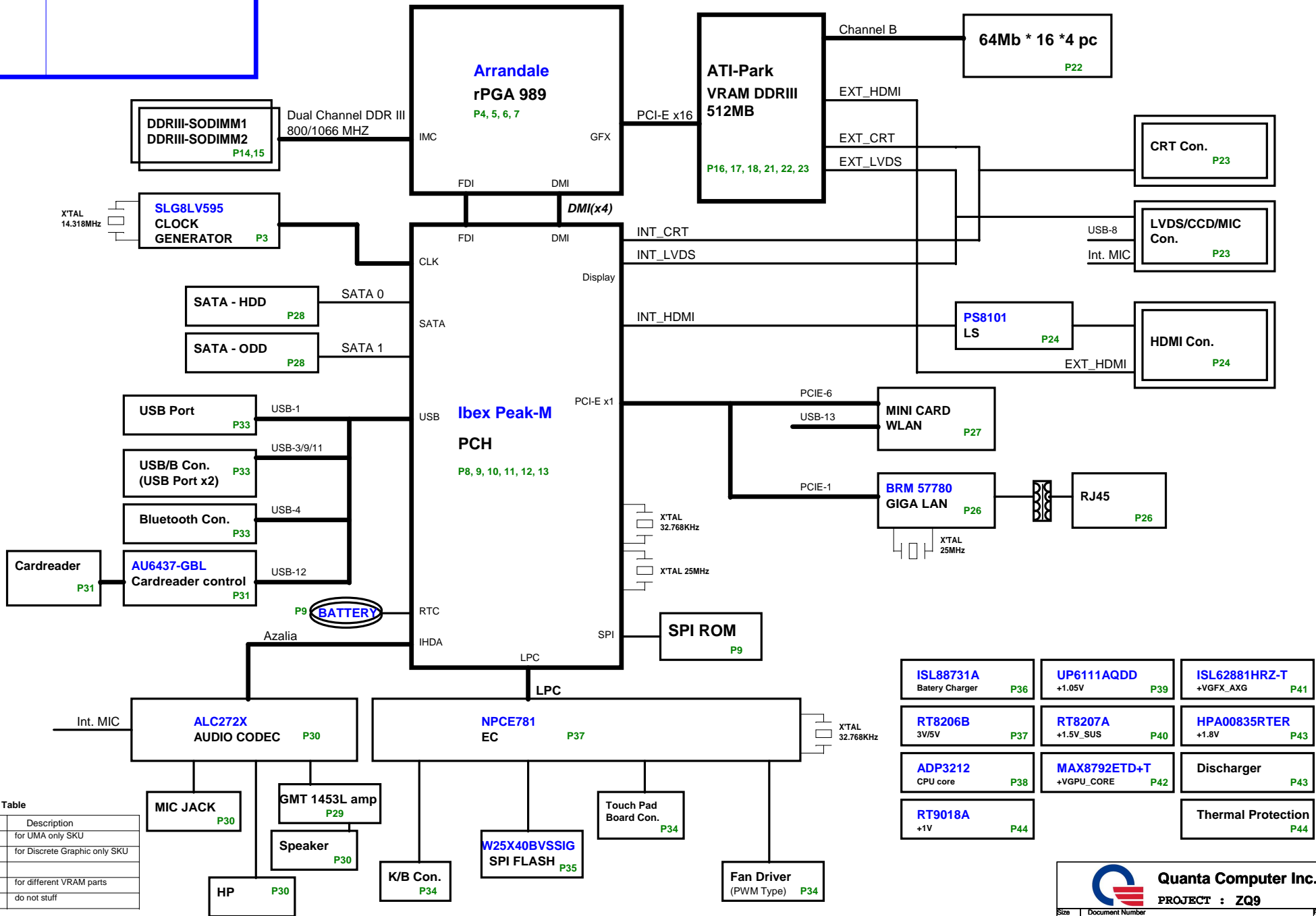


VER : 1A

ZQ9 SYSTEM BLOCK DIAGRAM

BOM P/N	Description

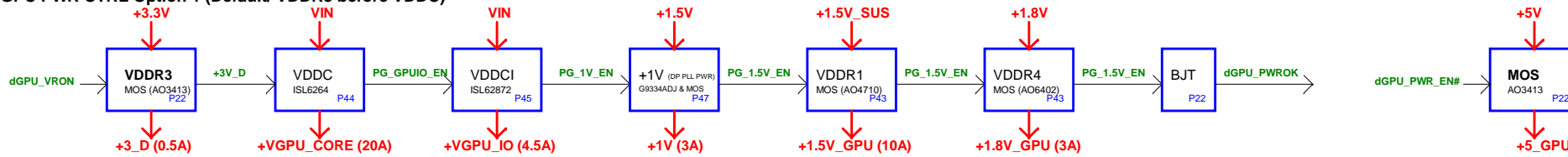


BOM Option Table

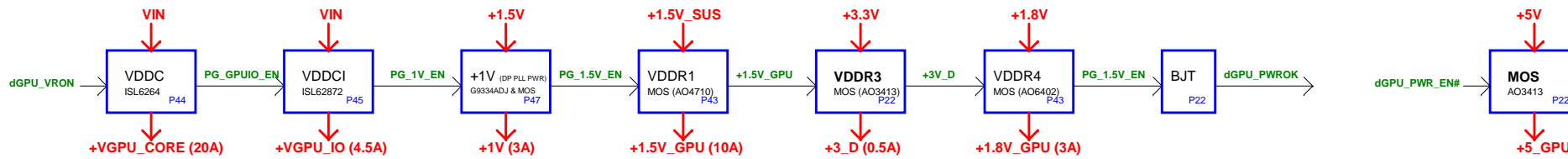
Reference	Description
IV@	for UMA only SKU
EV@	for Discrete Graphic only SKU
VRAM@	for different VRAM parts
*	do not stuff

Quanta Computer Inc.
PROJECT : ZQ9
Block Diagram
 Date: Tuesday, June 22, 2010 Sheet 1 of 45 Rev 1A

GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



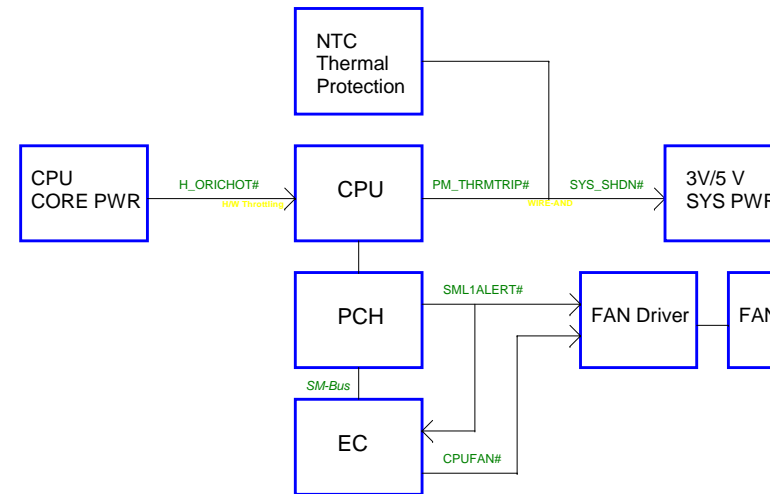
GPU PWR CTRL Option 2 (VDDR3 after VDDR1)

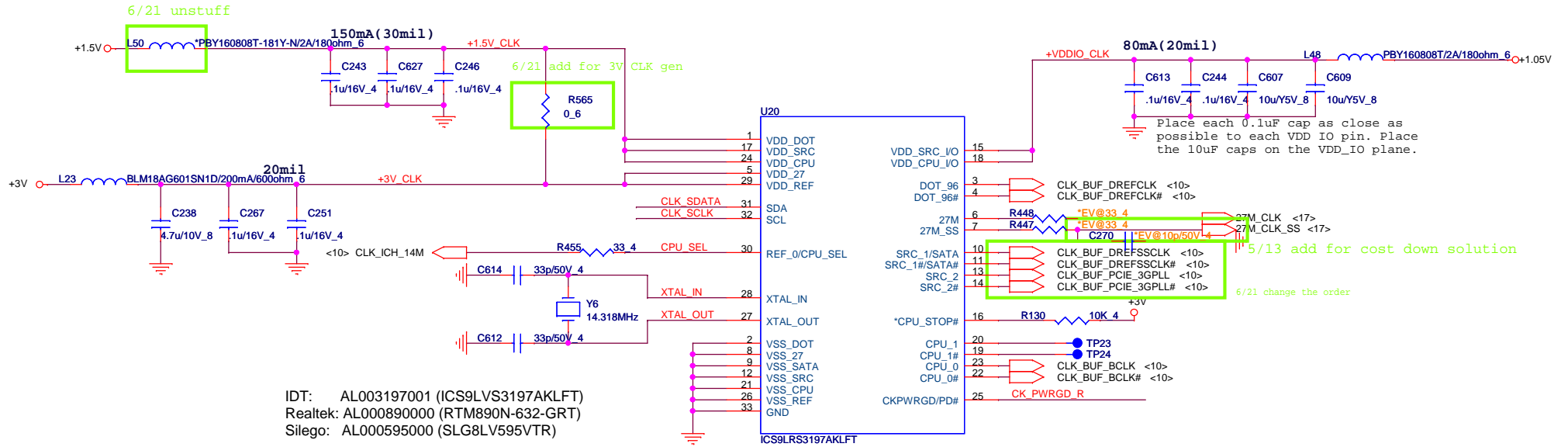


Power States

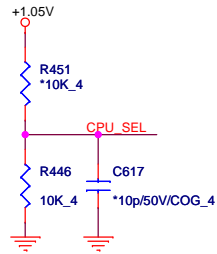
POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+5V_GPU	+5V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN#	Discrete enable
+GPU_CORE	+0.9V~+1.1V	GPU CORE POWER	+3V_D	Discrete enable
+GPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIO_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable
+1V	+1V	DP/PEG POWER	PG_1V_EN	Discrete enable

Thermal Follow Chart



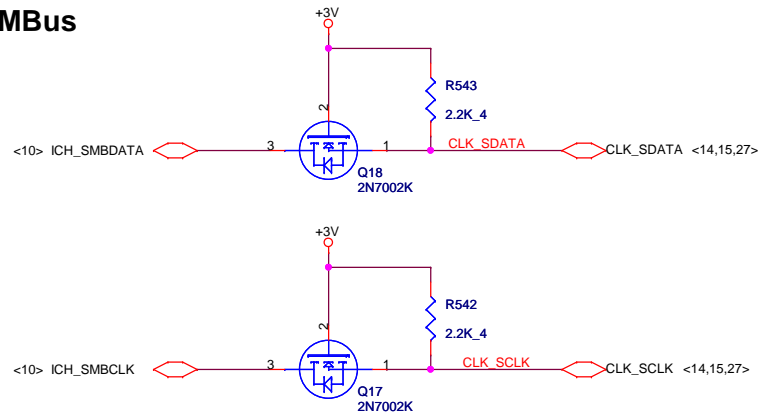


CPU_CLK select

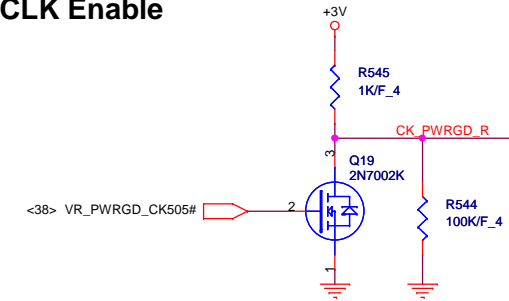



	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

SMBus



CLK Enable

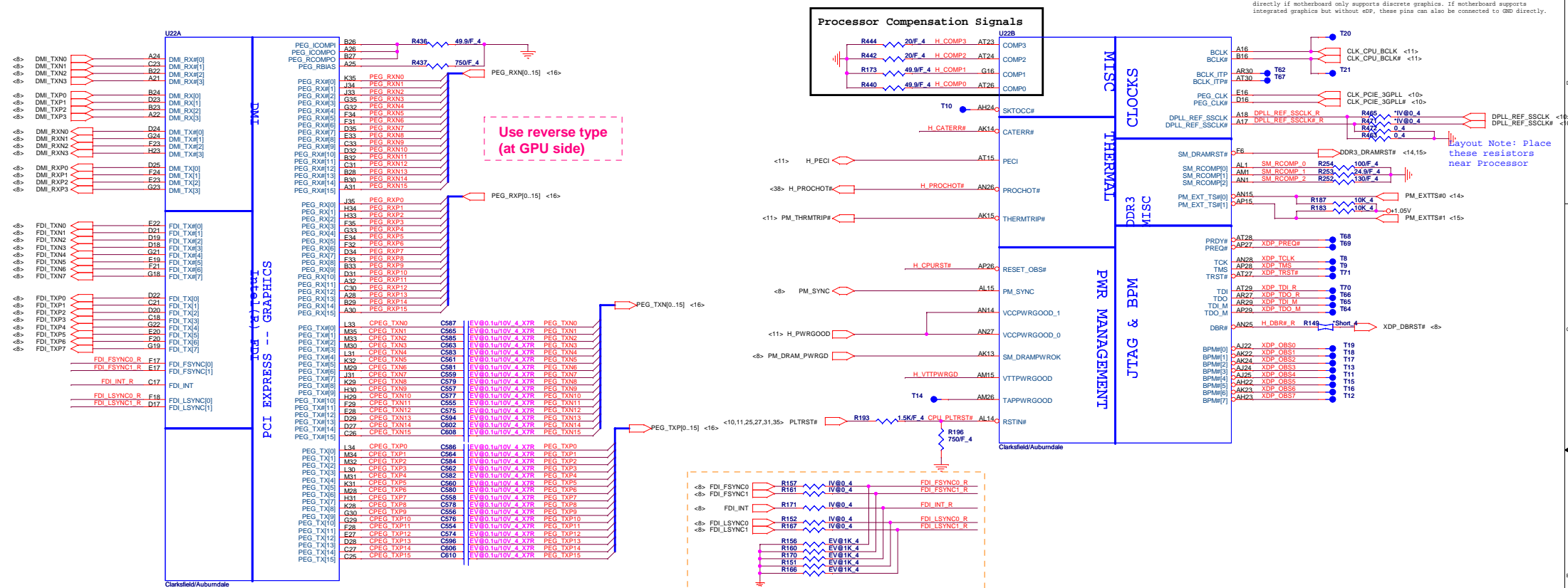




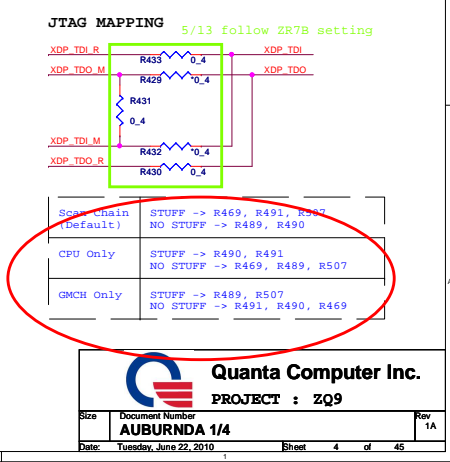
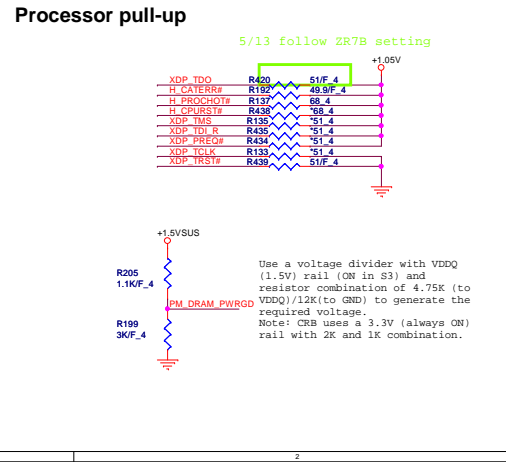
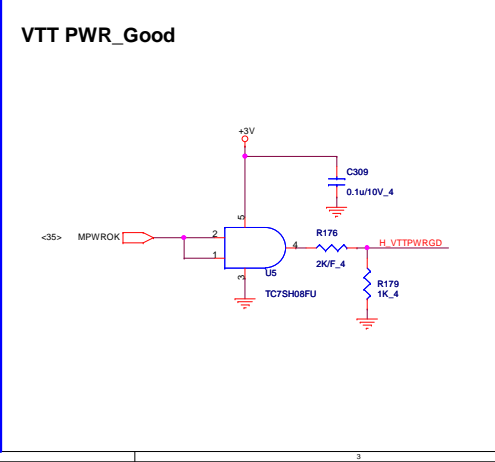
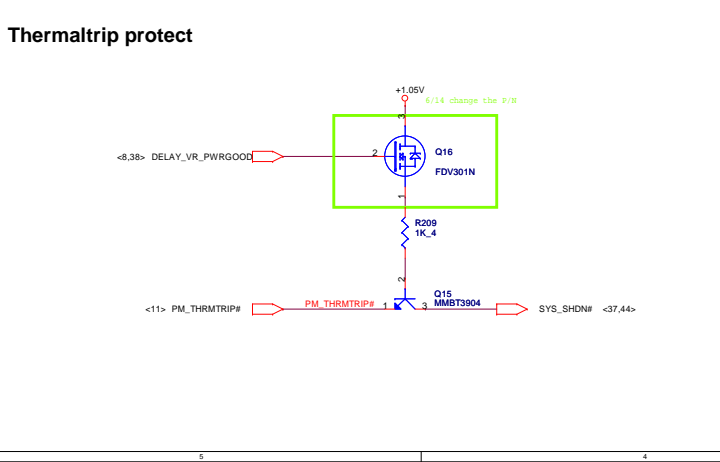
Quanta Computer Inc.
PROJECT : ZQ9

Size	Document Number	Rev
	Clock Generator	1A
Date:	Tuesday, June 22, 2010	Sheet 3 of 45

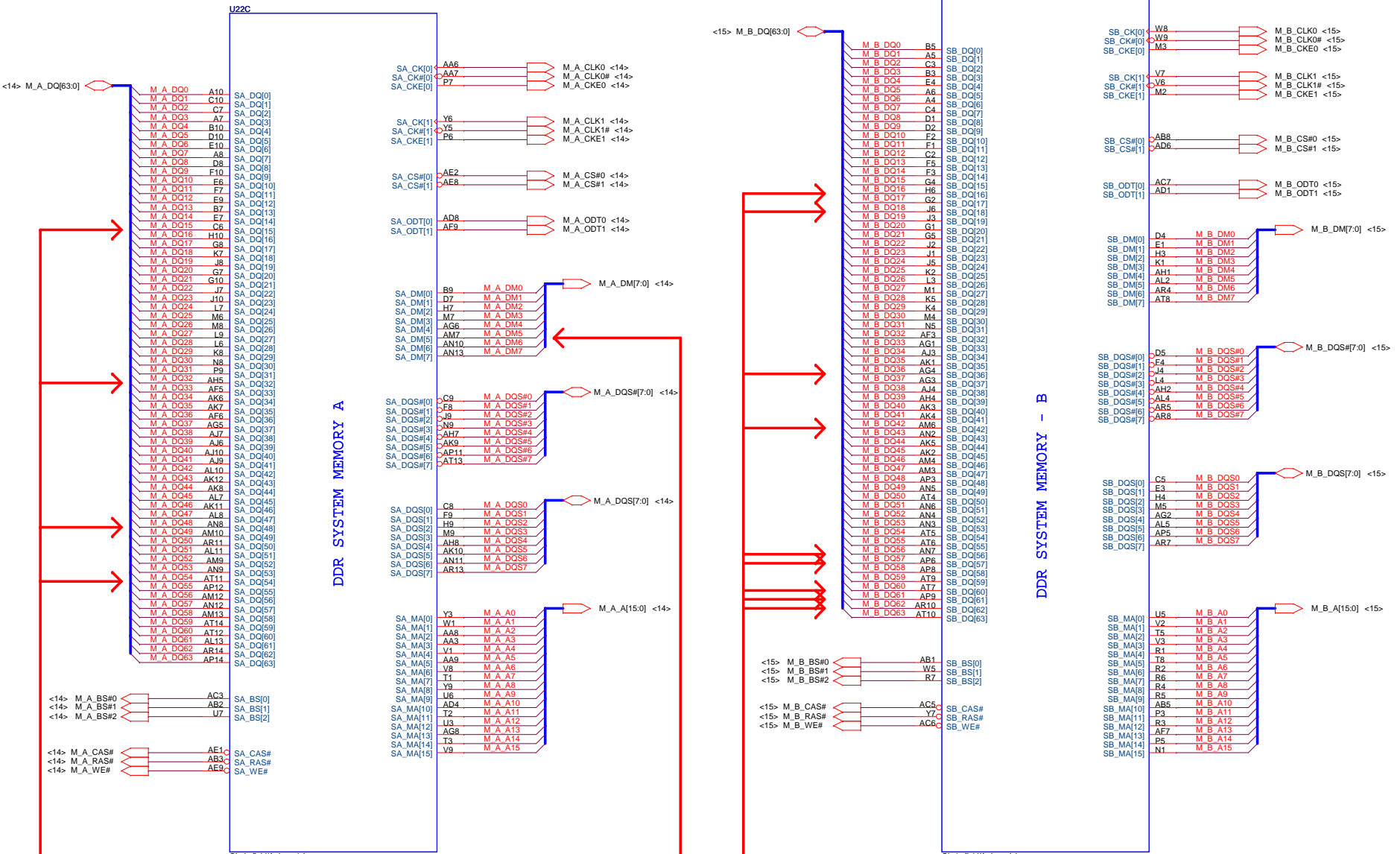
DPLL_REF_SSCCLK and DPLL_REF_SSCLK can be connected to GND on Arrandale directly if motherboard only supports discrete graphics. If motherboard supports integrated graphics but without eDP, these pins can also be connected to GND directly.



<The GFX_IMON, FDI_FSYN0[0], FDI_FSYN0[1], FDI_LSYN0[0], FDI_LSYN0[1], FDI_LSYN1[1], and FDI_INT>Note that if these signals are left as no connect, there are no functional impacts, but a small amount of power (~15 mW) maybe wasted.



AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

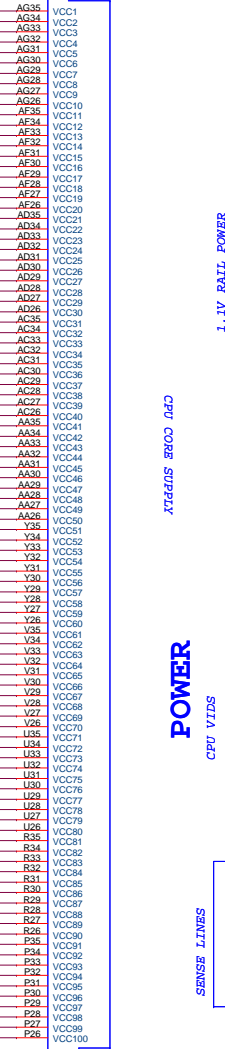
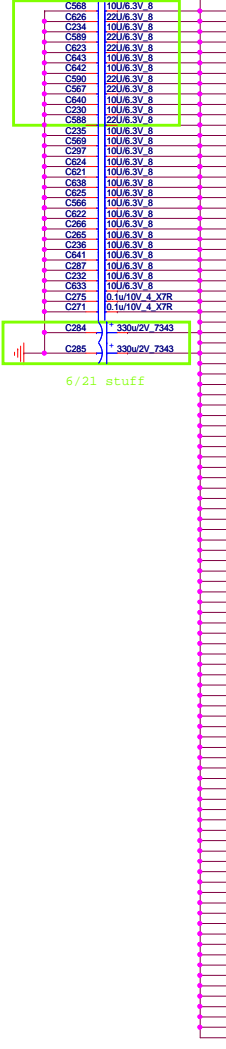


Channel A DQ[15,32,48,54], DM[5]
Requires minimum 12mils spacing
with all other signals, including data signals.

Channel B DQ[16,18,36,42,56,57,60,61,62]
Requires minimum 12mils spacing
with all other signals, including data signals.

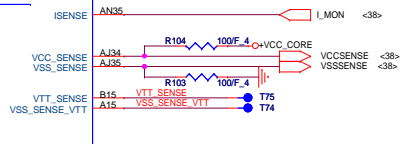
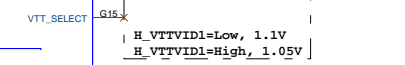
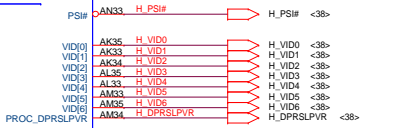
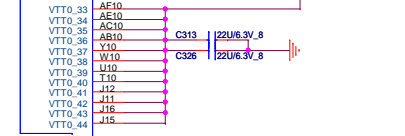
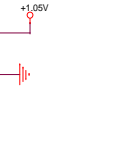
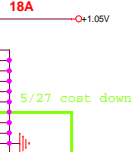
CPU Core Power U22F

5/27 cost down
ARD:48A
CFD:52A
 +VCC_CORE



1.1V RAIL POWER
 CPU CORE SUPPLY
 CPU VIDS
 SENSE LINES

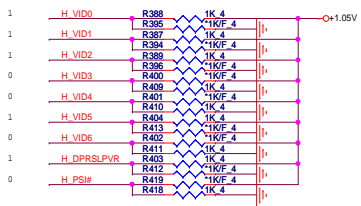
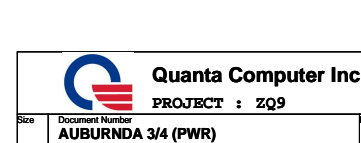
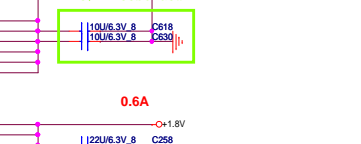
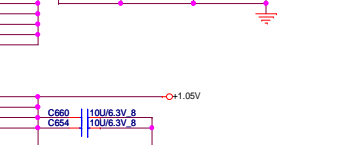
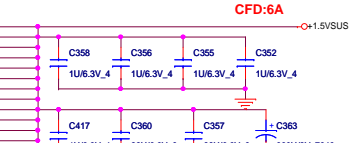
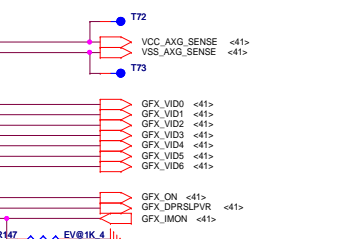
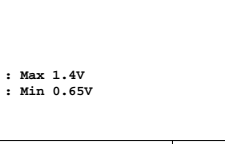
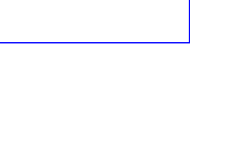
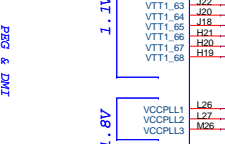
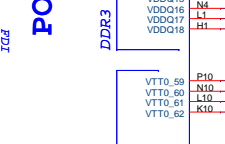
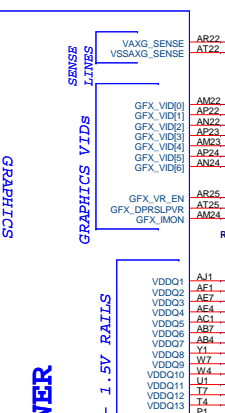
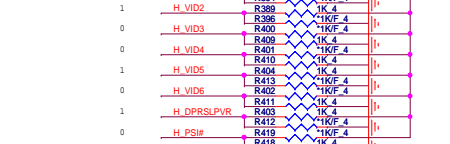
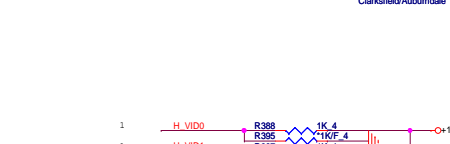
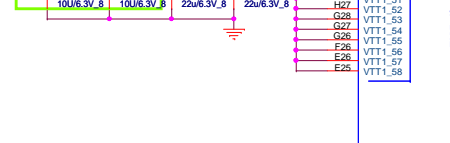
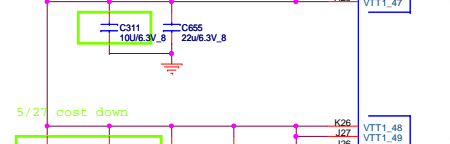
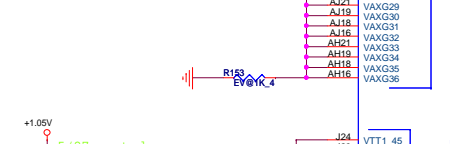
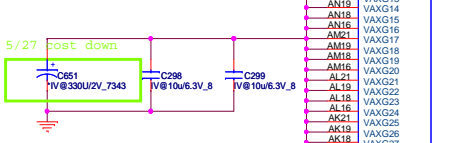
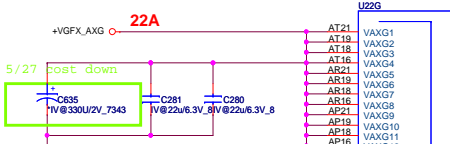
VTT Rail Values are
 Auburndale VTT=1.05V
 Clarkfield VTT=1.1V



Clarkfield/Auburndale

AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)

AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)



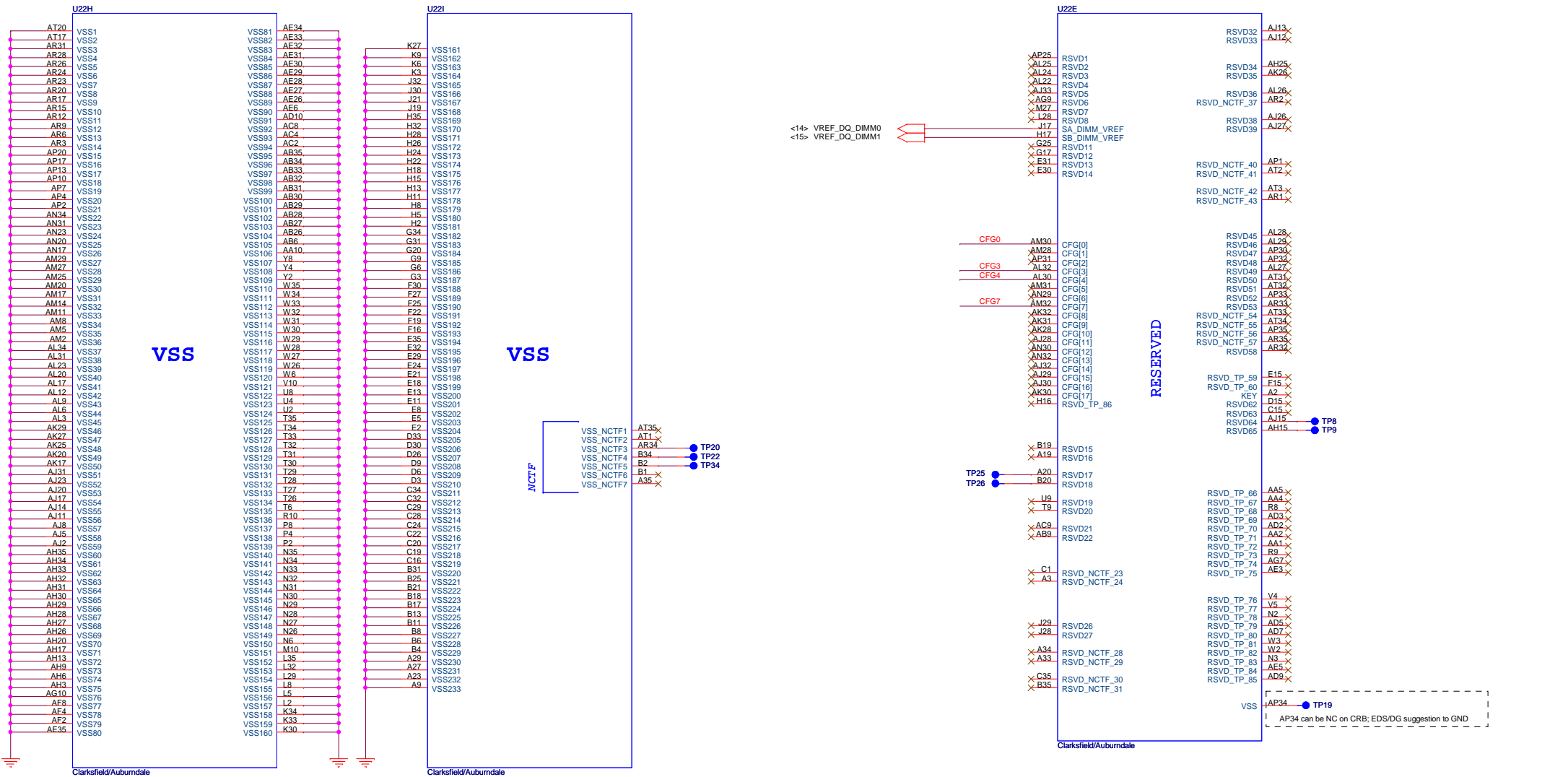
Note:
 For Validating IMV9 VR R6451 should be STUFF
 and R2N1 NO_STUFF

HFM_VID : Max 1.4V
 LFM_VID : Min 0.65V

Quanta Computer Inc.
PROJECT : ZQ9
 Size Document Number
AUBURND 3/4 (PWR)
 Date: Tuesday, Jun 22, 2010 Sheet 6 of 45


AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

AUBURNDALE/CLARKSFIELD PROCESSOR (RESERVED, CFG)



Processor Strapping

	1	0	DEFAULT	
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled	1	
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed	1	
CFG4 (Embedded Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port	1	



Quanta Computer Inc.
PROJECT : ZR7B

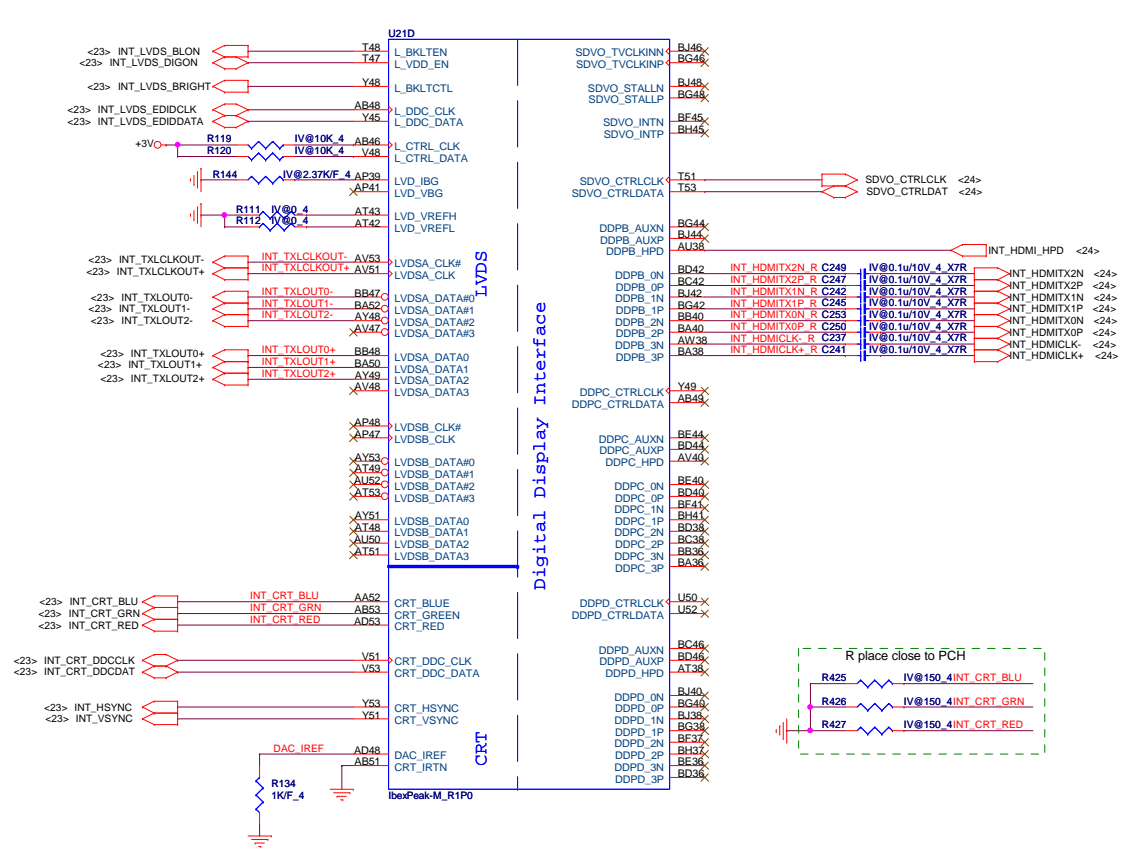
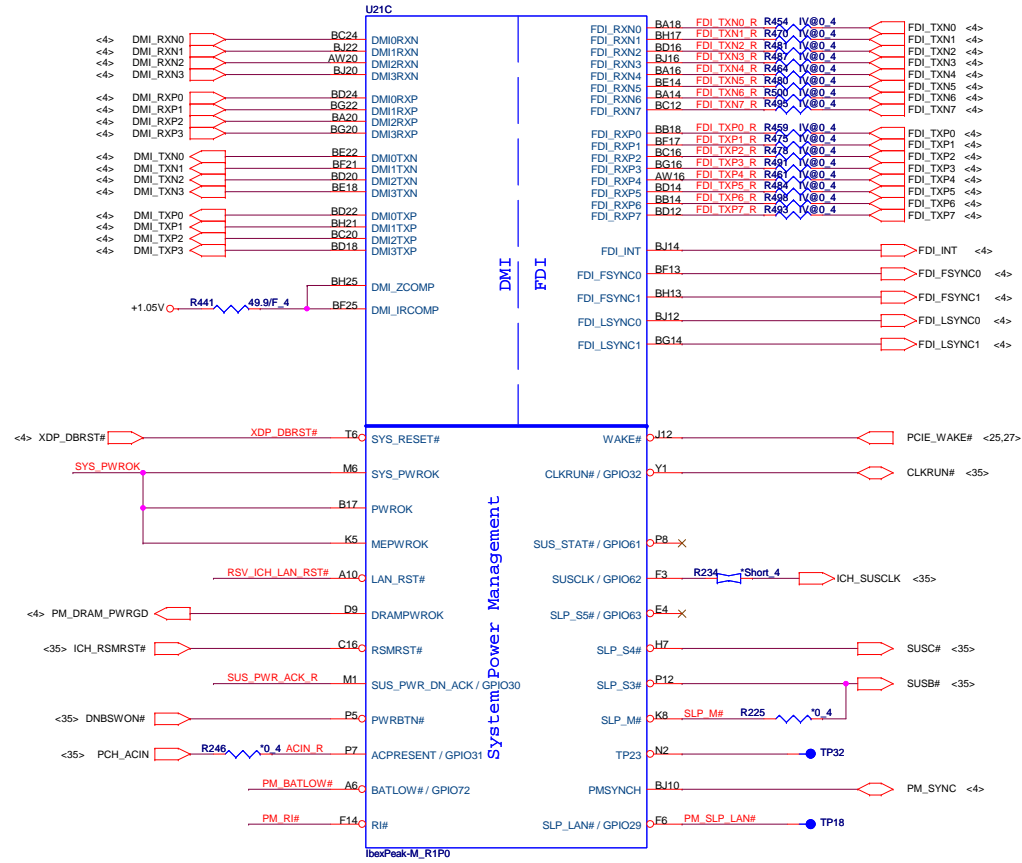
Size	Document Number	Rev
	AUBURND 4/4	1A
Date: Tuesday, June 22, 2010		Sheet 7 of 45

IBEX PEAK-M (DMI, FDI, GPIO)

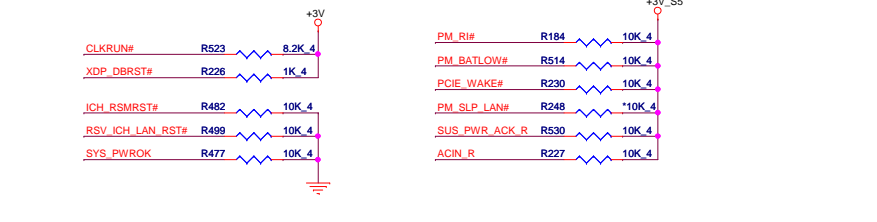
AC-coupling CAP place close to PCH

0-ohm resistor place close to PCH

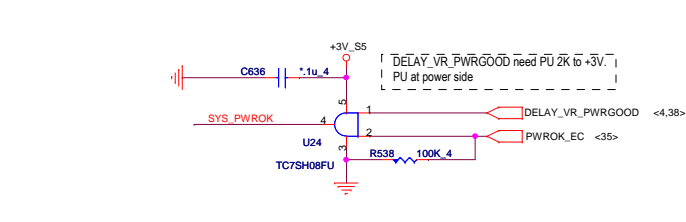
IBEX PEAK-M (LVDS, DDI)



PCH Pull-high/low



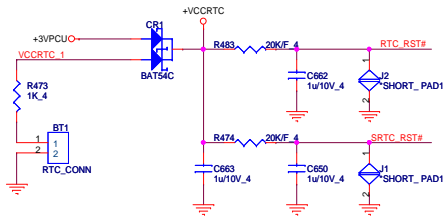
System PWR_OK



Quanta Computer Inc.
PROJECT : ZQ9

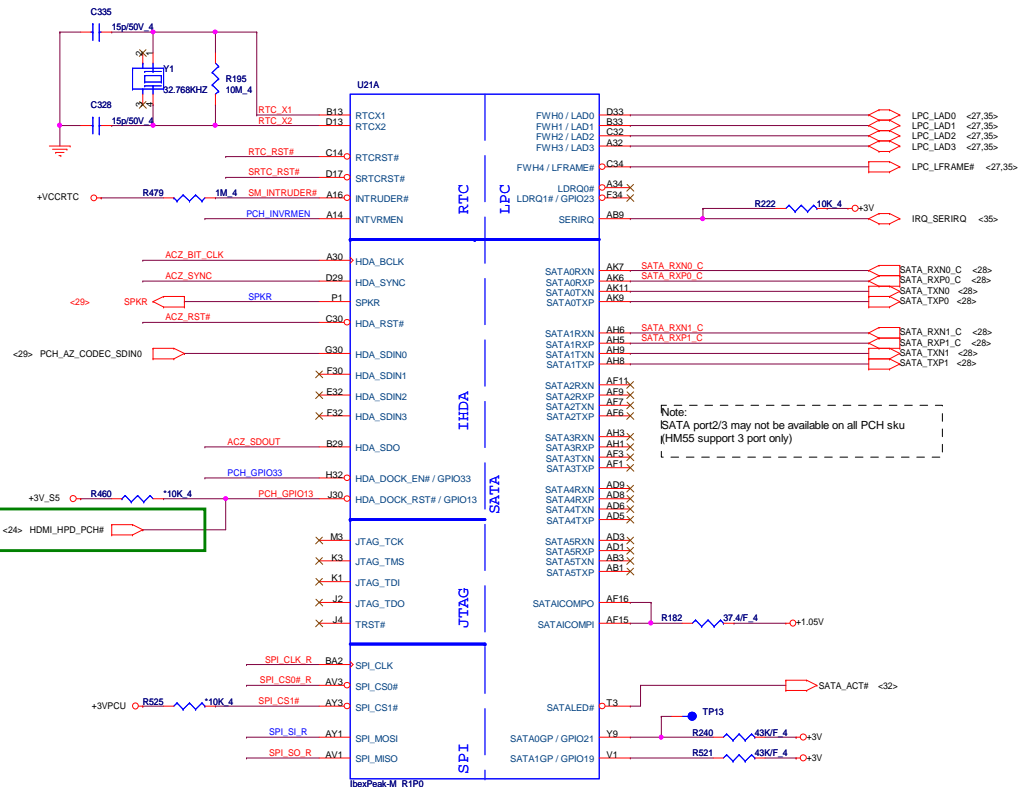
Size	Document Number	Rev	1A
IBEX PEAK-M 1/6			
Date:	Tuesday, June 22, 2010	Sheet	8 of 45

RTC Circuitry

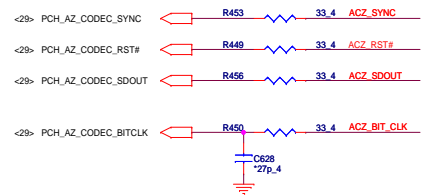


HDA_SYNC (PCH strap pin)

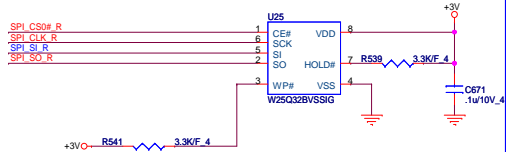
Internal weak pull-down
 VCCVRM=>+1.8V (default)
 external pull-up
 VCCVRM=>+1.5V



HDA Bus

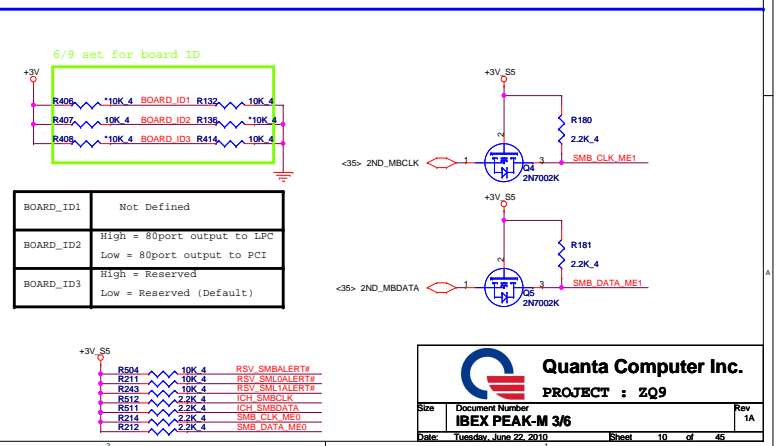
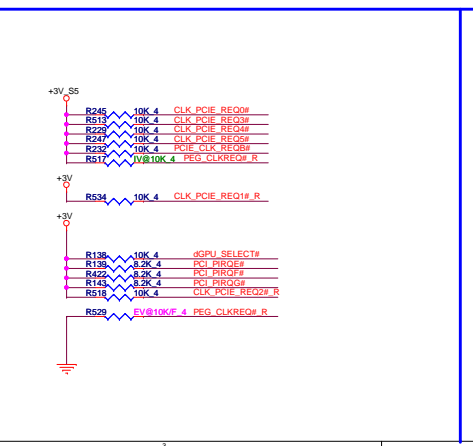
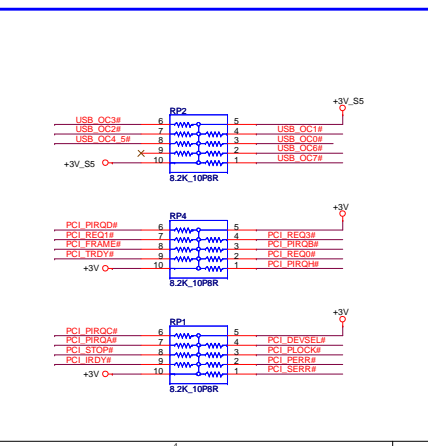
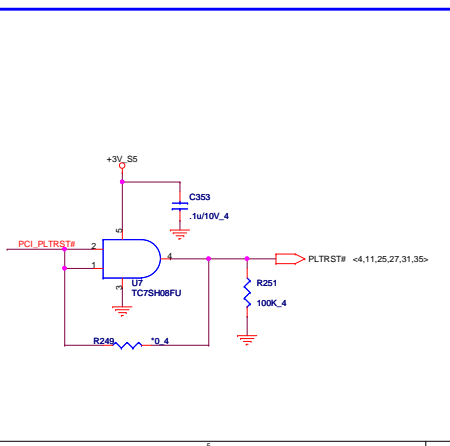
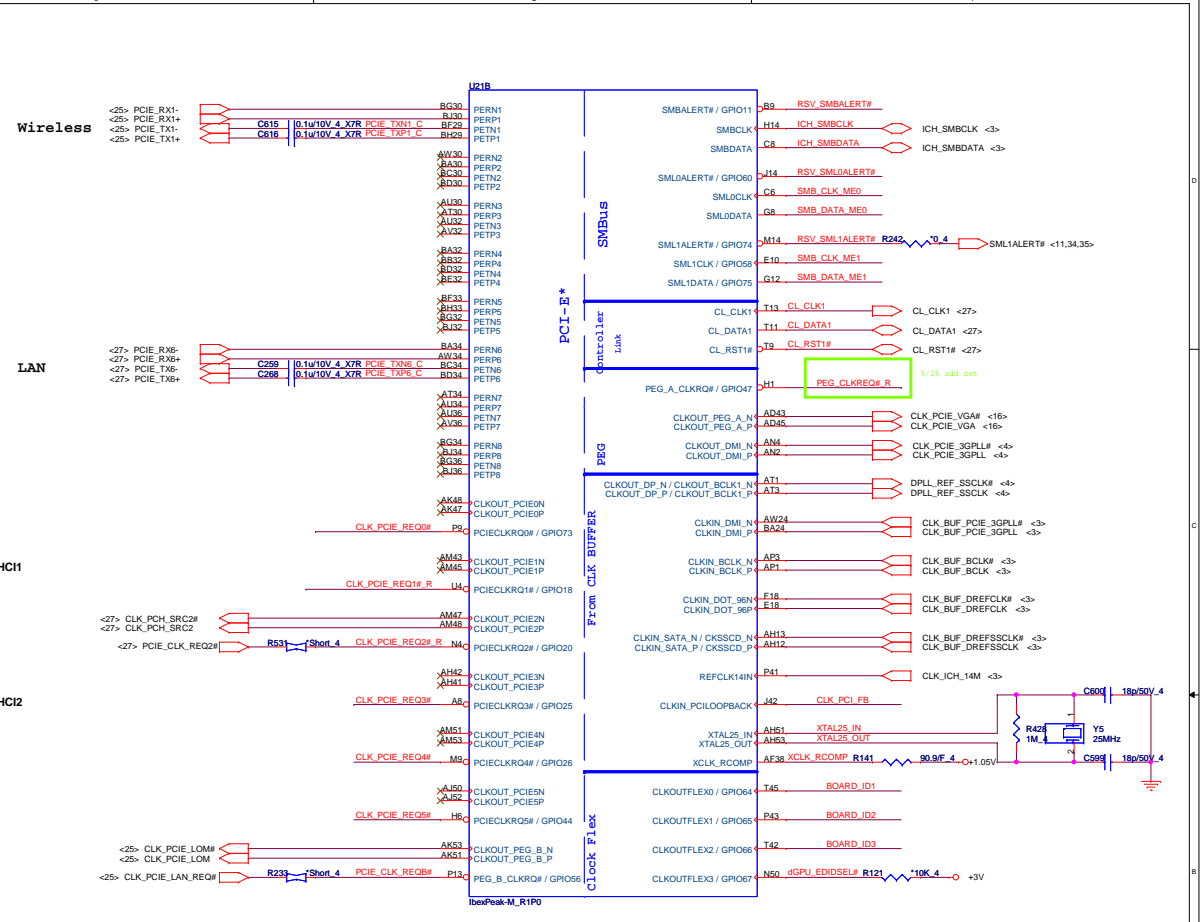
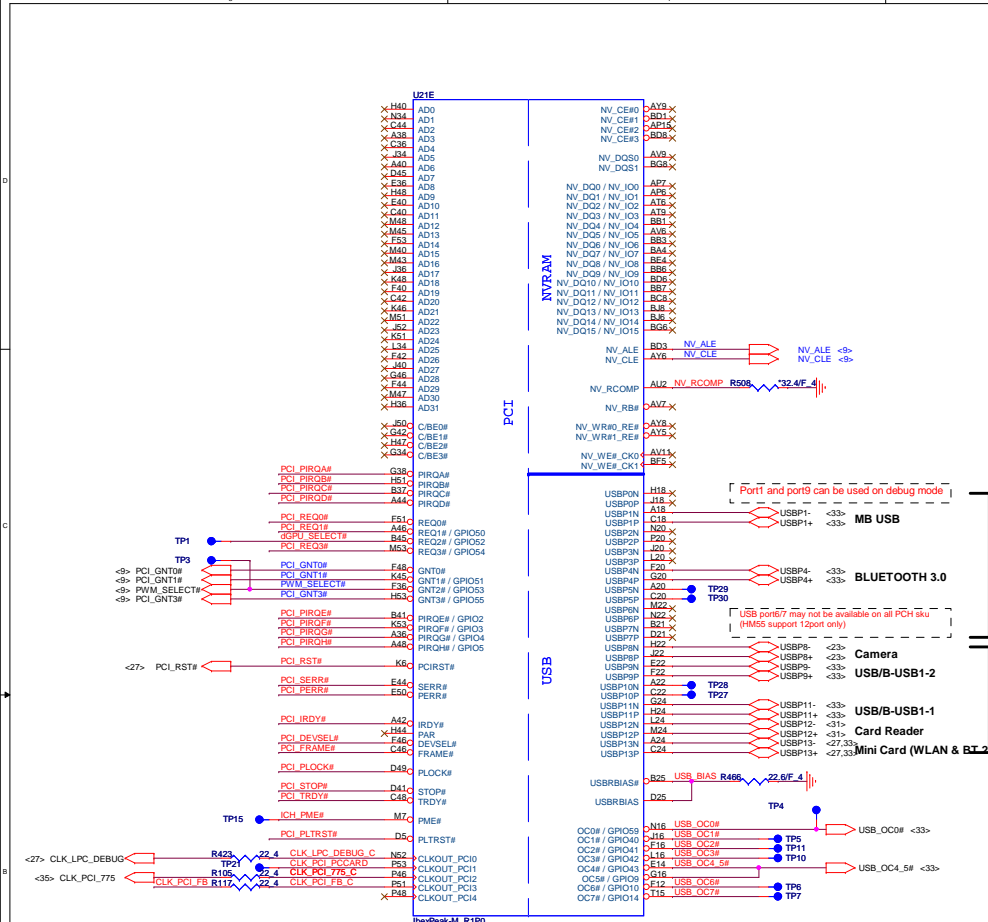


PCH SPI

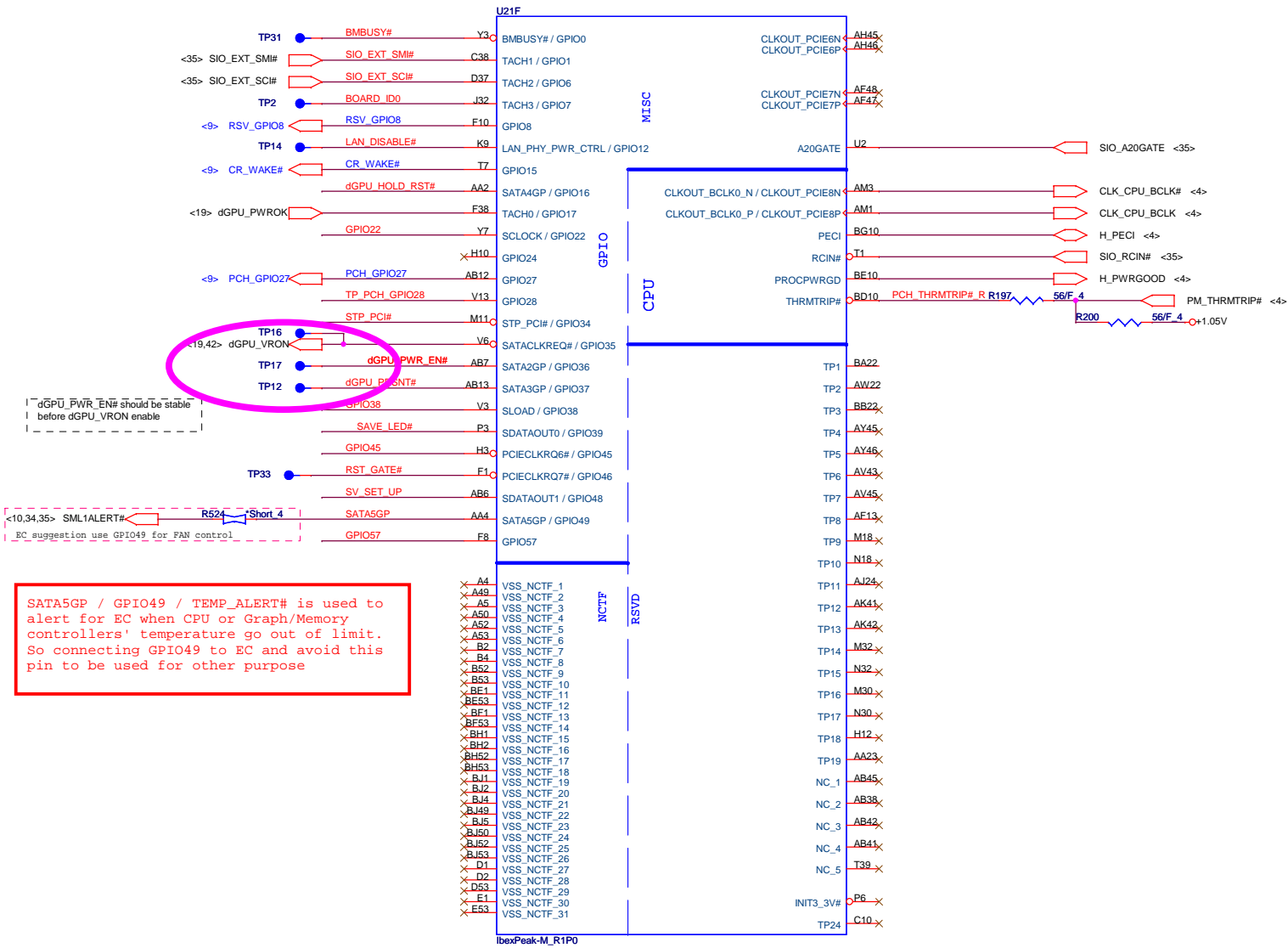


PCH Strap Pin Configuration Table-1

INTVRMEN	Integrated 1.05V VRM Enable / Disable	1 = Integrated VRM is enabled 0 = Integrated VRM is disabled	+VCCRTC - R489 - 330K_6 - PCH_INVRMEN
SPI_MOSI	TPM Functionality Disable	1 = Enabled 0 = Disable	+3V - R540 - 1K_4 - SPI_SI_R
SPKR	Reboot option at power-up	0 = Default Mode (Internal weak Pull-down) 1 = No Reboot Mode with TCO Disabled	+3V - R532 - 1K1F_4 - SPKR
HDA_DOCK# / GPIO33	Flash Descriptor Security Override	0 = Flash Descriptor Security will be overridden 1 = Security measure defined in the Flash Descriptor will be enabled.	PCH_GPI033 - R164 - 1K1F_4 - R145 - 1K1F_4 - +3V
GNT0#, GNT1#	Boot BIOS Strap	(0,0) = LPC (0,1) = Reserved NAND (1,0) = PCI (1,1) = SPI	<10> - R129 - 1K_4 - +3V <10> - R122 - 1K_4 - +3V <10> - R131 - 1K_4 - +3V
GNT2# / GPIO53	ESI Strap (Server Only)	ESI compatible mode is for server platforms only	<10> - PWM_SELECT# - R158 - 1K1F_4
GNT3# / GPIO55	Top-Block Swap Override	0 = Top Block Swap Mode 1 = Default Mode (Internal pull-up)	<10> - PCI_GNT3# - R421 - 10K1F_4
NV_ALE	IntelR Anti-Theft Technology HDD Data Protection (Intel AT-0) Enable	1 = Enabled 0 = Disabled (Default)	<10> - NV_ALE - R202 - 1K1F_4 - +1.8V
NV_CLE	DMI Termination Voltage	DMI termination voltage. Weak internal pull-up. Do not pull low.	<10> - NV_CLE - R206 - 1K1F_4 - +1.8V
GPIO8	Reserved	This signal has a weak internal pull up. NOTE: This signal should not be pulled low	SV_GPIO8 - R204 - 10K_4 - +3V_S5 R203 - 1K_4
GPIO15	Reserved	0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality	CR_WAKE# - R244 - 1K_4 - +3V_S5
GPIO27	On-Die PLL Voltage Regulator <internal weak pull-up>	0 = Disables the VccVRM. 1 = Enables the internal VccVRM to have a clean supply for analog rails.	<1> - PCH_GPIO27 - R221 - 10K_4

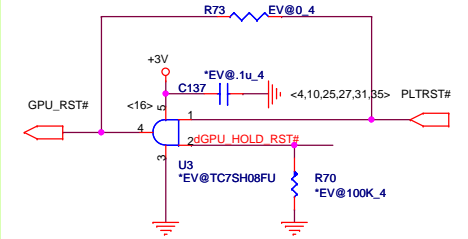


IBEX PEAK-M (GPIO, VSS_NCTF, RSVD)



GPU_RST#

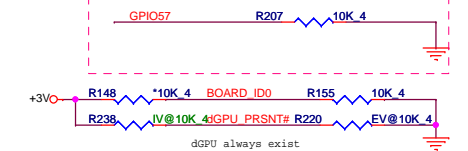
5/18 change for discrete only



GPIO Pull-up/Pull-down



GPIO57 stuff PD and not stuff PU for Intel suggestion at 6/1



5/18 separate for 14" & 15"

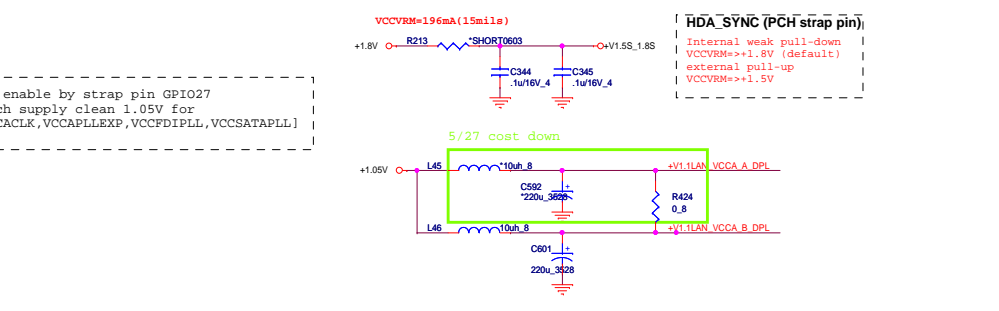
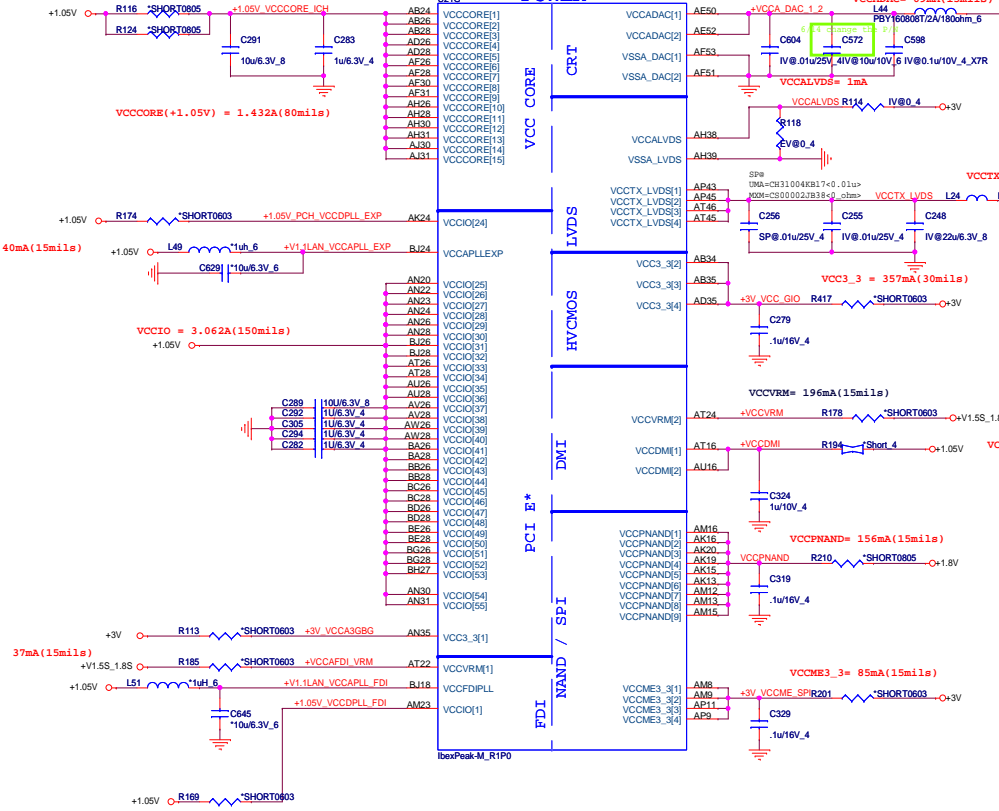
BOARD_ID0	High = 15"
	Low = 14"
RSV_GPIO8	High = Disable
	Low = Enable



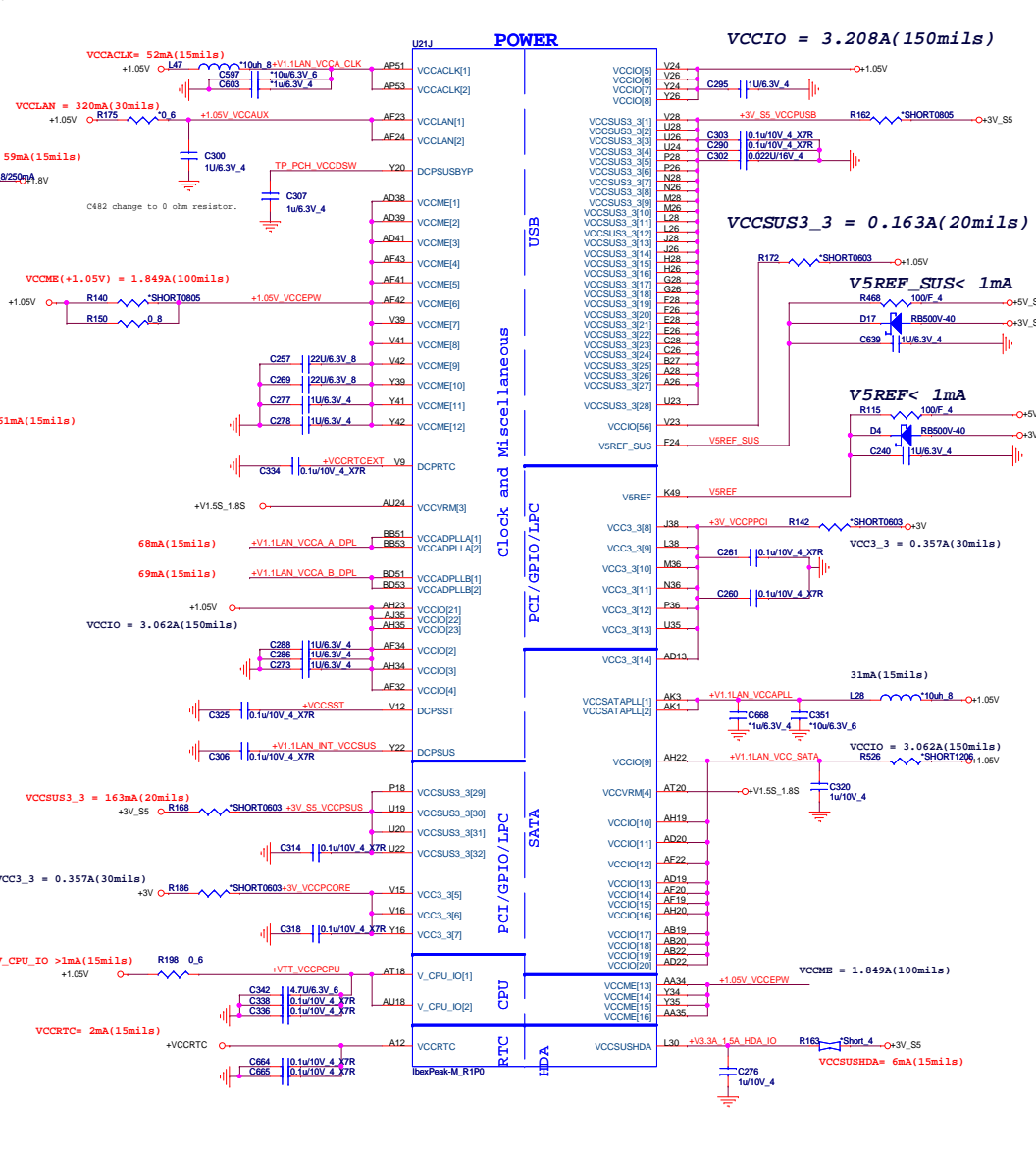
Quanta Computer Inc.

PROJECT : ZQ9

IBEX PEAK-M (POWER)



3.3 V. This rail should be powered during B9 system state. Note that Thermal Sensor shares the same power supply rail with DAC. The external filters on this pin are not needed in case internal graphic is disabled so only 3.3-V connection is required.

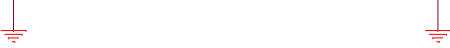


IBEX PEAK-M (GND)

U21H

AB16	VSS[0]	
AA19	VSS[1]	VSS[80] AK30
AA20	VSS[2]	VSS[81] AK31
AA22	VSS[3]	VSS[82] AK32
AM19	VSS[4]	VSS[83] AK34
AA24	VSS[5]	VSS[84] AK35
AA26	VSS[6]	VSS[85] AK38
AA28	VSS[7]	VSS[86] AK43
AA31	VSS[8]	VSS[87] AK46
AA33	VSS[9]	VSS[88] AK49
AA32	VSS[10]	VSS[89] AK5
AB11	VSS[11]	VSS[90] AK8
AB15	VSS[12]	VSS[91] AL2
AB23	VSS[13]	VSS[92] AL52
AB30	VSS[14]	VSS[93] AM11
AB31	VSS[15]	VSS[94] BB44
AB32	VSS[16]	VSS[95] AD24
AB39	VSS[17]	VSS[96] AM20
AB43	VSS[18]	VSS[97] AM22
AB47	VSS[19]	VSS[98] AM24
AB5	VSS[20]	VSS[99] AM26
AB5	VSS[21]	VSS[100] BM20
AC2	VSS[22]	VSS[101] BE12
AC52	VSS[23]	VSS[102] BE16
AD11	VSS[24]	VSS[103] BE20
AD12	VSS[25]	VSS[104] BE24
AD16	VSS[26]	VSS[105] AM30
AD23	VSS[27]	VSS[106] AM31
AD30	VSS[28]	VSS[107] AM32
AD31	VSS[29]	VSS[108] AM34
AD32	VSS[30]	VSS[109] AM35
AD34	VSS[31]	VSS[110] AM38
AU22	VSS[32]	VSS[111] AM39
AD42	VSS[33]	VSS[112] AM42
AD46	VSS[34]	VSS[113] AU2
AD49	VSS[35]	VSS[114] AM46
AD7	VSS[36]	VSS[115] AM50
AE2	VSS[37]	VSS[116] BE50
AE4	VSS[38]	VSS[117] AN32
AF12	VSS[39]	VSS[118] AN50
AH9	VSS[40]	VSS[119] AN52
AU4	VSS[41]	VSS[120] AP12
AF35	VSS[42]	VSS[121] AP42
AF13	VSS[43]	VSS[122] AP46
AN34	VSS[44]	VSS[123] AP49
AF45	VSS[45]	VSS[124] AP5
AF46	VSS[46]	VSS[125] AP8
AF49	VSS[47]	VSS[126] AR2
AF5	VSS[48]	VSS[127] AR52
AF5	VSS[49]	VSS[128] AT11
AG2	VSS[50]	VSS[129] BA12
AG52	VSS[51]	VSS[130] AH48
AH11	VSS[52]	VSS[131] AT32
AH15	VSS[53]	VSS[132] AT36
AH16	VSS[54]	VSS[133] AT41
AH24	VSS[55]	VSS[134] AT47
AH32	VSS[56]	VSS[135] AT7
AV18	VSS[57]	VSS[136] AV12
AH43	VSS[58]	VSS[137] AV16
AH47	VSS[59]	VSS[138] AV20
AH7	VSS[60]	VSS[139] AV24
AJ19	VSS[61]	VSS[140] AV30
AJ2	VSS[62]	VSS[141] AV34
AJ20	VSS[63]	VSS[142] AV38
AJ22	VSS[64]	VSS[143] AV42
AJ23	VSS[65]	VSS[144] AV46
AJ26	VSS[66]	VSS[145] AV49
AJ28	VSS[67]	VSS[146] AV5
AJ32	VSS[68]	VSS[147] AW14
AJ34	VSS[69]	VSS[148] AW18
AT5	VSS[70]	VSS[149] AW18
AJ4	VSS[71]	VSS[150] AW2
AK12	VSS[72]	VSS[151] AW32
AM41	VSS[73]	VSS[152] AW36
AN19	VSS[74]	VSS[153] AW40
AK26	VSS[75]	VSS[154] AW52
AK22	VSS[76]	VSS[155] AW52
AK23	VSS[77]	VSS[156] AY11
AK28	VSS[78]	VSS[157] AY43
AK28	VSS[79]	VSS[158] AY47

IbexPeak-M_R1P0



U21

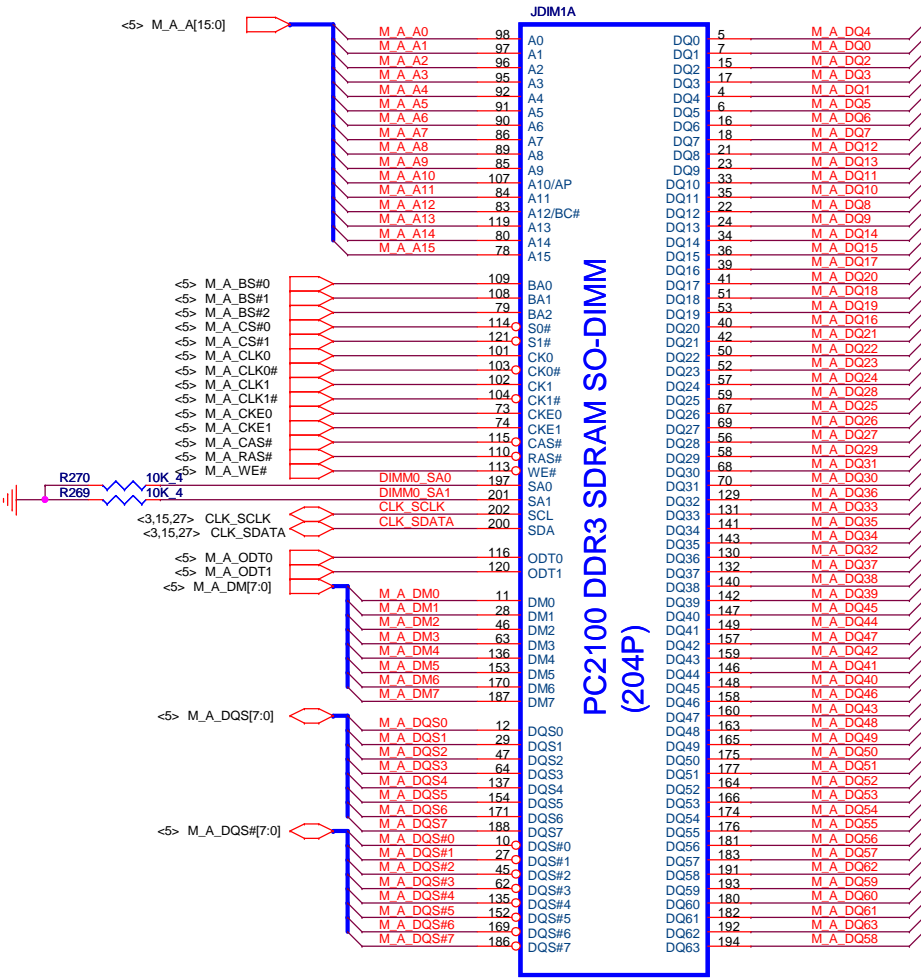
AY7	VSS[159]	VSS[259] H49
B11	VSS[160]	VSS[260] H5
B15	VSS[161]	VSS[261] J24
B19	VSS[162]	VSS[262] K11
B23	VSS[163]	VSS[263] K43
B31	VSS[164]	VSS[264] K47
B35	VSS[165]	VSS[265] K7
B39	VSS[166]	VSS[266] L14
B43	VSS[167]	VSS[267] L18
B47	VSS[168]	VSS[268] L2
B7	VSS[169]	VSS[269] L22
BG12	VSS[170]	VSS[270] L32
BB12	VSS[171]	VSS[271] L36
BB16	VSS[172]	VSS[272] L40
BB20	VSS[173]	VSS[273] L52
BB24	VSS[174]	VSS[274] M12
BB30	VSS[175]	VSS[275] M16
BB34	VSS[176]	VSS[276] M20
BB38	VSS[177]	VSS[277] M38
BB42	VSS[178]	VSS[278] M34
BB49	VSS[179]	VSS[279] M38
BB5	VSS[180]	VSS[280] M42
BC10	VSS[181]	VSS[281] M46
BC14	VSS[182]	VSS[282] M46
BC18	VSS[183]	VSS[283] M5
BC2	VSS[184]	VSS[284] M8
BC22	VSS[185]	VSS[285] P11
BC32	VSS[186]	VSS[286] AD15
BC36	VSS[187]	VSS[287] P22
BC40	VSS[188]	VSS[288] P30
BC44	VSS[189]	VSS[289] P32
BC52	VSS[190]	VSS[290] P34
BH9	VSS[191]	VSS[291] P42
BD48	VSS[192]	VSS[292] P45
BD49	VSS[193]	VSS[293] P47
BD5	VSS[194]	VSS[294] R2
BE12	VSS[195]	VSS[295] R52
BE16	VSS[196]	VSS[296] T12
BE20	VSS[197]	VSS[297] T41
BE24	VSS[198]	VSS[298] T46
BE30	VSS[199]	VSS[299] T49
BE34	VSS[200]	VSS[300] T5
BE38	VSS[201]	VSS[301] T8
BE42	VSS[202]	VSS[302] U30
BE46	VSS[203]	VSS[303] U31
BE48	VSS[204]	VSS[304] U32
BE50	VSS[205]	VSS[305] U34
BE6	VSS[206]	VSS[306] P38
BE8	VSS[207]	VSS[307] V11
BF3	VSS[208]	VSS[308] P16
BF49	VSS[209]	VSS[309] V19
BF51	VSS[210]	VSS[310] V20
BG18	VSS[211]	VSS[311] V22
BG24	VSS[212]	VSS[312] V30
BG4	VSS[213]	VSS[313] V31
BG50	VSS[214]	VSS[314] V32
BH11	VSS[215]	VSS[315] V34
BH15	VSS[216]	VSS[316] V35
BH19	VSS[217]	VSS[317] V38
BH23	VSS[218]	VSS[318] V43
BH31	VSS[219]	VSS[319] V45
BH35	VSS[220]	VSS[320] V46
BH39	VSS[221]	VSS[321] V47
BH43	VSS[222]	VSS[322] V49
BH47	VSS[223]	VSS[323] V5
BH7	VSS[224]	VSS[324] V7
C12	VSS[225]	VSS[325] V8
C50	VSS[226]	VSS[326] W2
D51	VSS[227]	VSS[327] W52
E12	VSS[228]	VSS[328] Y11
E16	VSS[229]	VSS[329] Y12
E20	VSS[230]	VSS[330] Y15
E24	VSS[231]	VSS[331] Y19
E30	VSS[232]	VSS[332] Y23
E34	VSS[233]	VSS[333] Y28
E38	VSS[234]	VSS[334] Y30
E42	VSS[235]	VSS[335] Y31
E46	VSS[236]	VSS[336] Y32
E48	VSS[237]	VSS[337] Y38
E6	VSS[238]	VSS[338] Y43
E8	VSS[239]	VSS[339] Y46
F49	VSS[240]	VSS[340] P49
F5	VSS[241]	VSS[341] Y5
G10	VSS[242]	VSS[342] Y6
G14	VSS[243]	VSS[343] Y8
G18	VSS[244]	VSS[344] P24
G2	VSS[245]	VSS[345] T43
G22	VSS[246]	VSS[346] AD51
G32	VSS[247]	VSS[347] ATR
G36	VSS[248]	VSS[348] AD47
G40	VSS[249]	VSS[349] Y47
G44	VSS[250]	VSS[350] AT12
G52	VSS[251]	VSS[351] AM6
AF39	VSS[252]	VSS[352] AT13
H16	VSS[253]	VSS[353] AM5
H20	VSS[254]	VSS[354] AK45
H30	VSS[255]	VSS[355] AK38
H34	VSS[256]	VSS[356] AV14
H38	VSS[257]	
H42	VSS[258]	

IbexPeak-M_R1P0



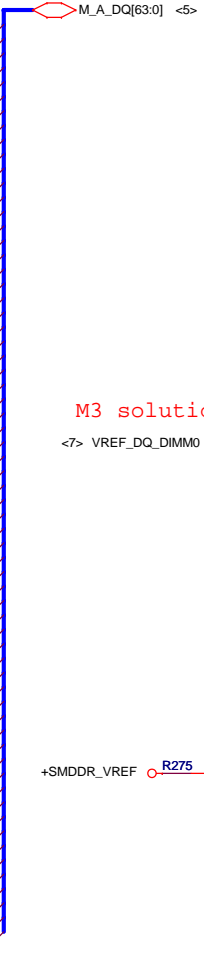
Quanta Computer Inc.
PROJECT : ZQ9

Size	Document Number	Rev
	IBEX PEAK-M 6/6	1A
Date:	Tuesday, June 22, 2010	Sheet 13 of 45

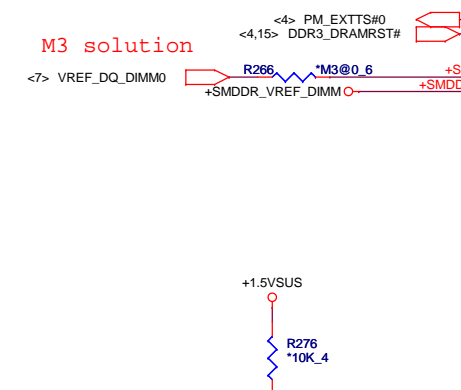


PC2100 DDR3 SDRAM SO-DIMM (204P)

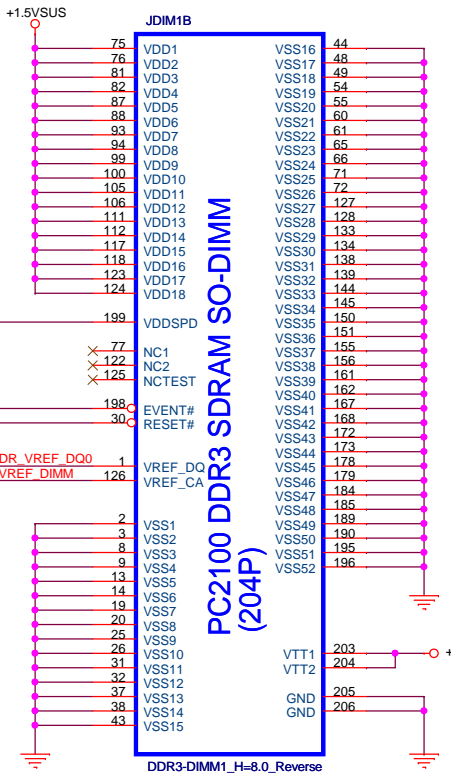
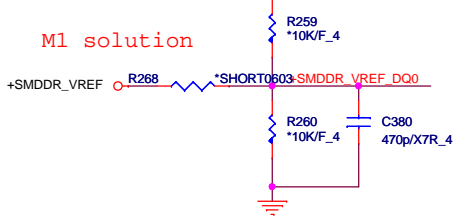
DDR3-DIMM1_H=8.0_Reverse



M3 solution



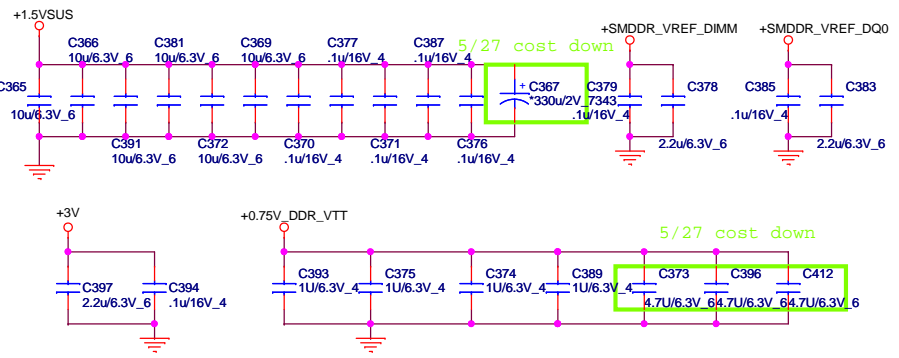
M1 solution

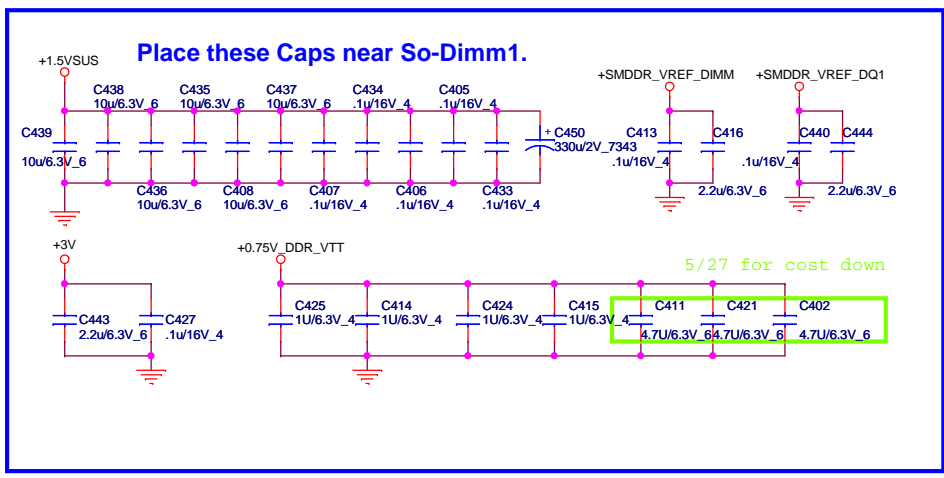
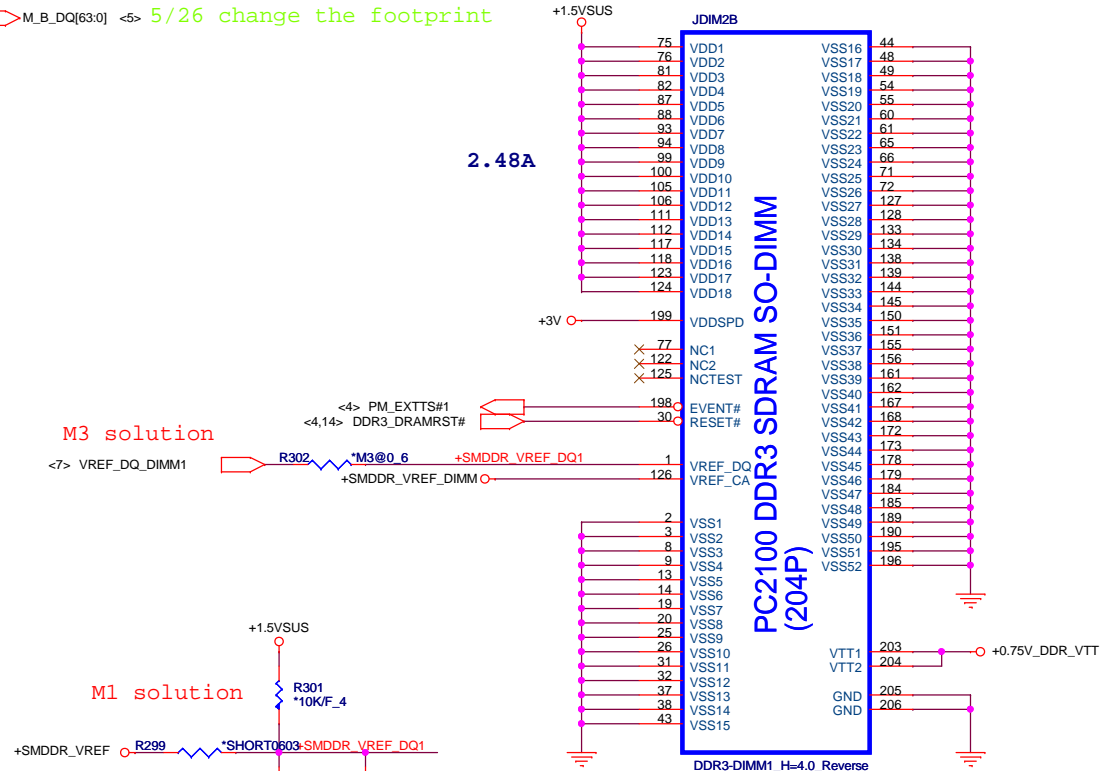
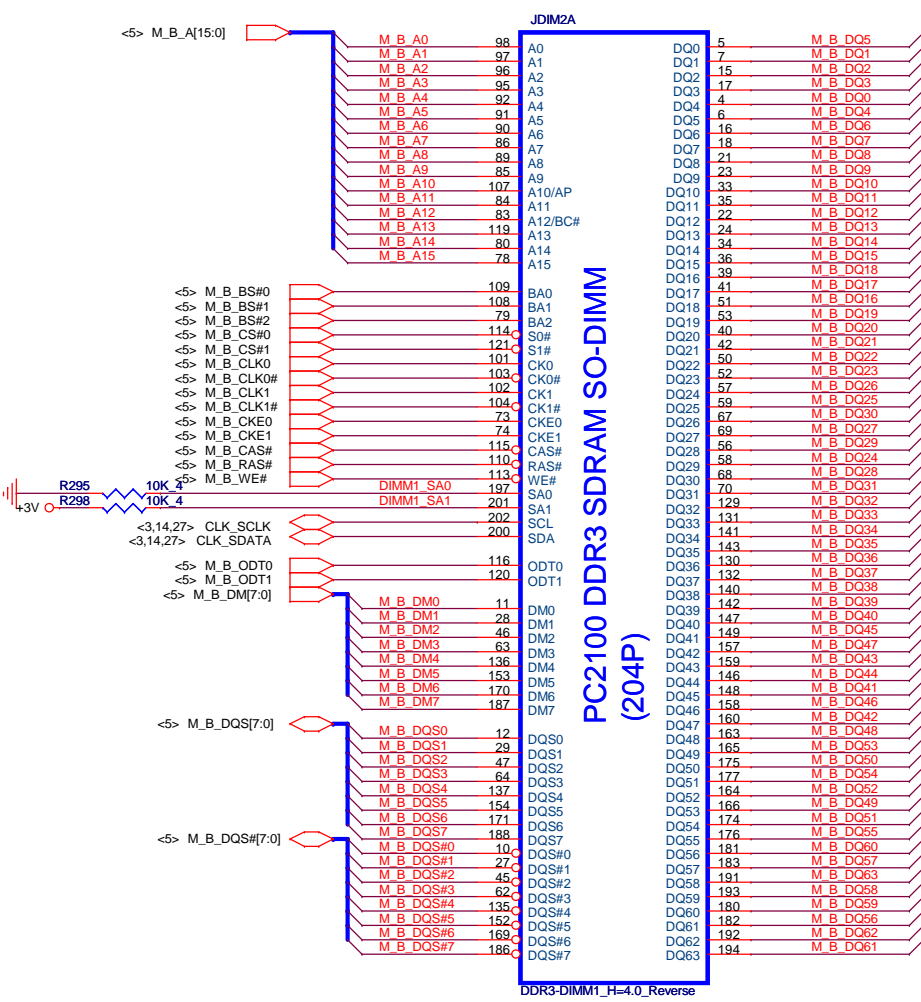


PC2100 DDR3 SDRAM SO-DIMM (204P)



Place these Caps near So-Dimm0.



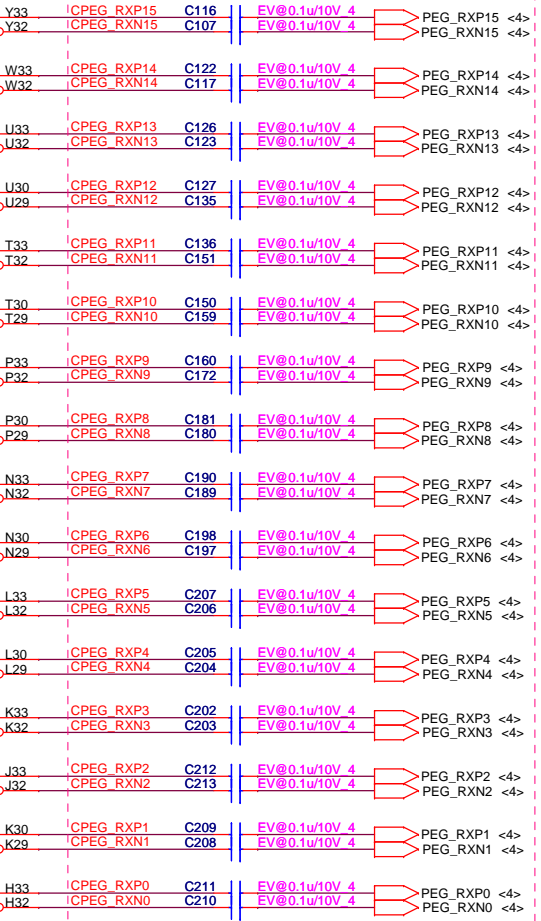
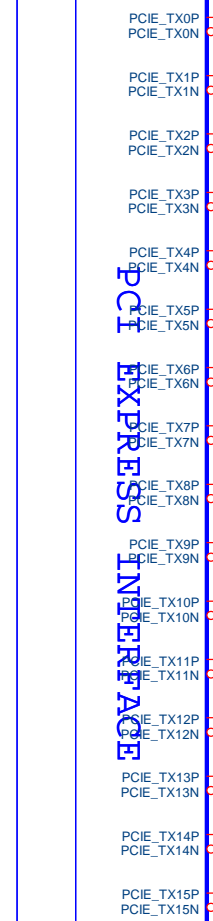
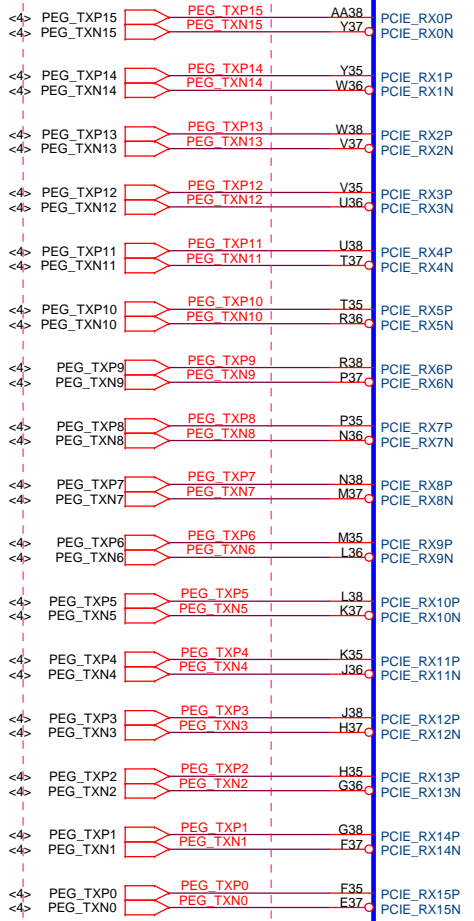
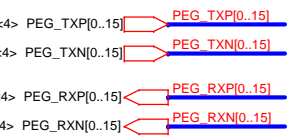


GPU_1(VGA)

U15A

0518 SWAP PCIE for VGA side

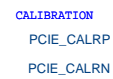
0518 SWAP PCIE for VGA side



PCI EXPRESS INTERFACE



For Broadway, Madison and Park the PWRGOOD ball must be connected to ground



For M97, Broadway, Madison and Park PCIE_VDDC is 1.0V

Madison	AJ007720T02
Park	AJ077400T08

Quanta Computer Inc.
PROJECT : ZQ9

Size	Document Number	Rev
Date	Tuesday, June 22, 2010	1A

Sheet 16 of 45

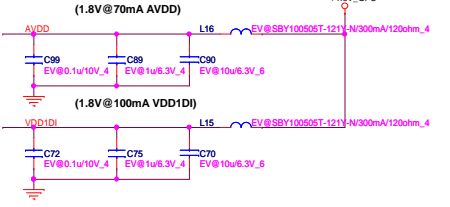
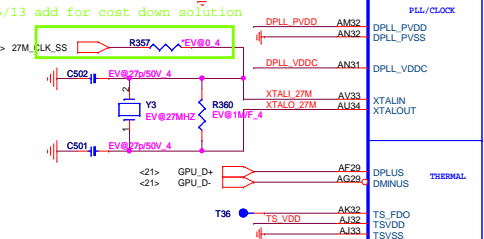
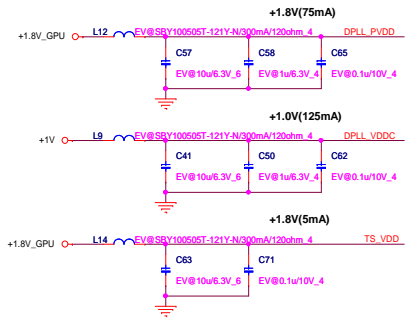
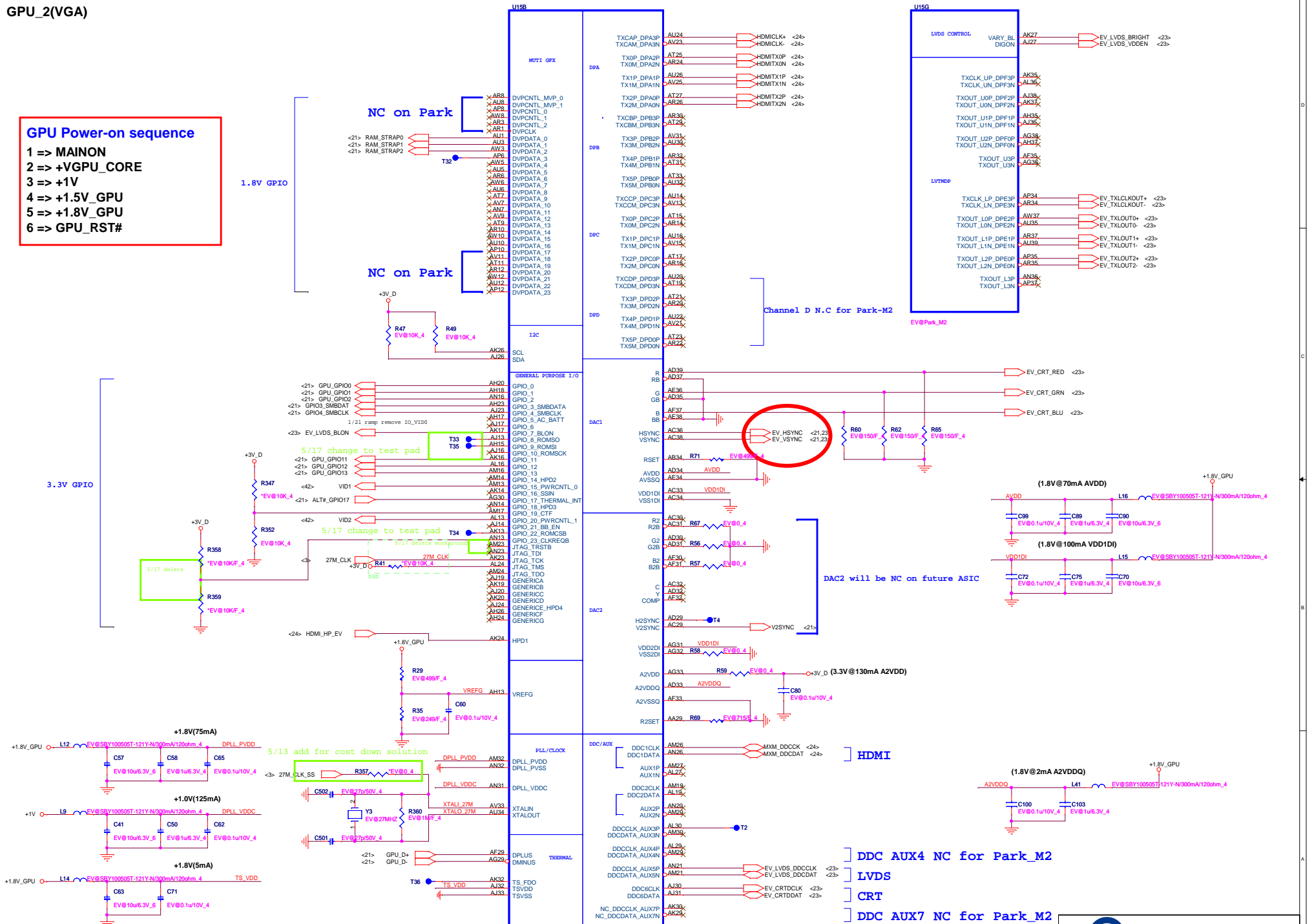
GPU_2(VGA)

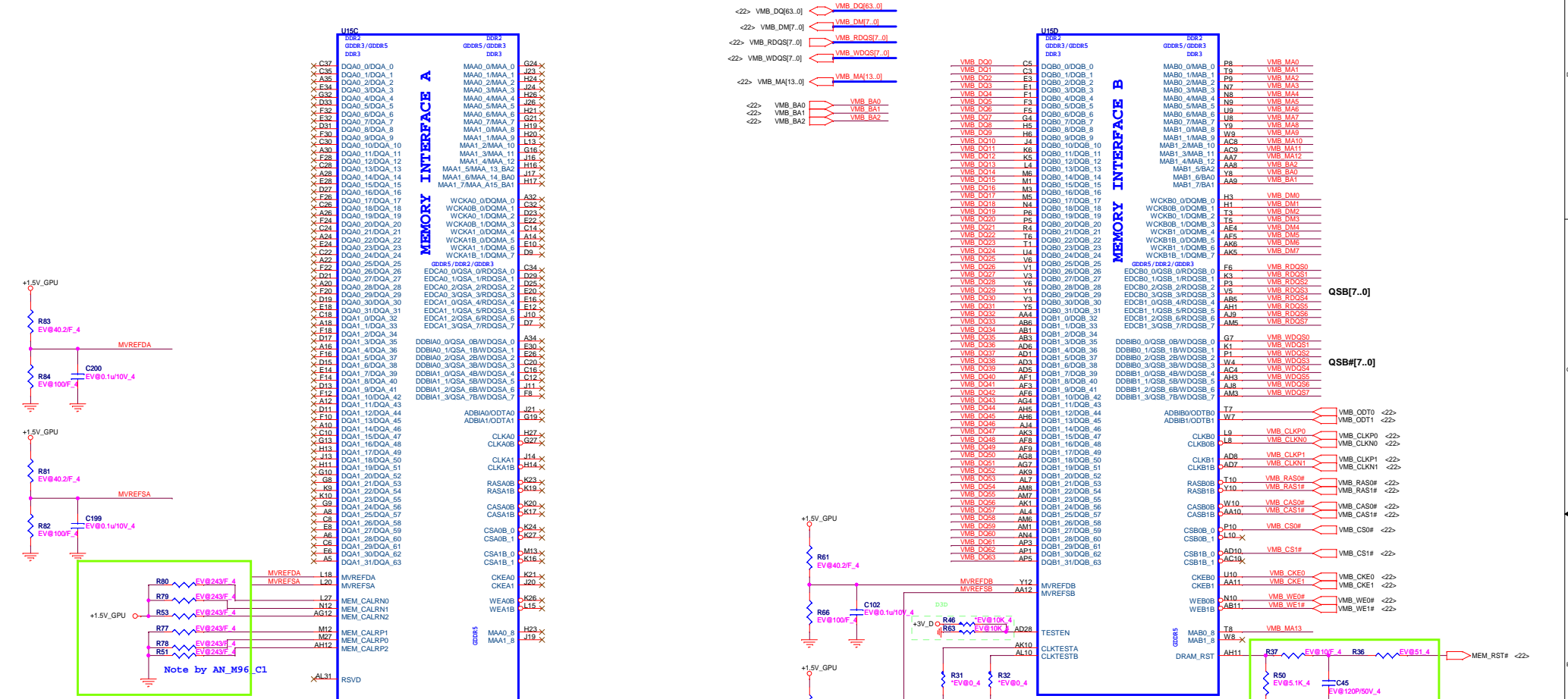
GPU Power-on sequence

- 1 => MAINON
- 2 => +VGPU_CORE
- 3 => +1V
- 4 => +1.5V_GPU
- 5 => +1.8V_GPU
- 6 => GPU_RST#

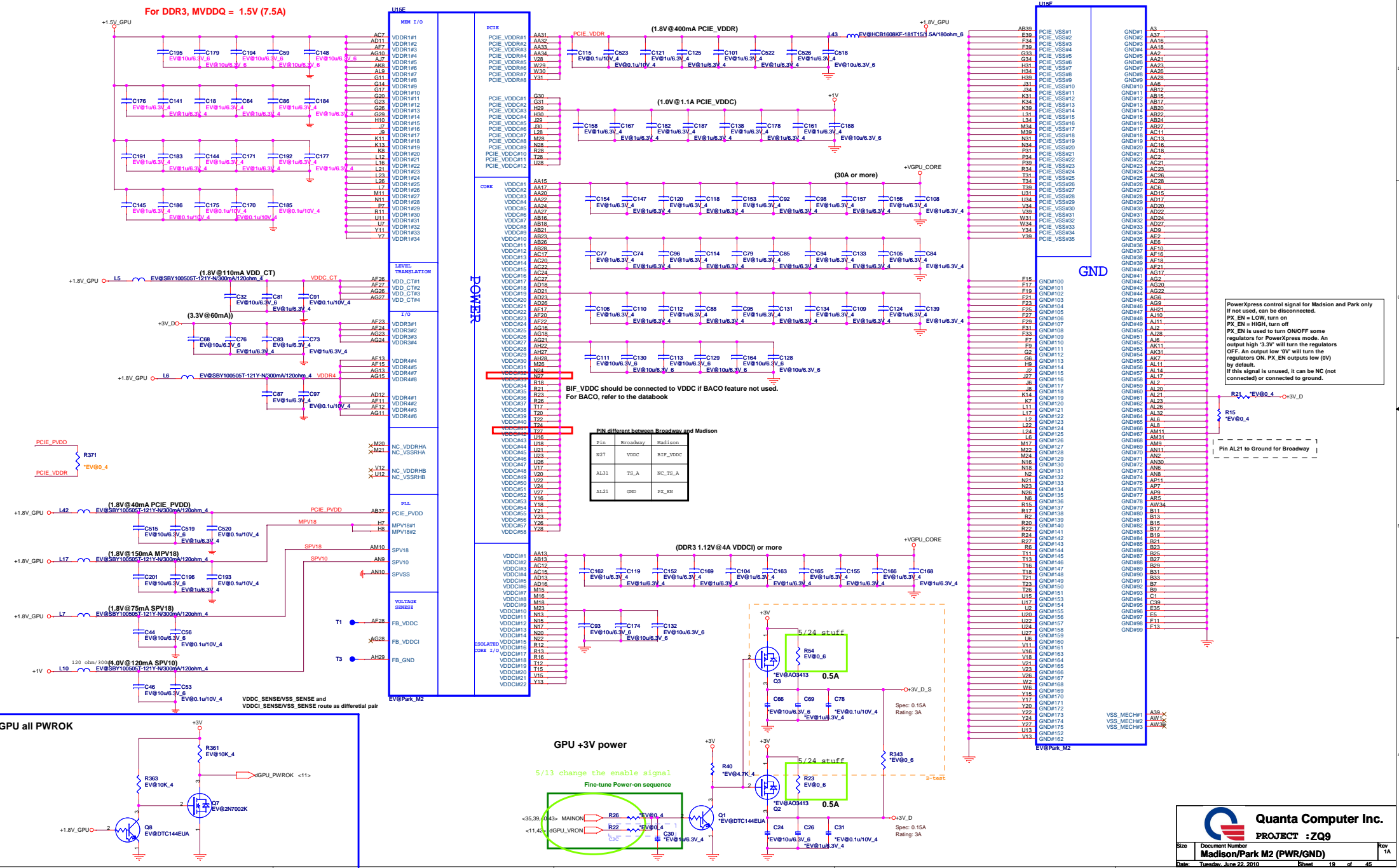
1.8V GPIO

3.3V GPIO





For DDR3, MVDDQ = 1.5V (7.5A)



BIF_VDDC should be connected to VDDC if BACO feature not used. For BACO, refer to the databook

Pin different between Broadway and Madison

Pin	Broadway	Madison
N27	VDDC	BIF_VDDC
AL31	TS_A	NC_TS_A
AL21	GND	PX_EN

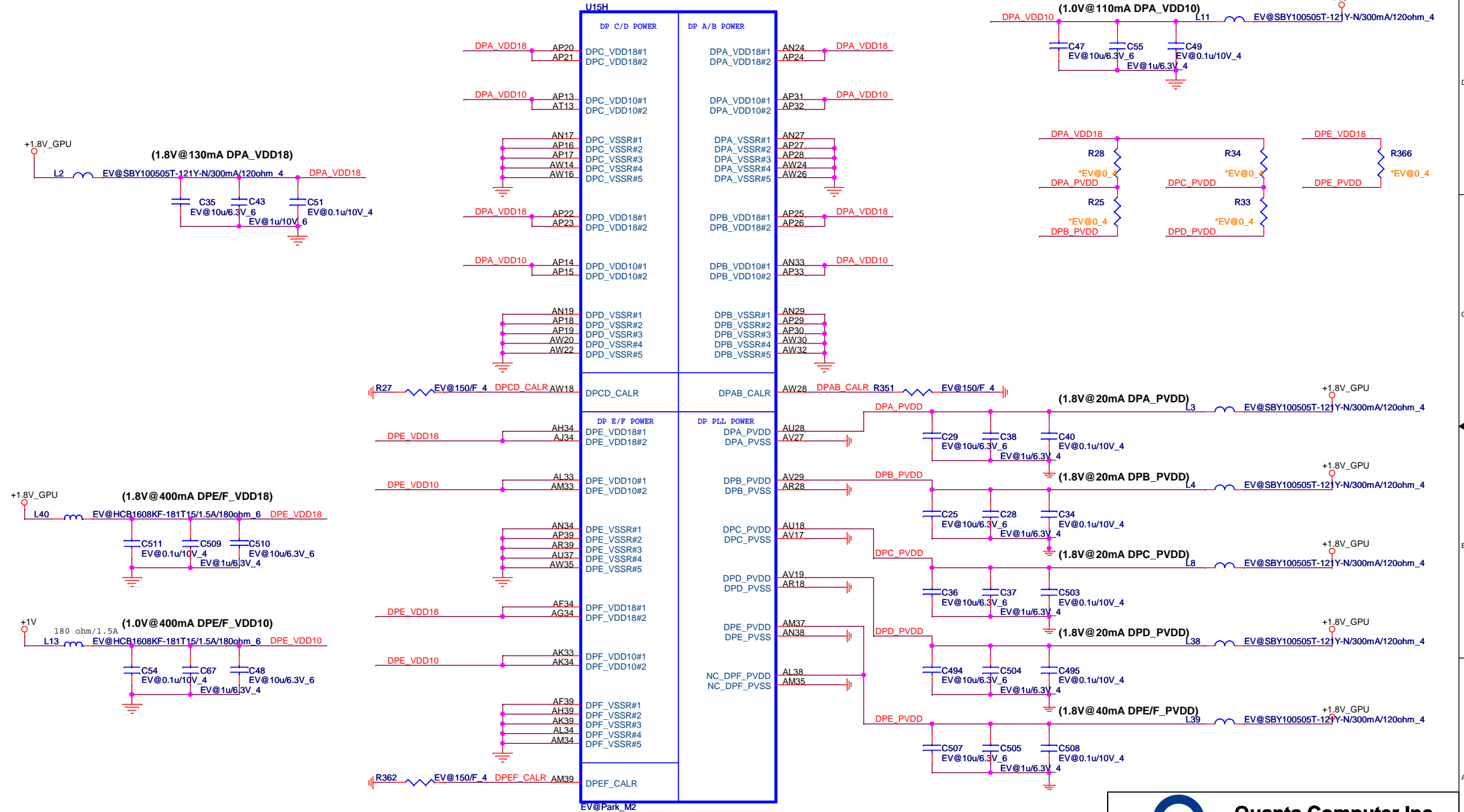
GPU +3V power

5/13 change the enable signal
Fine-tune Power-on sequence

PowerXpress control signal for Madison and Park only
If not used, can be disconnected.
PX_EN = LOW, turn on regulators for PowerXpress mode. An output high 3.3V will turn the regulators OFF. An output low 0V will turn the regulators ON. PX_EN outputs low (0V) by default.
If this signal is unused, it can be NC (not connected) or connected to ground.

Quanta Computer Inc.
PROJECT : ZQ9
Document Number: **Madison/Park M2 (PWR/GND)**
Rev 1A
Date: Tuesday, June 22, 2010 Sheet 19 of 45

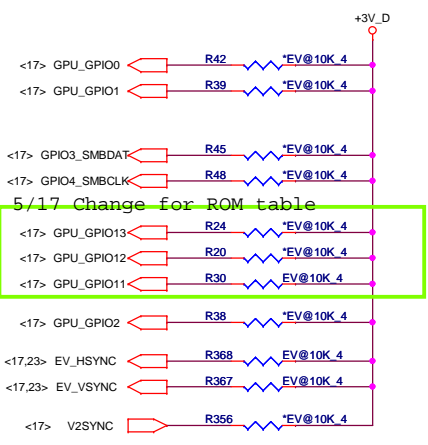
GPU_5(VGA)



Quanta Computer Inc.
PROJECT : ZQ9

Size	Document Number	Rev
	<Doc>	1A
Date:	Tuesday, June 22, 2010	Sheet 20 of 45

PIN STRAPS(VGA)



Size of the primary memory apertures	GPIO[13:11]
128 MB	000
256MB	001
64 MB	010
32 MB	011
More than 512 MB	Not Supported

CONFIGURATION STRAPS				
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET				
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	0	
ROMIDCFG[2:0]	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	001	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

EEPROM(VGA) 5/17 delete EEPROM

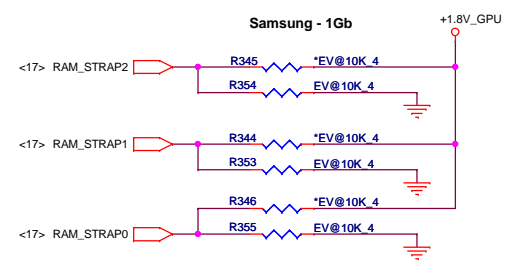
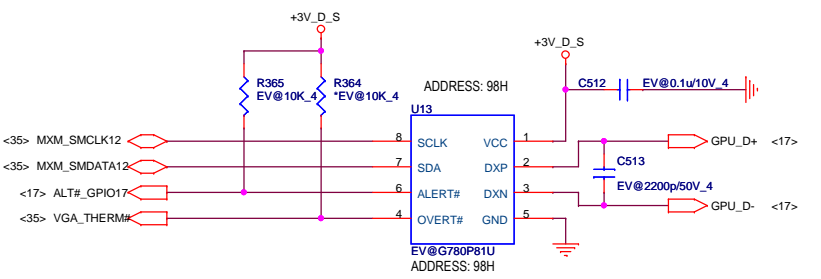
DDR3 Memory Aperture size(GPU)

DDR3 Memory size					
Vendor	Vendor P/N	STN B/S P/N	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix			1	1	0
	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	1	0	0
	H5TQ2G63BFR-12C	AKD5MGTTW03 (128M*16)	1	0	1
Samsung	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	0	0	0
	K4W2G1646B-HC12	AKD5MGTT500 (128m*16)	0	0	1
AMD	23EY2387MA12-SZ	AKD5LGGT700	0	1	0

Thermal Sensor(VGA)

Vendor	P/N
WINDBOND	AL83L771K01
GMT	AL000780000

USD0.16



RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.

Quanta Computer Inc.
PROJECT : ZQ9

Size Document Number Strip/Thermal Rev 1A
Date: Tuesday, June 22, 2010 Sheet 21 of 45

CHANNEL B: 512MB DDR3 (16*64M*4pcs)

Park, M92M Use Channel B Memory Interface Only

<18> VMB_DM[63..0] VMB_DM[63..0]

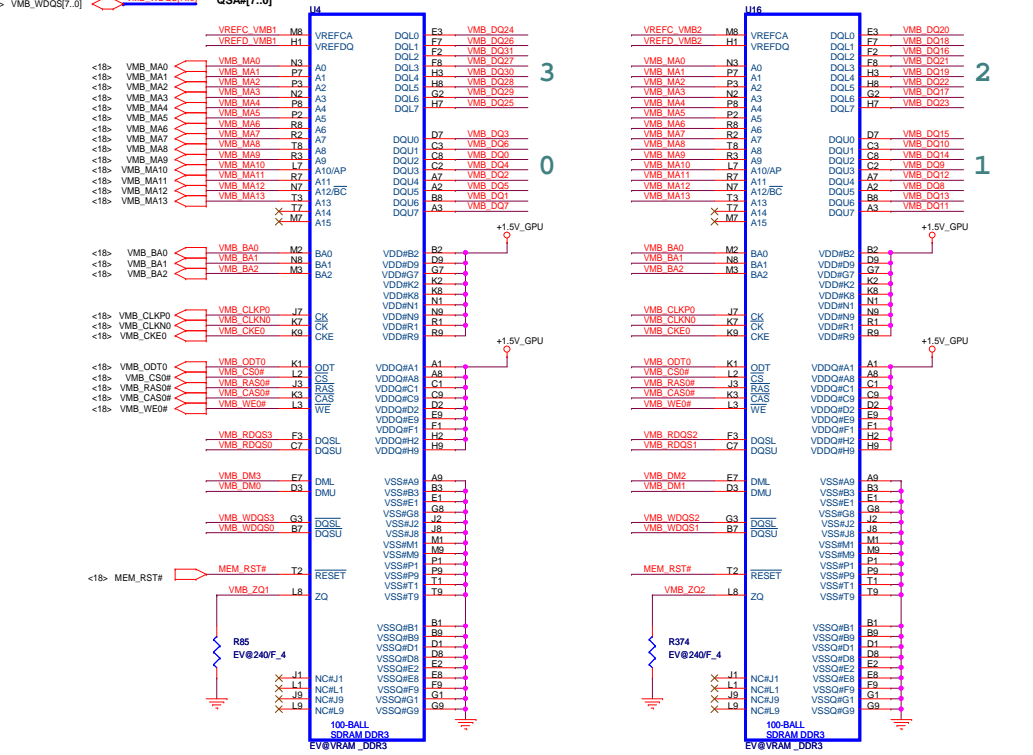
<18> VMB_DM[7..0] VMB_DM[7..0]

<18> VMB_RDQS[7..0] VMB_RDQS[7..0]

<18> VMB_WDQS[7..0] VMB_WDQS[7..0]

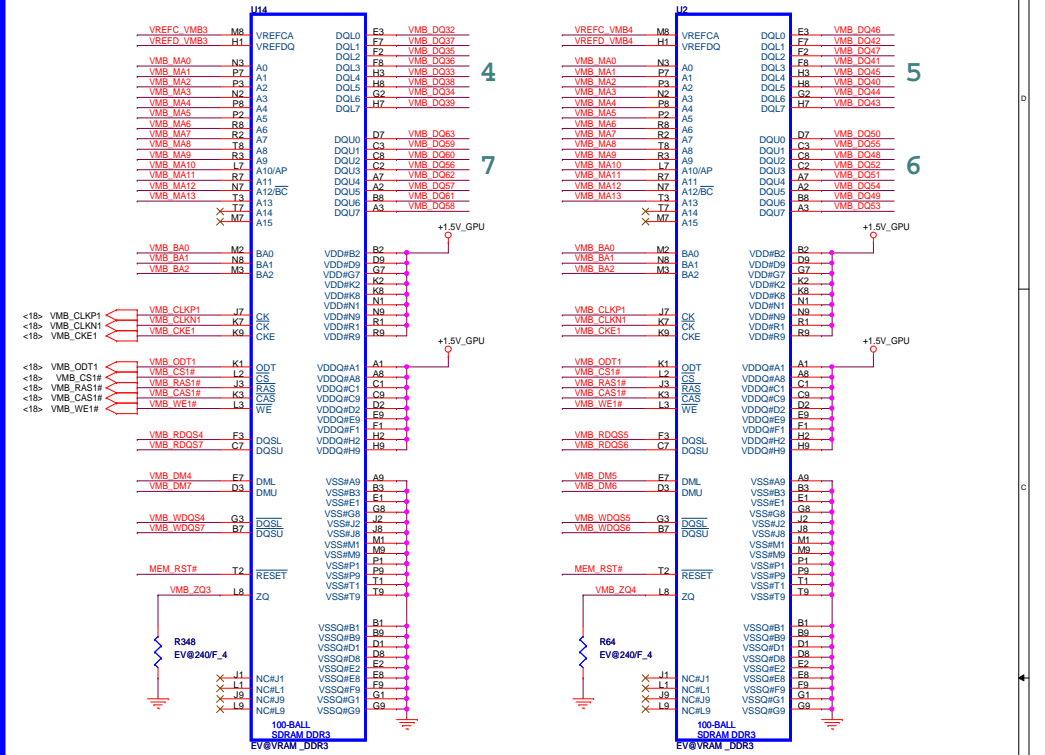
QSA#[7..0] QSA#[7..0]

QSA#[7..0] QSA#[7..0]



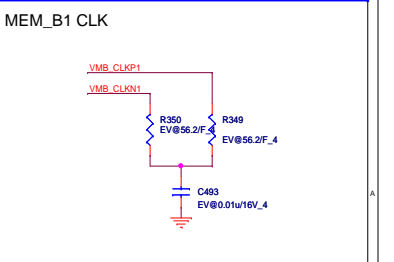
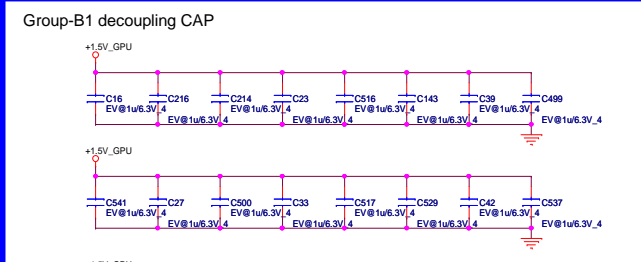
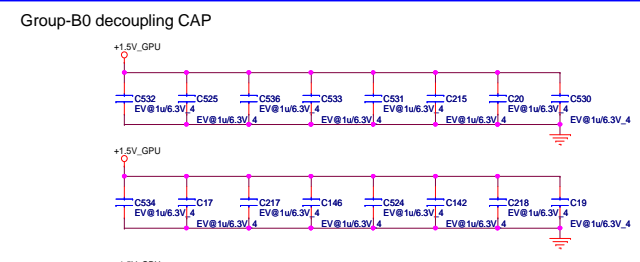
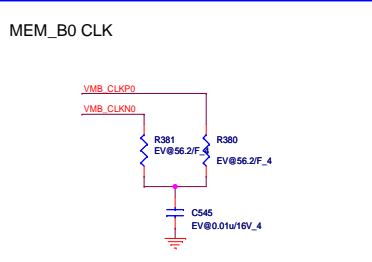
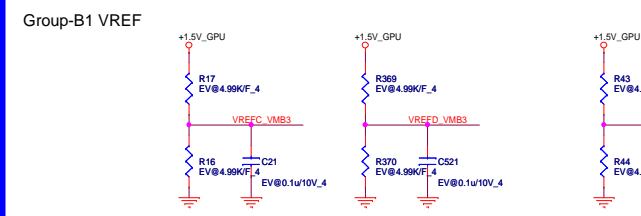
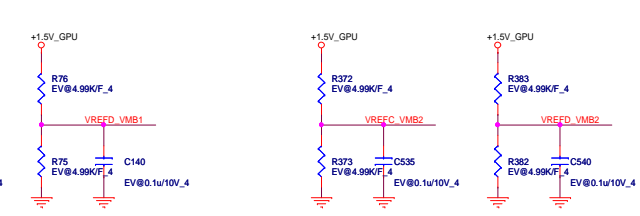
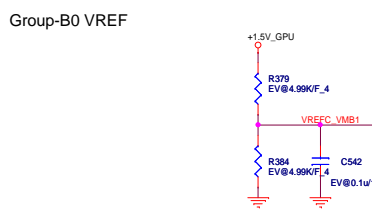
BOT Down

TOP Down



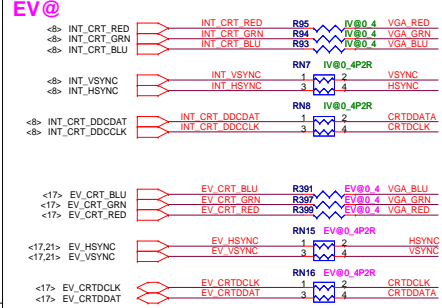
TOP Up

BOT Up

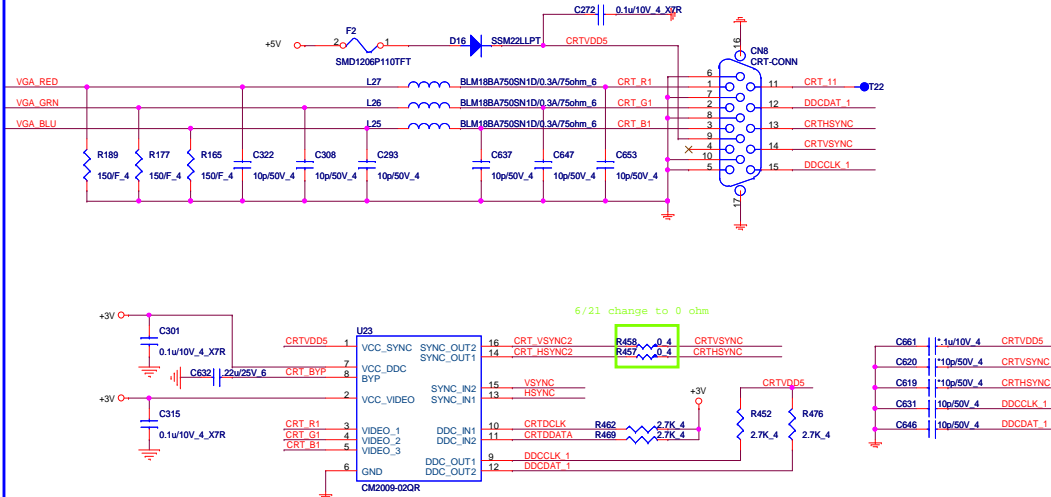


CRT Switch

IV@ 0_ohm Resistor place close to Joint-Point



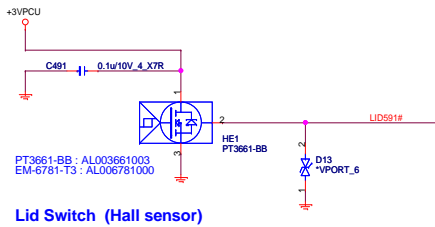
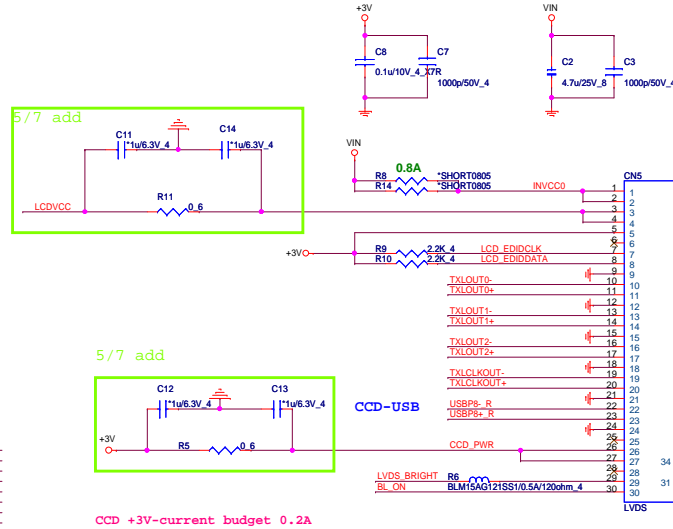
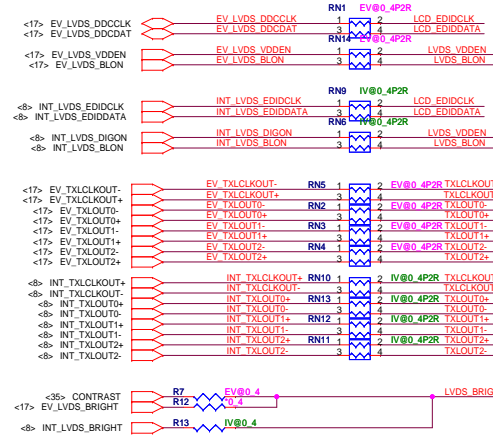
CRT



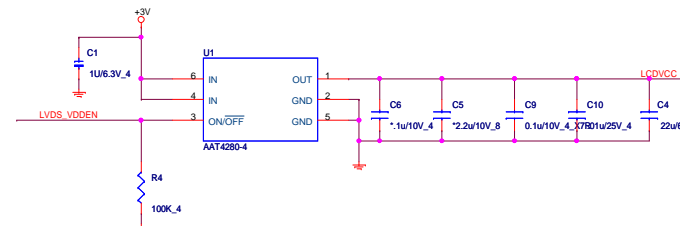
LVDS

LVDS

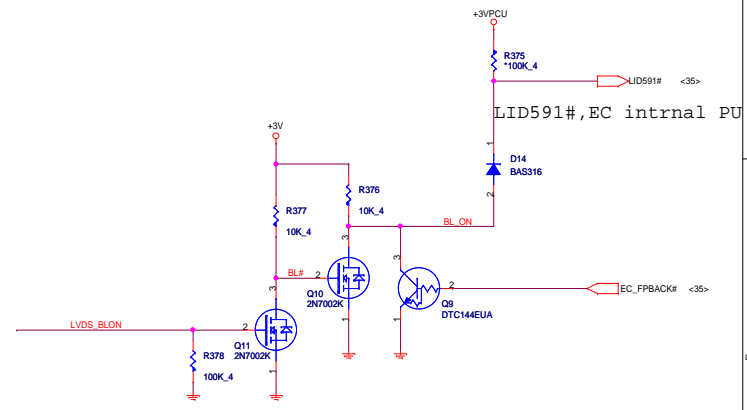
0_ohm Resistor place close to Joint-Point



LCD Power

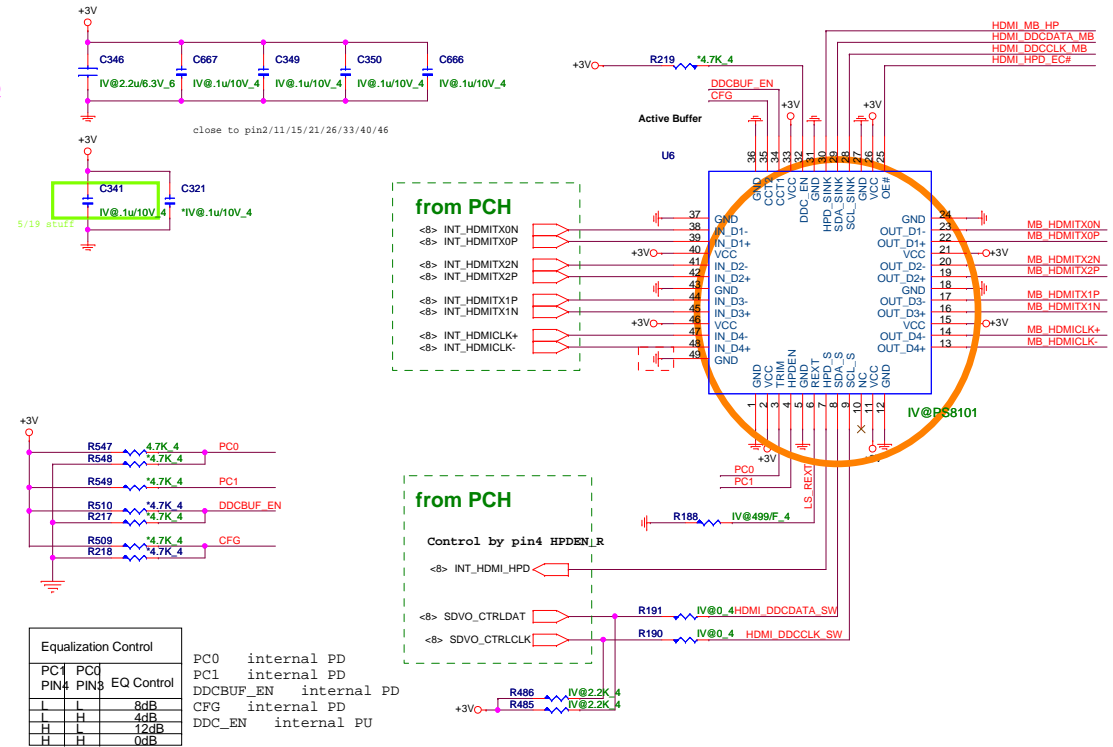


Backlight Control

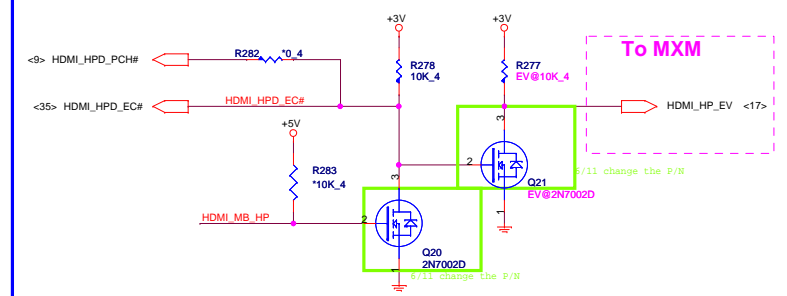


I@ HDMI LEVEL SHIFTER

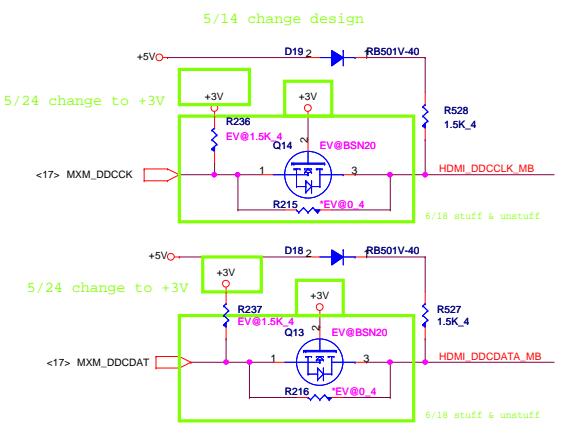
IV@
EV@



SW@HDMI-detect



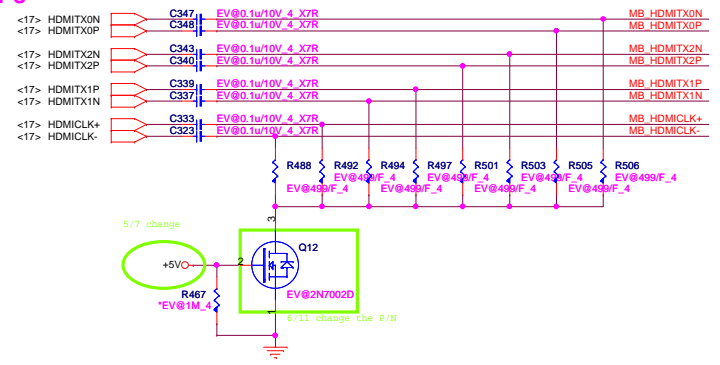
I2C



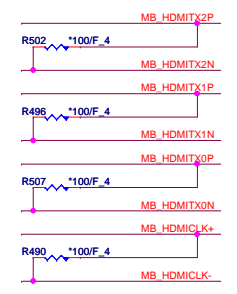
AC-coupling CAP place close to HDMI-connector

Switchable Graphic HDMI source

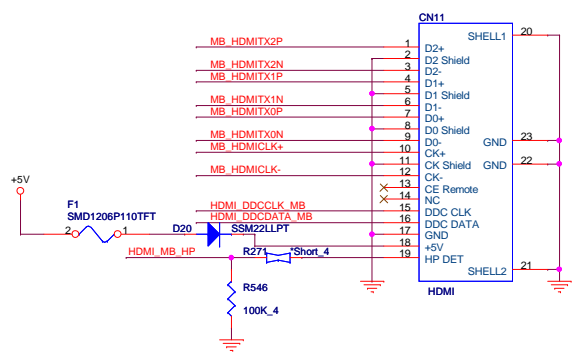
From GPU



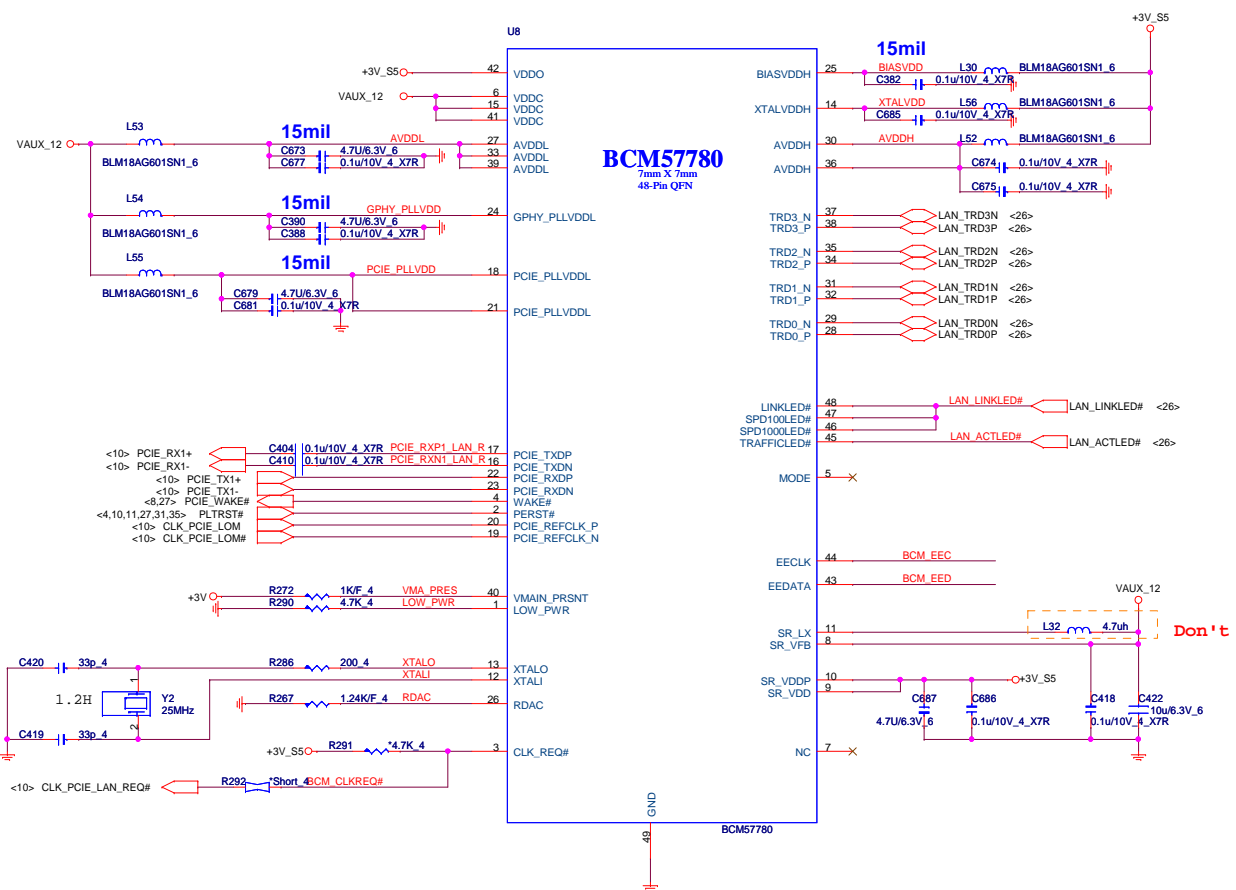
EMI



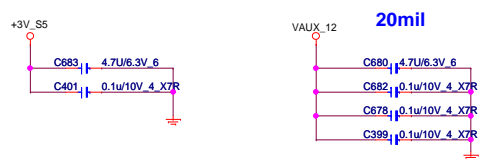
HDMI connector



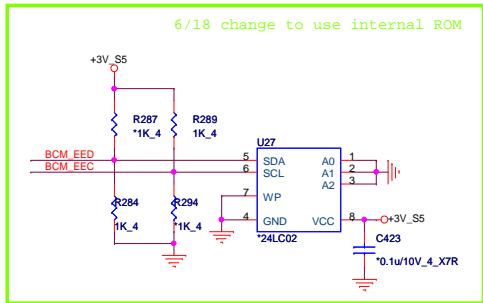
Giga-LAN BCM57780



LAN POWER



EEPROM

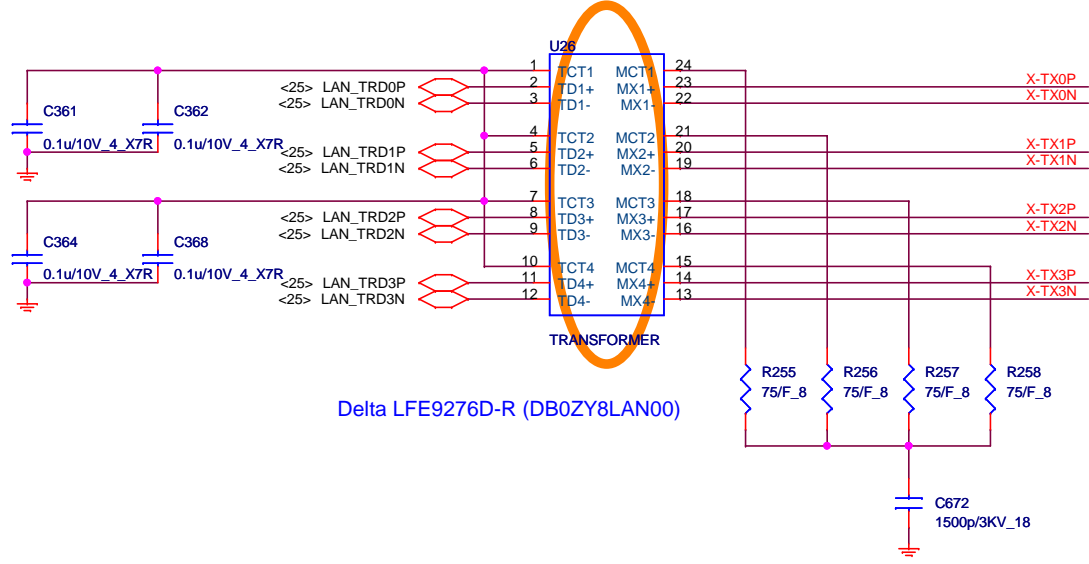


EEPROM Strapping

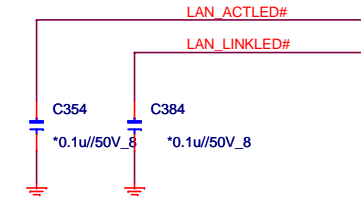
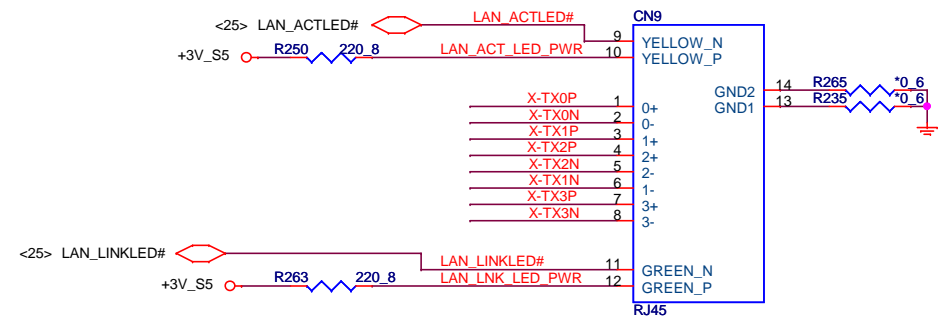
EEPROM Type	EECLK	EEDATA
24LC02	1	1
Internal	1	0

A version Still mount the EEPROM

TRANSFORMER



Delta LFE9276D-R (DB0ZY8LAN00)



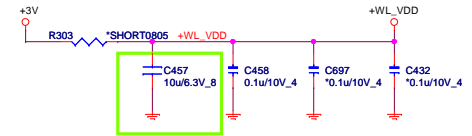
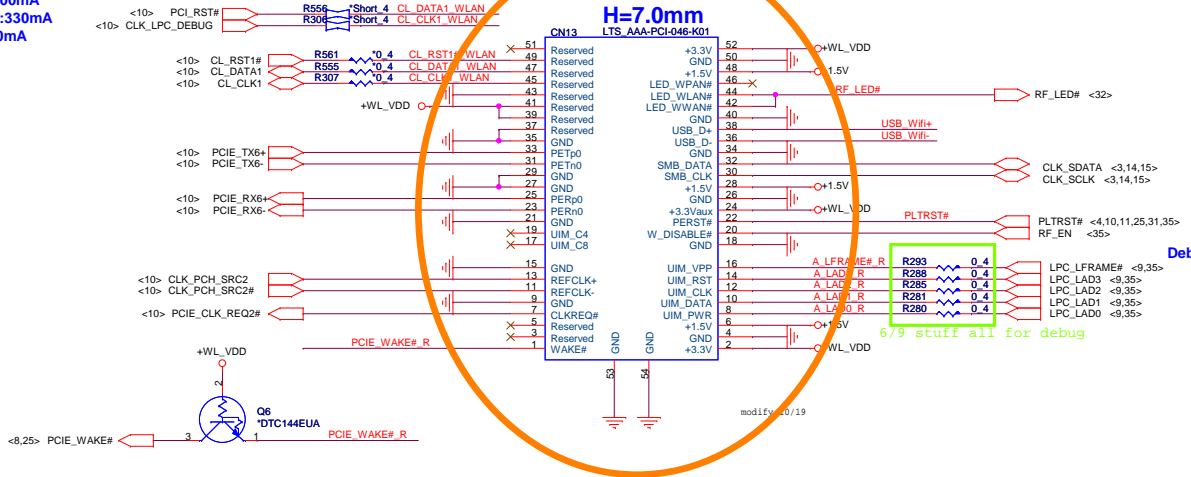
MINI-CARD WLAN(MPC)

+3.3V: 1000mA
 +3.3Vaux: 330mA
 +1.5V: 500mA

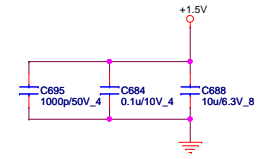
Debug

Check LED signal. (active high or low)

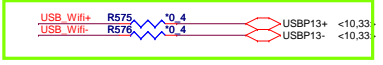
H=7.0mm
 LTS AAA-PCI-046-K01




5/13 change to 6.3V



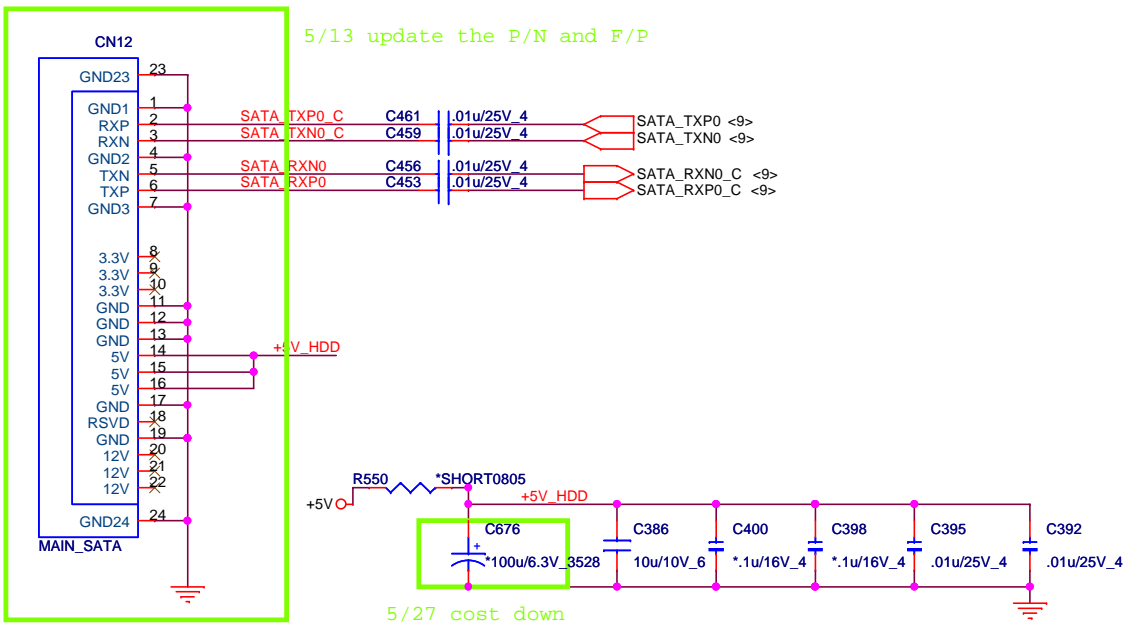
Debug



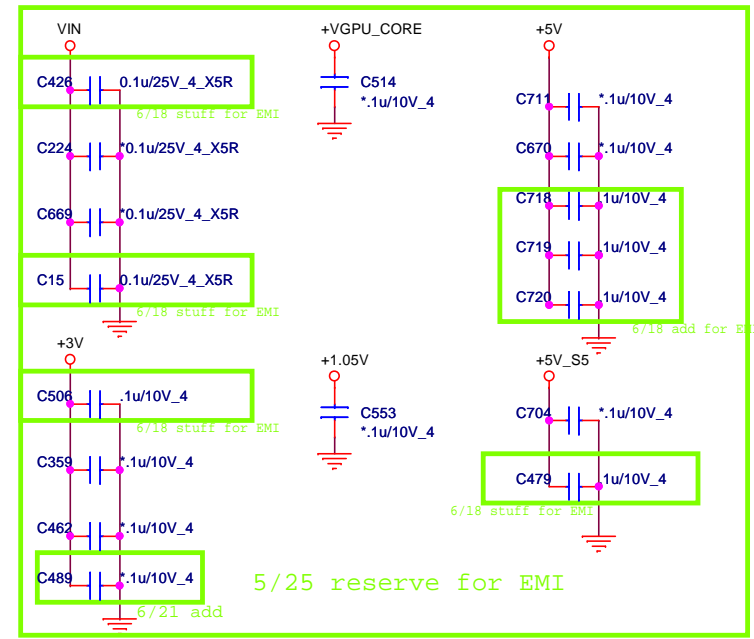
 Quanta Computer Inc. PROJECT : ZQ9		Rev 1A
Date: Tuesday, June 22, 2010	Sheet 27 of 45	

MAIN SATA HDD

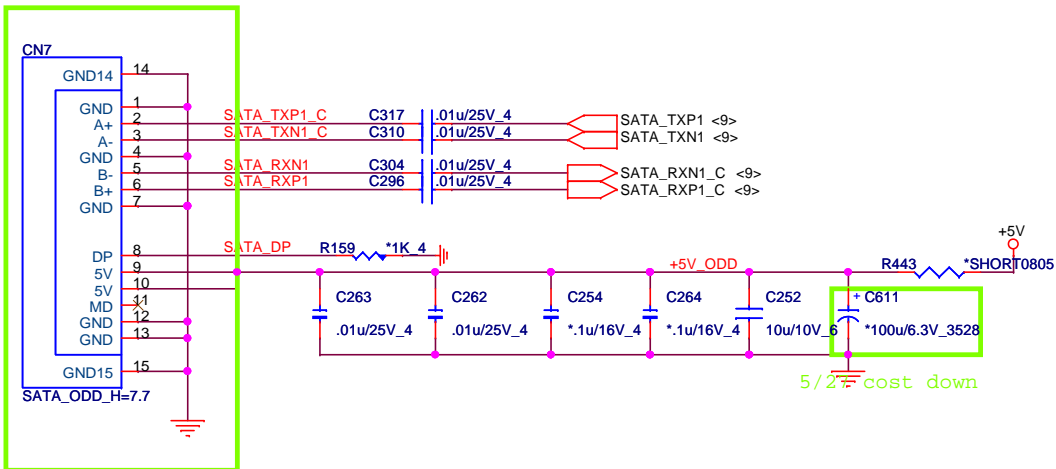
5/13 update the P/N and F/P



EE RETURN-PATH CAPACITORS



ODD (SATA)



5/26 change the footprint



Quanta Computer Inc.

PROJECT : ZQ9

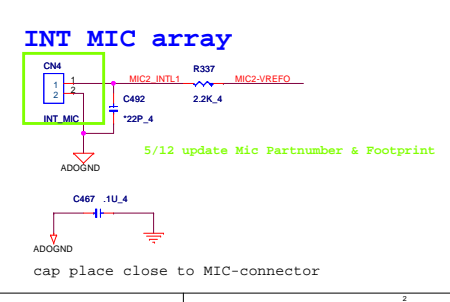
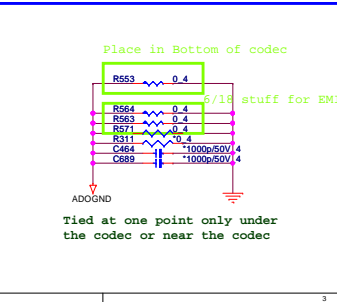
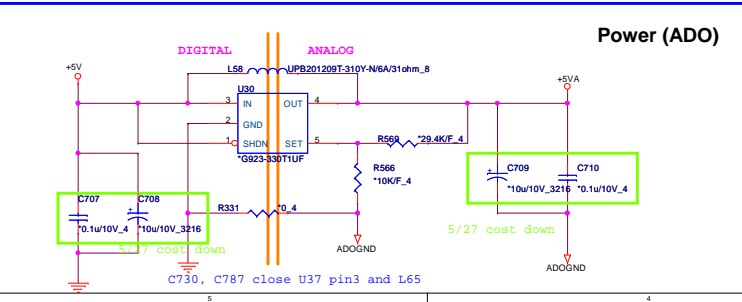
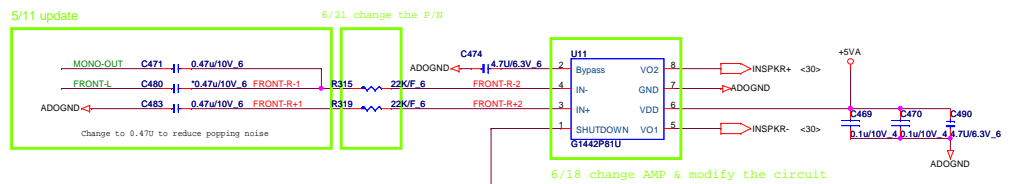
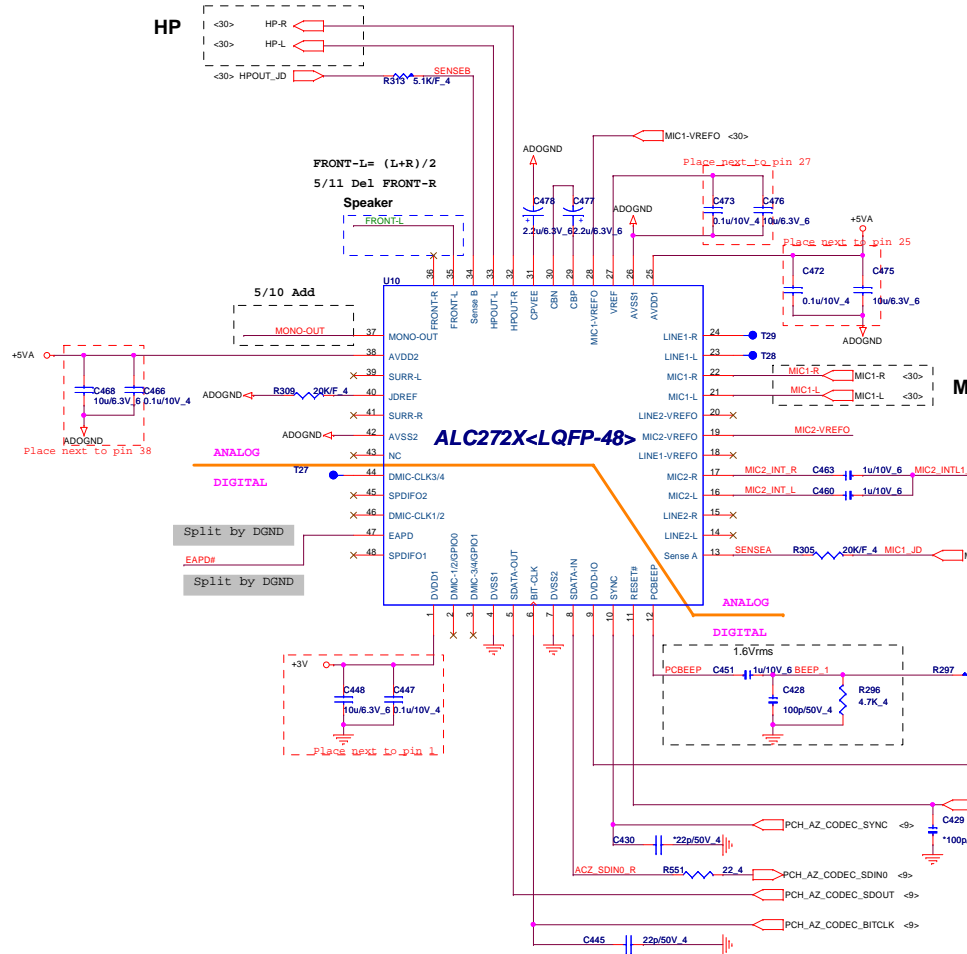
Size	Document Number	Rev
	SATA-HDD/ODD/USB-ESATA	1A

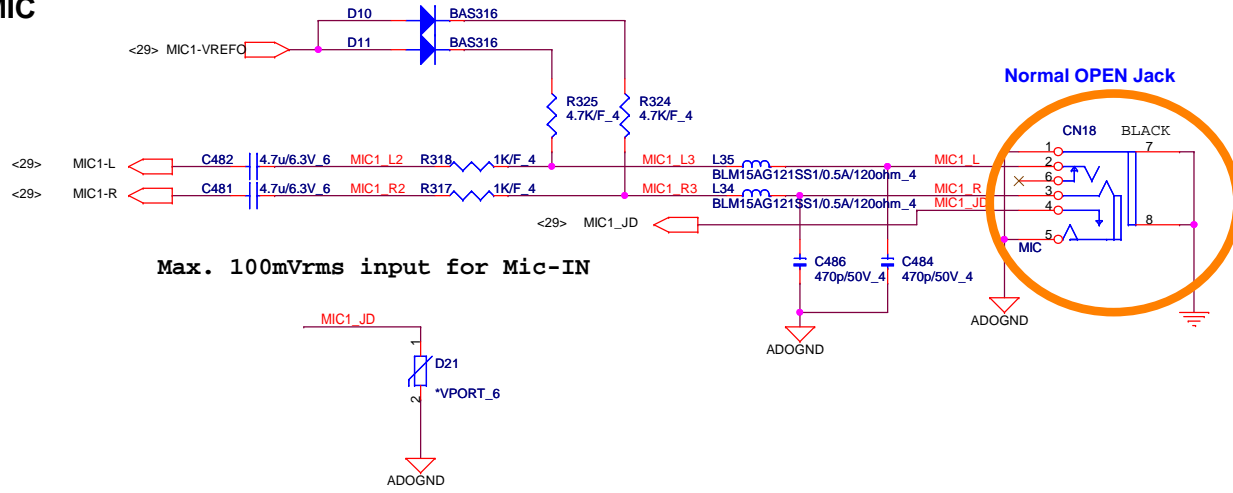
Date: Tuesday, June 22, 2010 Sheet 28 of 45

Codec(ADO)

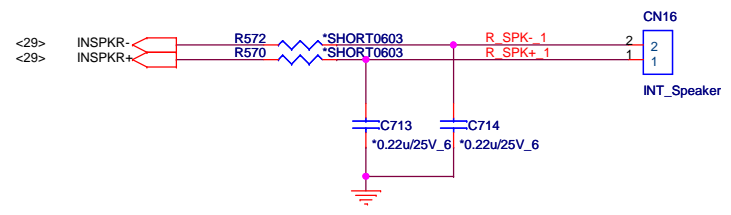
HP

MUTE(AMP)

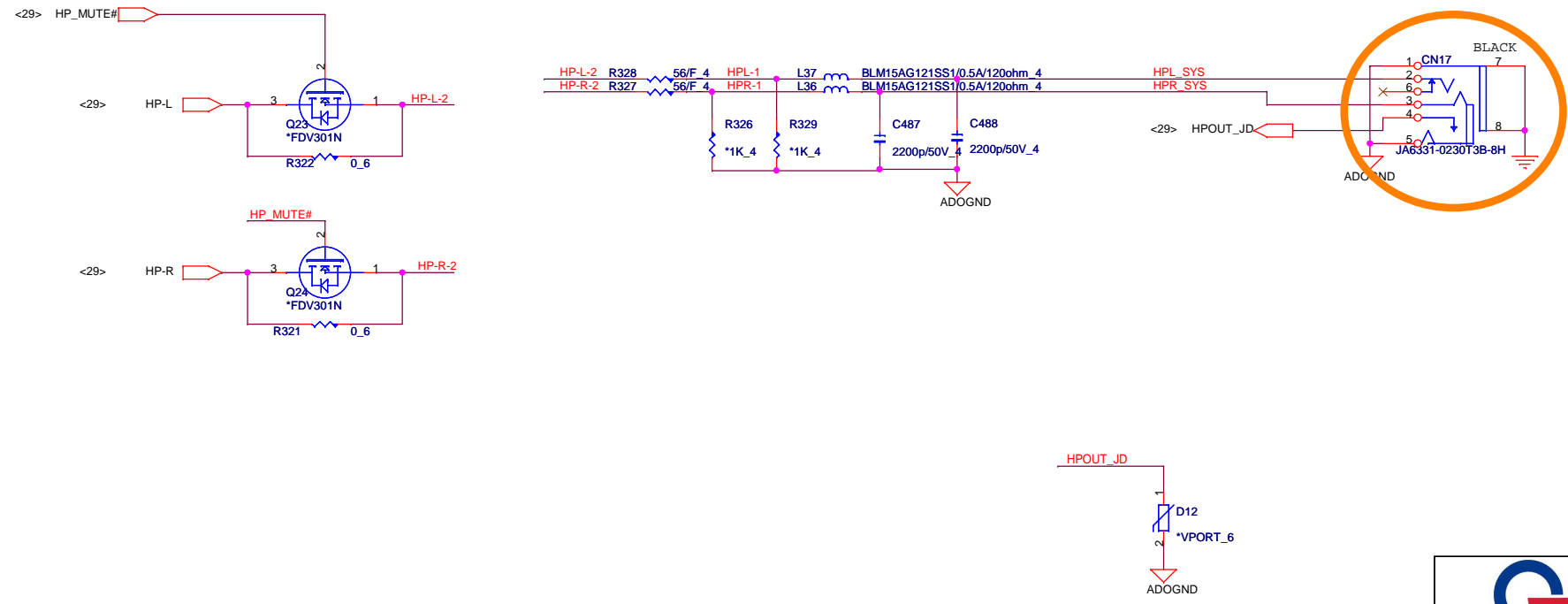




Internal Speaker



HP/SPDIF

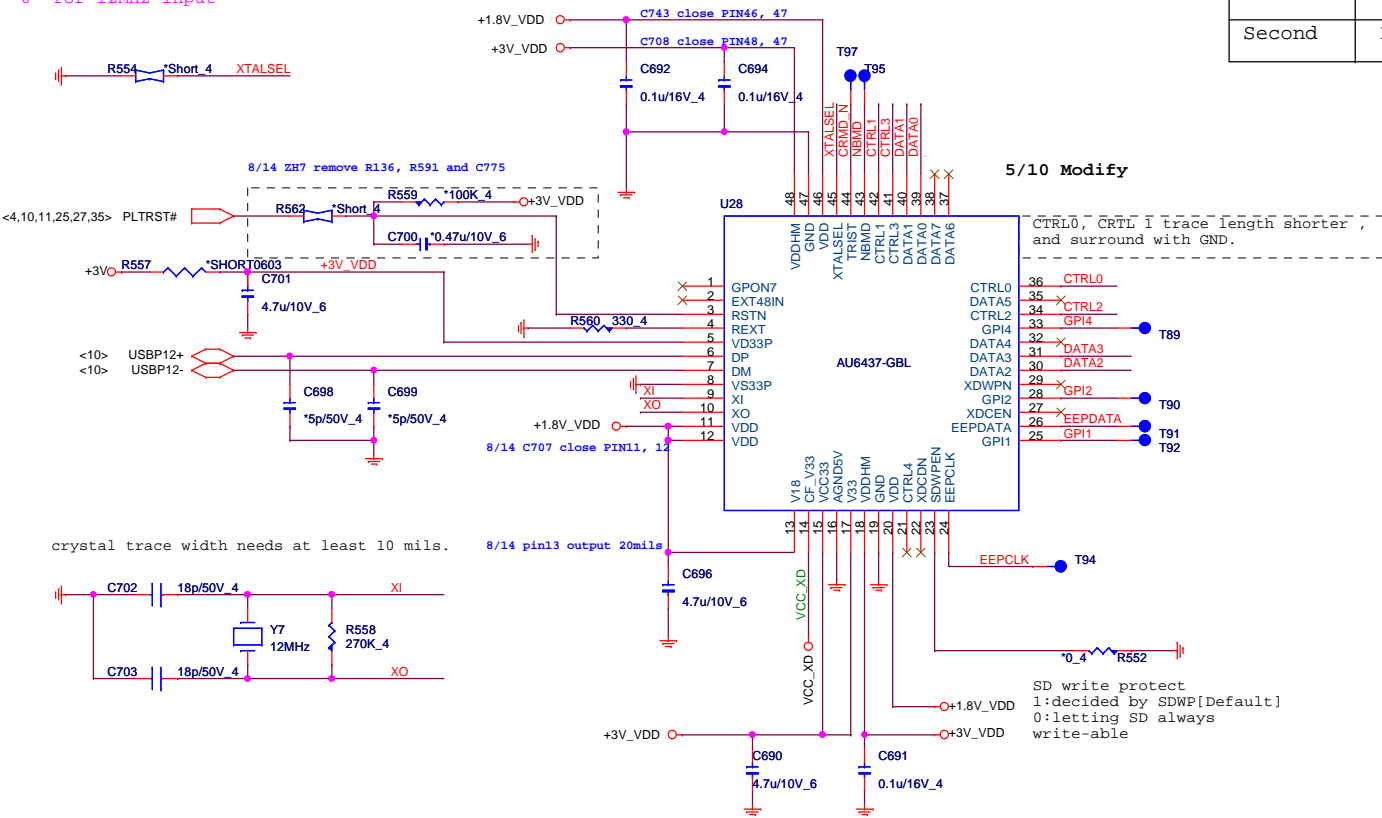


		Quanta Computer Inc.	
		PROJECT : ZQ9	
Size	Document Number	AMP /AUDIO JACK CONN	
Date: Tuesday, June 22, 2010	Sheet	30	of 45
			Rev 1A

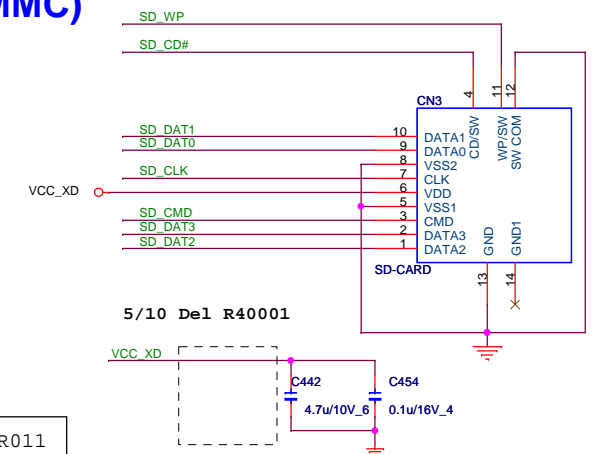
CARD READER Controller

2 IN 1 CARD READER (SD/MMC)

Clock input selection
 '1' for 48MHz input [Default, Internal PU]
 '0' for 12MHz input



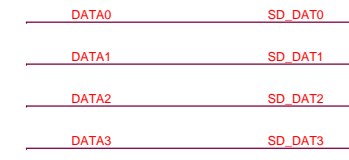
Main	DFHS11FR011
Second	DFHS11FR033



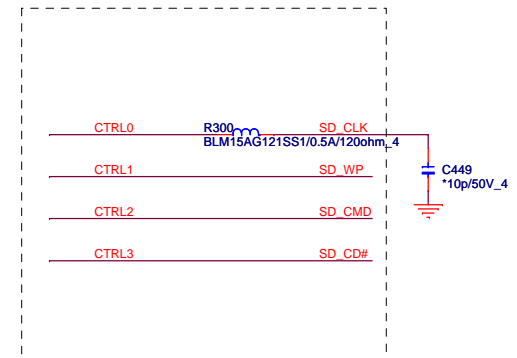
5/10 Del R40001

Close to CN14 pin 14 & pin23
 4.7u CAP close to pin23

5/10 change Card Redaer conn
 footprint sdcard-sdsn09-08-xa-11p-smt



Close to connector



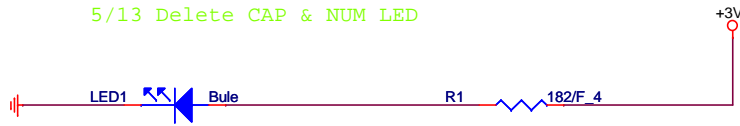
PROJECT : ZQ5
Quanta Computer Inc.

Size	Document Number AU6433 CardReader	Rev 1A
Date: Tuesday, June 22, 2010 Sheet 31 of 43		

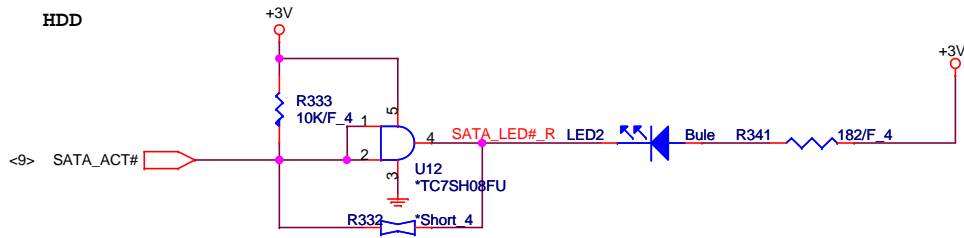
LED

5/13 Delete CAP & NUM LED

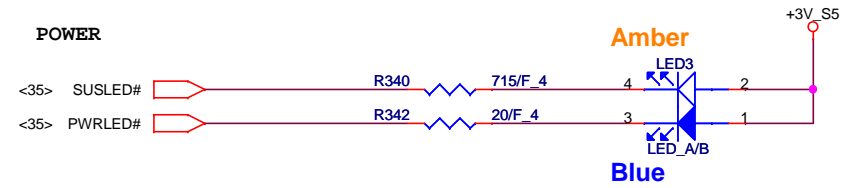
Power LED



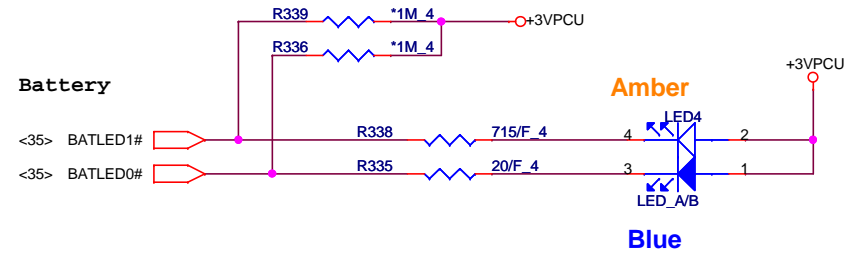
HDD



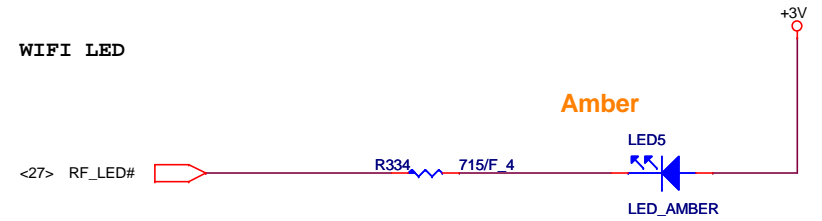
POWER



Battery



WIFI LED



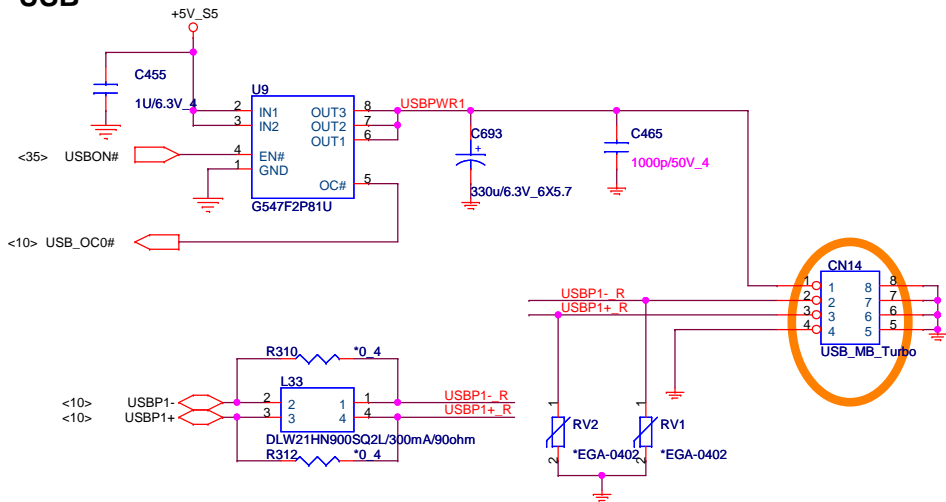
Quanta Computer Inc.

PROJECT : ZQ9

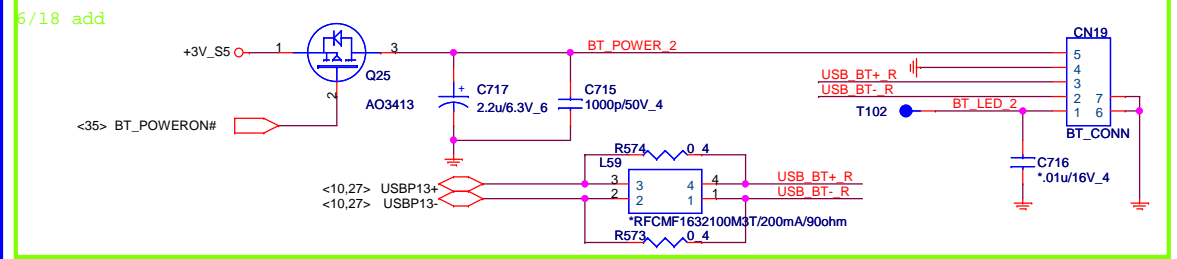
Size	Document Number	Rev
	POWER/MMB/LAUNCH/LED	1A

Date: Tuesday, June 22, 2010 Sheet 32 of 45

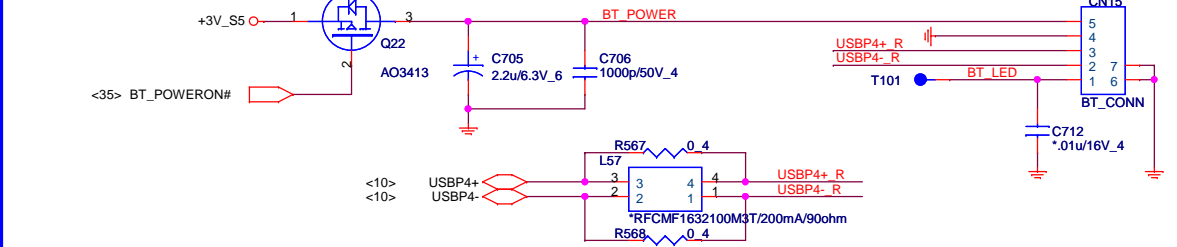
USB



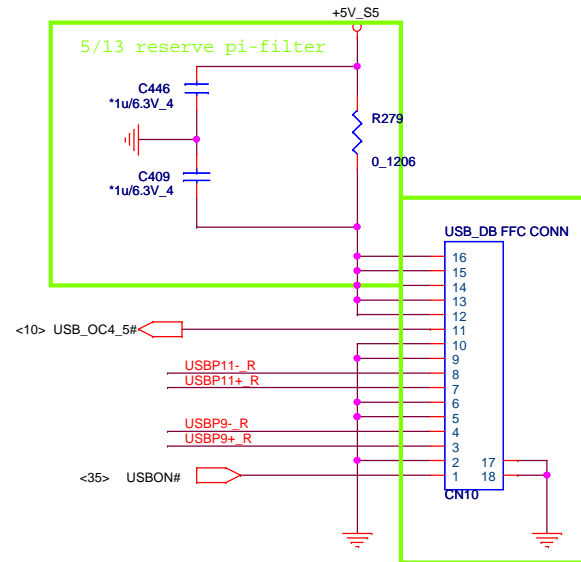
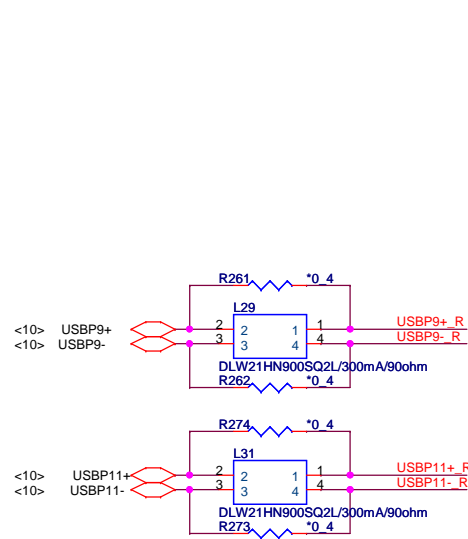
BLUETOOTH CONNECTOR for 2.0




BLUETOOTH CONNECTOR for 3.0



USB/B



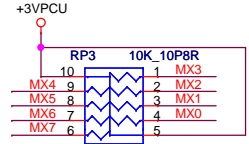
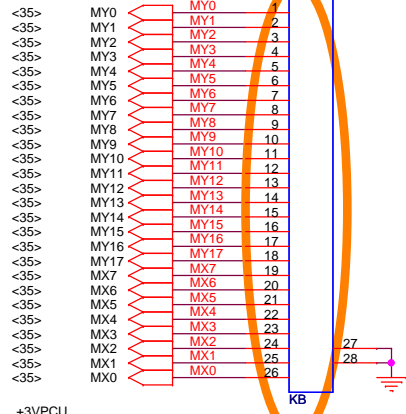
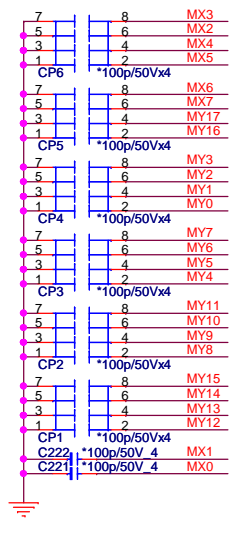
5/11 update the footprint



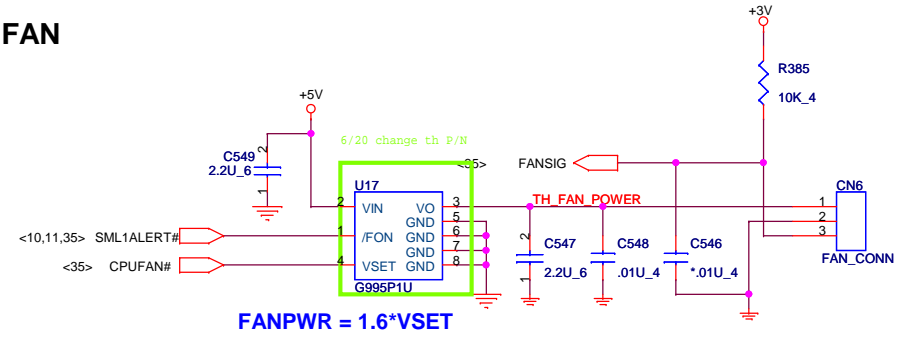
Quanta Computer Inc.
PROJECT : ZQ9

Size	Document Number	Rev
	USB/ BT	1A
Date:	Tuesday, June 22, 2010	Sheet 33 of 45

K/B

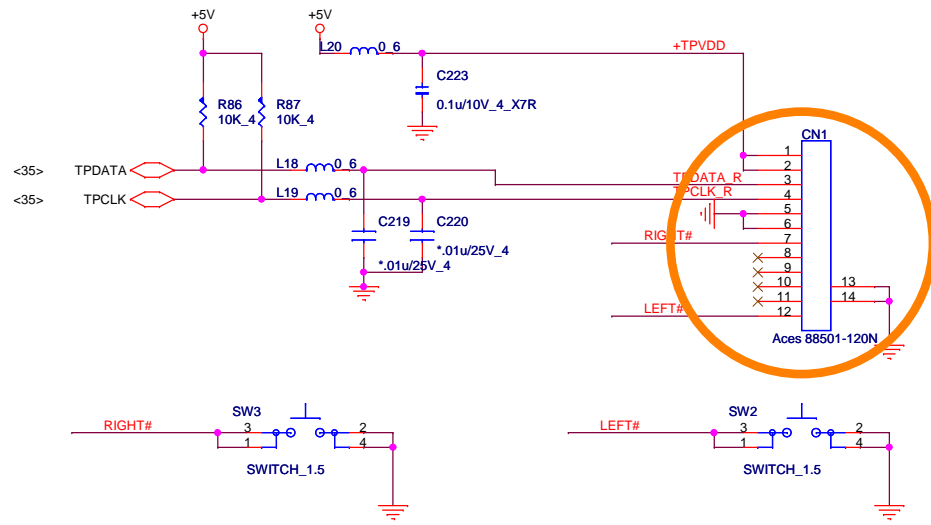


CPU FAN

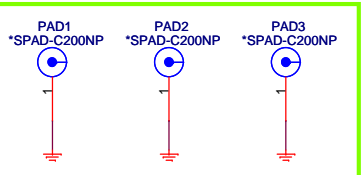
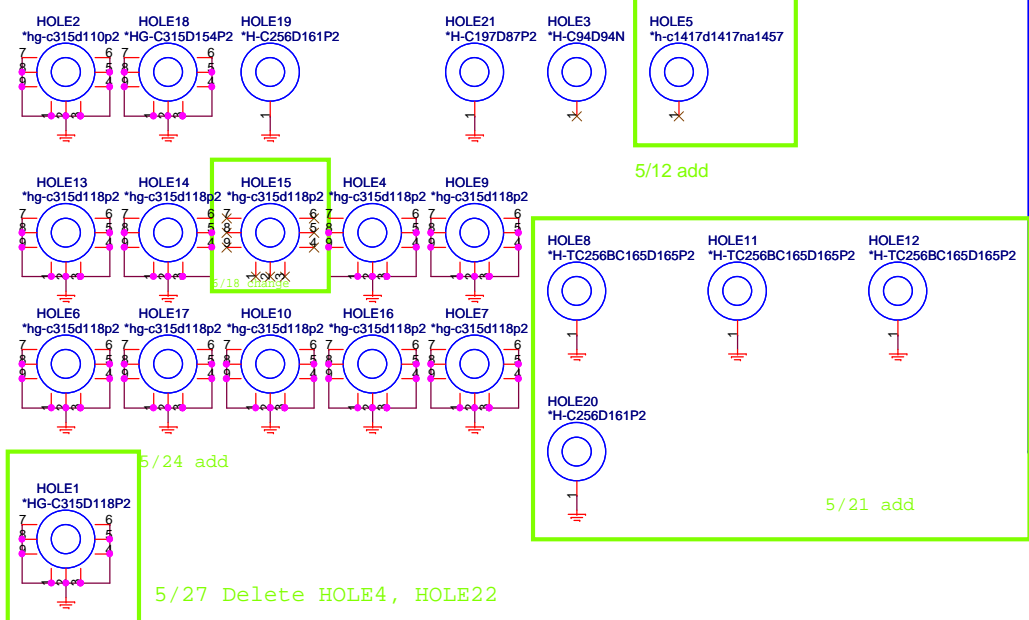



FANPWR = 1.6*VSET

TOUCHPAD & Switch CONN.



HOLE

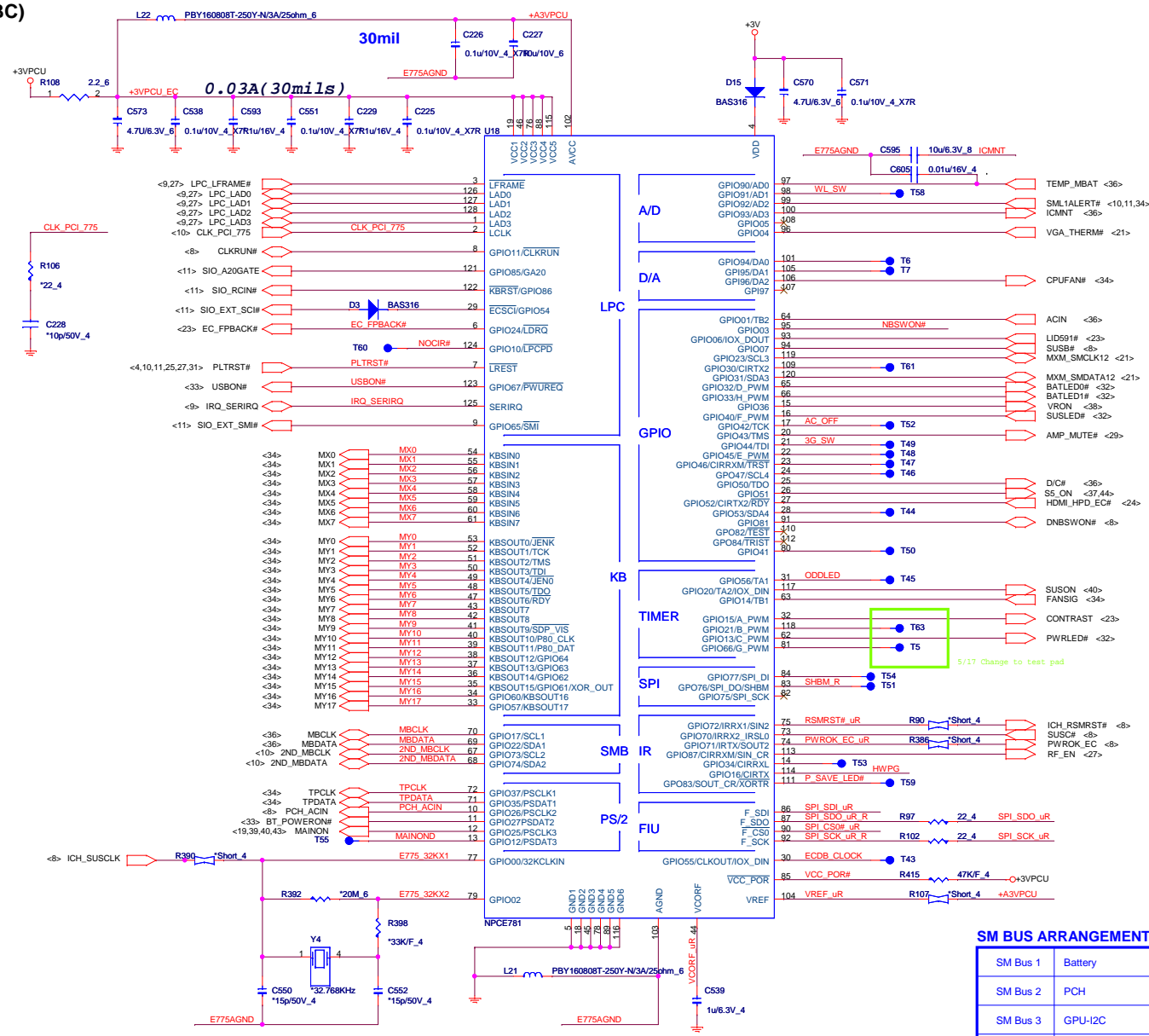




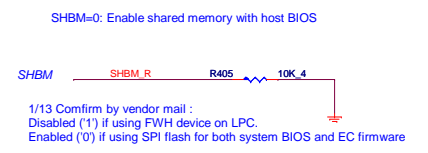
Quanta Computer Inc.
PROJECT : ZQ9

Size	Document Number	Rev
	KB/FAN/TP+FP	1A
Date:	Tuesday, June 22, 2010	Sheet 34 of 45

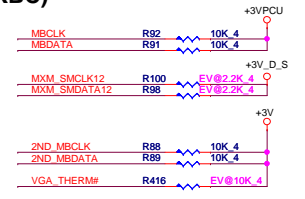
EC(KBC)



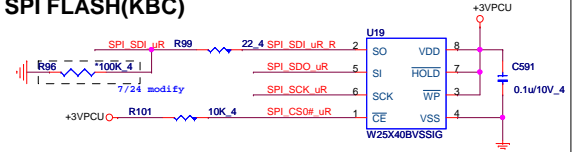
I/O ADDRESS SETTING(KBC)



SM BUS PU(KBC)

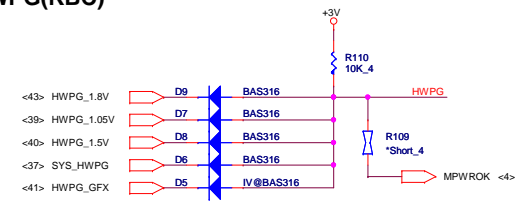


SPI FLASH(KBC)



1/13 Confirm by vendor mail :
If the Southbridge enables "Long Wait Abort" by default, the flash device should be 50MHz (or faster)

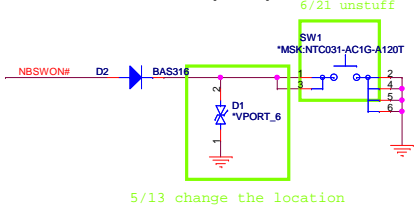
HWPG(KBC)



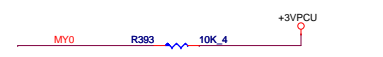
SM BUS ARRANGEMENT TABLE

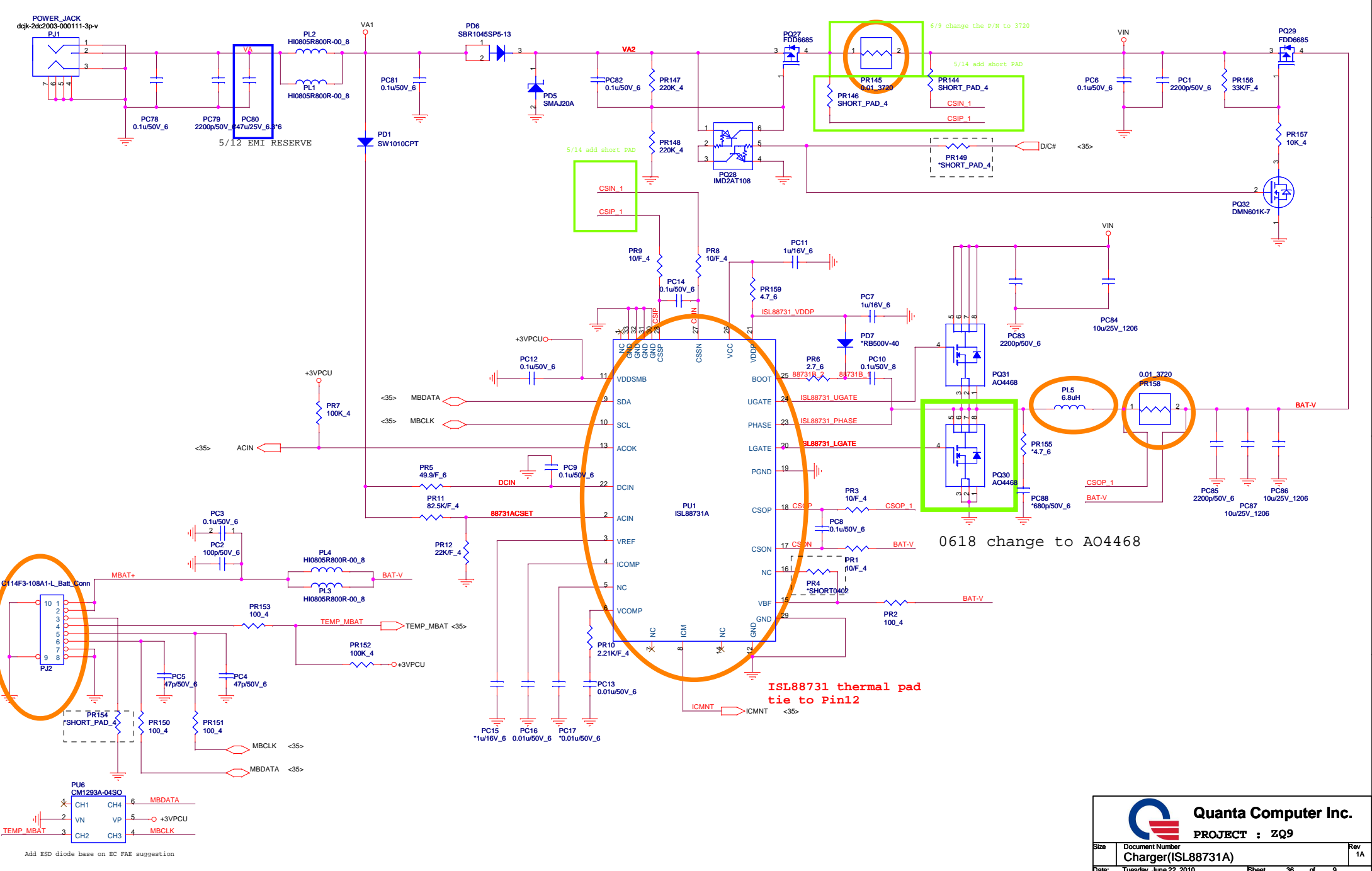
SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	GPU-I2C
SM Bus 4	N/A

POWER-ON Switch(KBC)




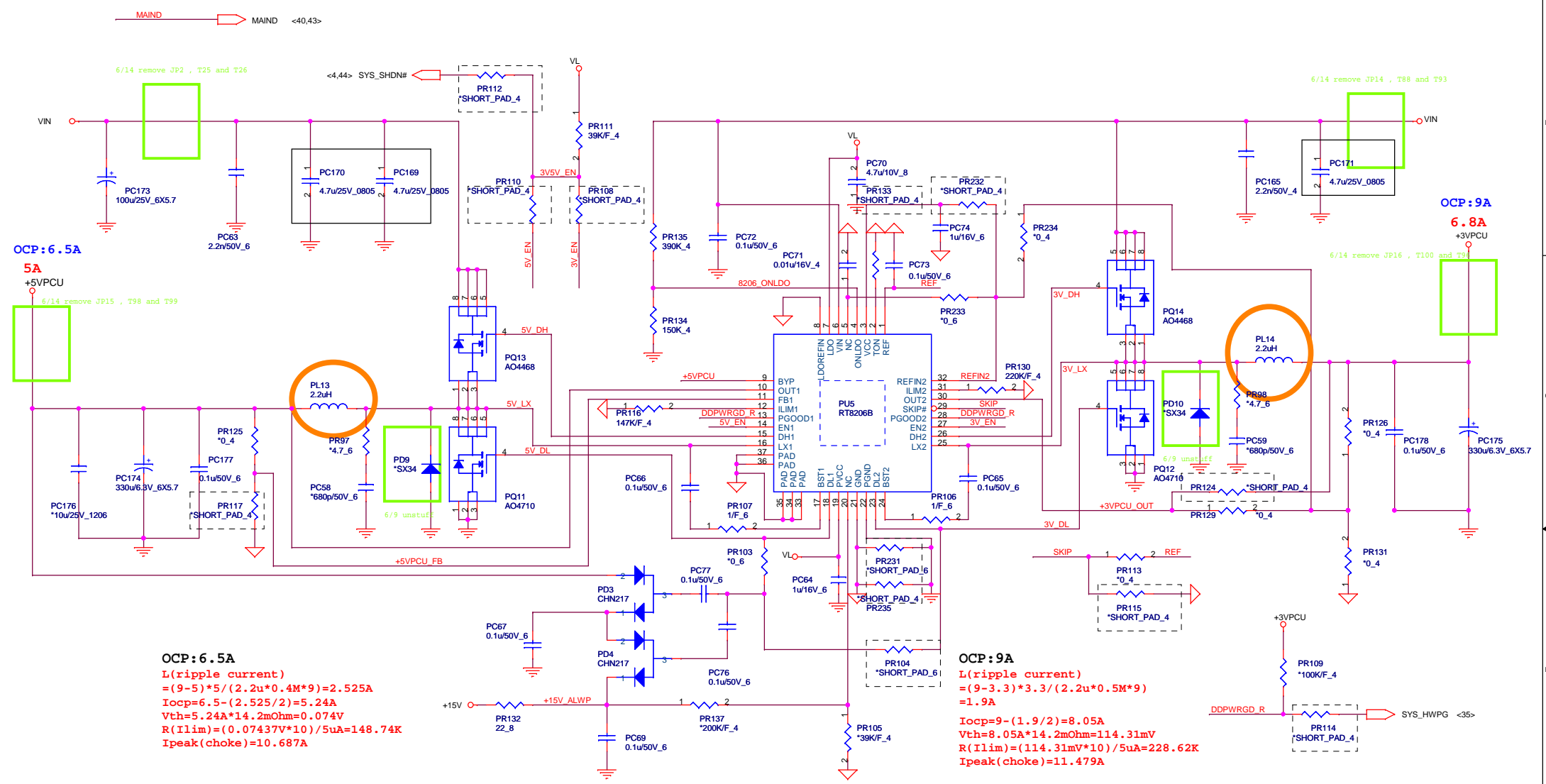
INTERNAL KEYBOARD STRIP SET(KBC)



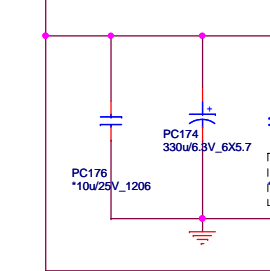
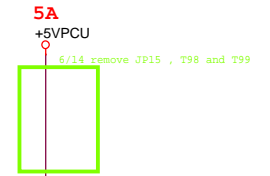


Add ESD diode base on EC FAE suggestion

 Quanta Computer Inc. PROJECT : ZQ9		Rev
		1A
Size	Document Number	
Charger (ISL88731A)		
Date:	Tuesday, June 22, 2010	Sheet 36 of 9



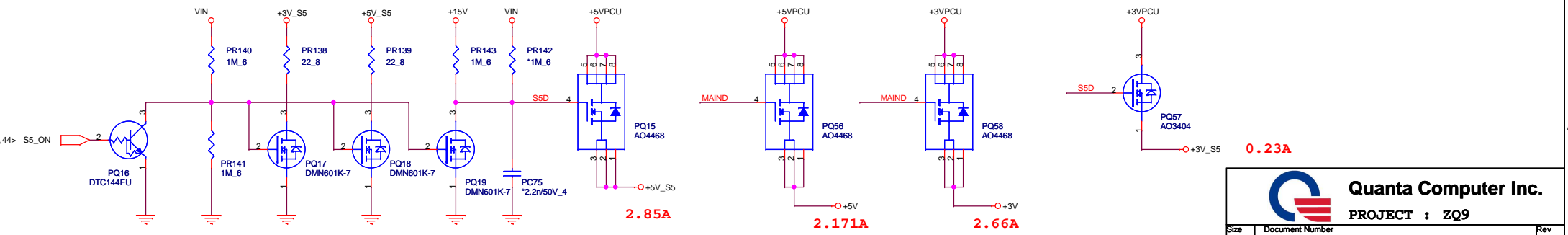
OCP : 6.5A



OCP : 6.5A
 $L(\text{ripple current}) = (9-5) * 5 / (2.2u * 0.4m * 9) = 2.525A$
 $I_{ocp} = 6.5 - (2.525 / 2) = 5.24A$
 $V_{th} = 5.24A * 14.2m\Omega = 0.074V$
 $R(I_{lim}) = (0.07437V * 10) / 5uA = 148.74K$
 $I_{peak}(\text{choke}) = 10.687A$

OCP : 9A
 $L(\text{ripple current}) = (9-3.3) * 3.3 / (2.2u * 0.5m * 9) = 1.9A$
 $I_{ocp} = 9 - (1.9 / 2) = 8.05A$
 $V_{th} = 8.05A * 14.2m\Omega = 114.31mV$
 $R(I_{lim}) = (114.31mV * 10) / 5uA = 228.62K$
 $I_{peak}(\text{choke}) = 11.479A$

OCP : 9A
 +3VPCU
 6.8A



2.85A

2.171A

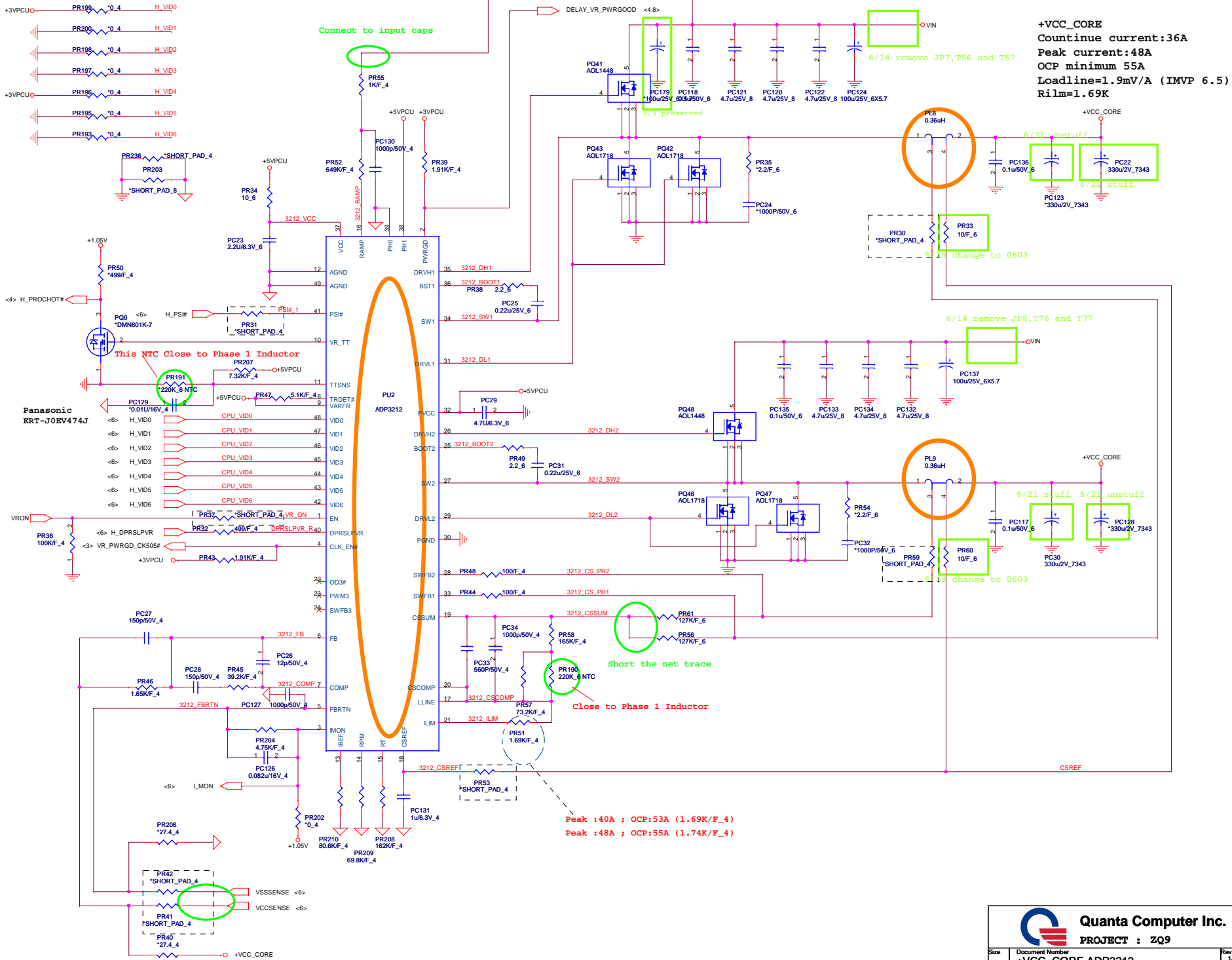
2.66A

0.23A

Quanta Computer Inc.
PROJECT : ZQ9

Size	Document Number	Rev
	SYSTEM 5V/3V (RT8206)	1A
Date: Tuesday, June 22, 2010		Sheet 37 of 9

VID 1.2875V



+VCC_CORE
 Continue current:36A
 Peak current:48A
 OCP minimum 55A
 Loadline=1.9mV/A (IMVP 6.5)
 Rilm=1.69K

Connect to input caps

6/14 remove JP7,T56 and T57

6/9 preserved

PLB 0.36uH

6/21 unstuff

6/21 stuff

5/19 change to 0603

6/14 remove JP8,T76 and T77

PL9 0.36uH

6/21 stuff

6/21 unstuff

5/19 change to 0603

Short the net trace

Close to Phase 1 Inductor

Peak :40A ; OCP:53A (1.69K/F_4)
 Peak :48A ; OCP:55A (1.74K/F_4)

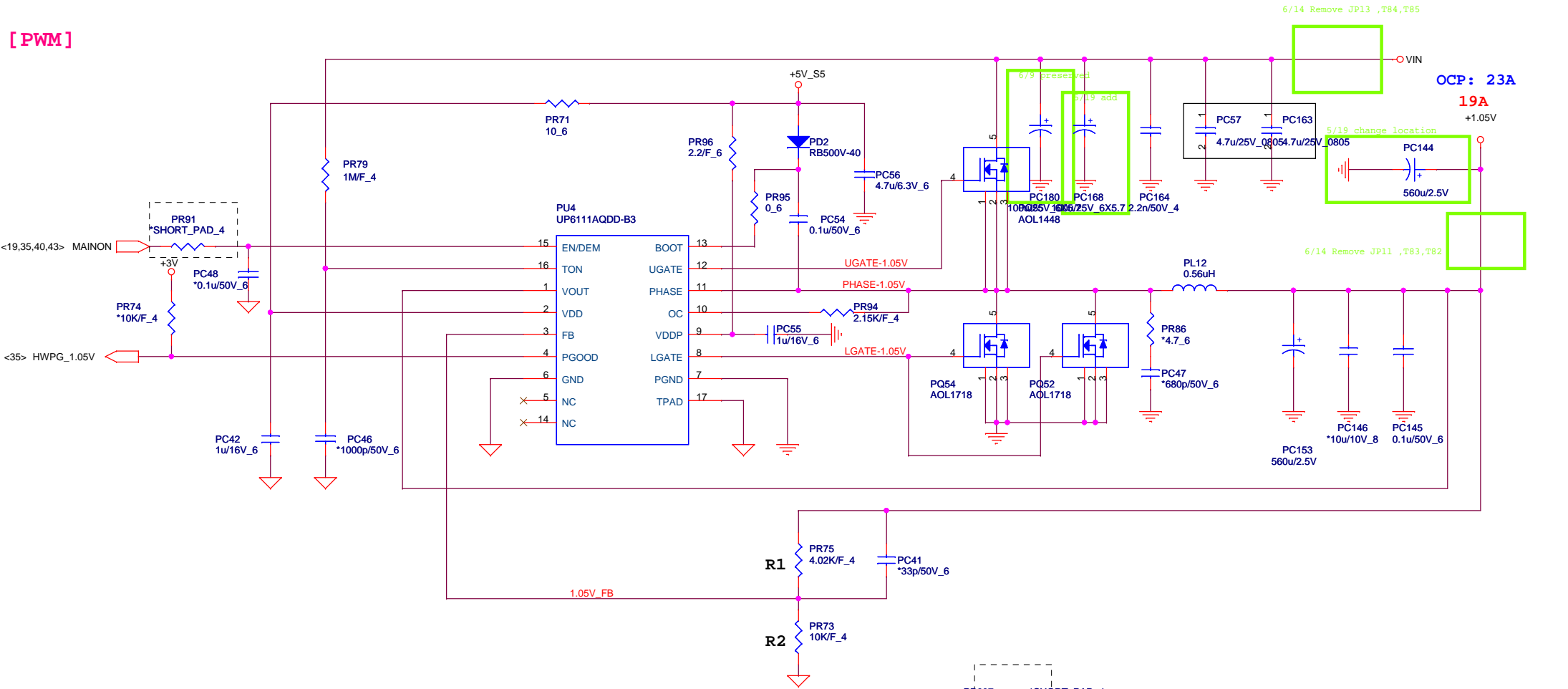
This NTC Close to Phase 1 Inductor

Panasonic
 ERT-J0EV474J

Quanta Computer Inc.
 PROJECT : ZQ9

Size	Document Number	Rev
	+VCC_CORE ADP3212	1A
Date:	Tuesday, June 22, 2010	Sheet 38 of 9

[PWM]



$$TON = 3.85p * RTON * Vout / (Vin - 0.5)$$


$$Frequency = Vout / (Vin * TON)$$

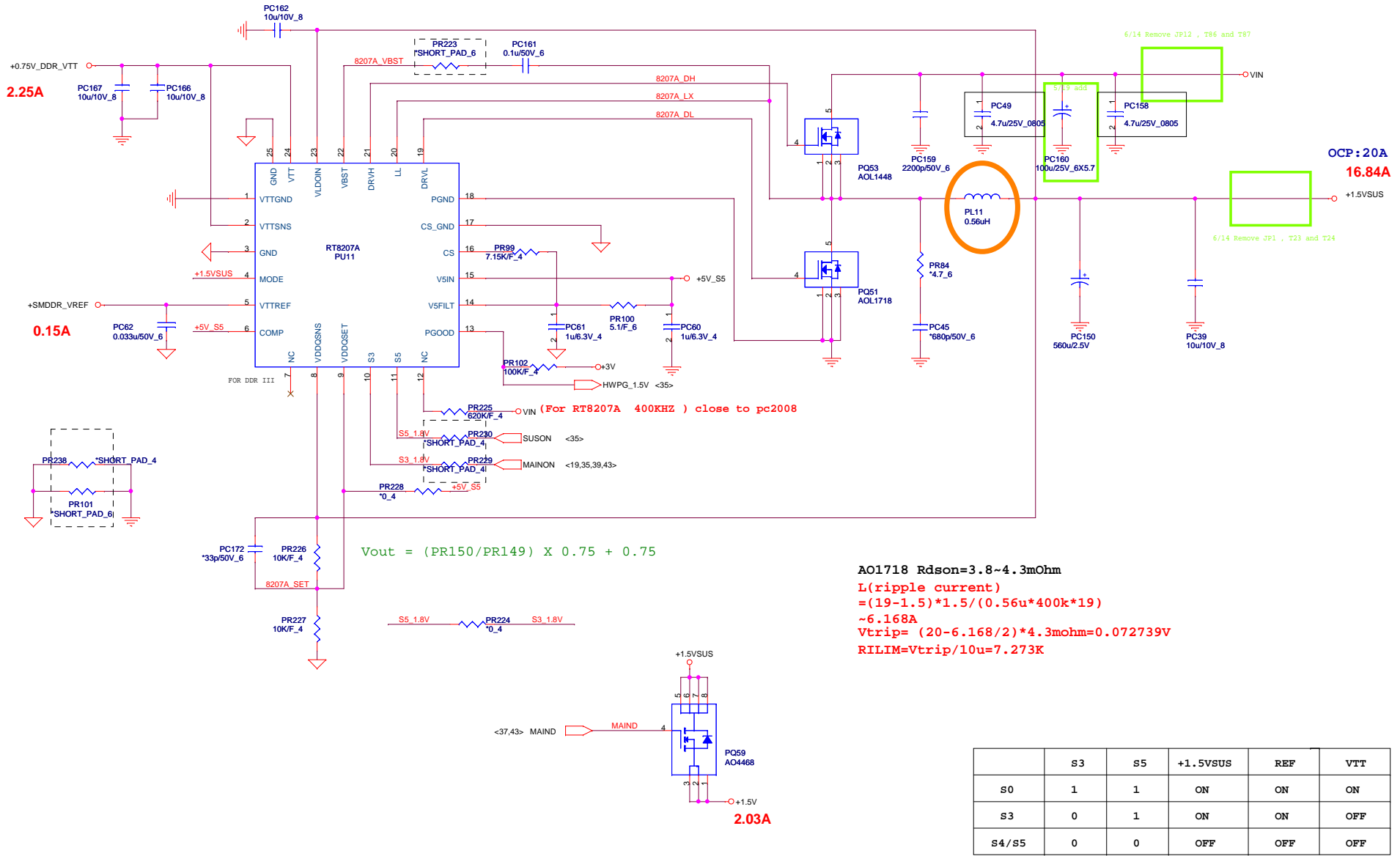
$$TON = 3.85p * 1M * 1 / (Vin - 0.5)$$

$$Frequency = 1 / (0.0036767) = 272K$$

AO1718 $R_{dson} = 3 \sim 4.3m\Omega$
 $I(ripple\ current) = (19 - 1.05) * 1.05 / (0.56u * 272k * 19) \sim 6.512A$

$RILIM = 2.15m\Omega * 23 - 3.256 / 20uA = 2.122K\Omega$
 $I(choke)\ peak = 29.512A$

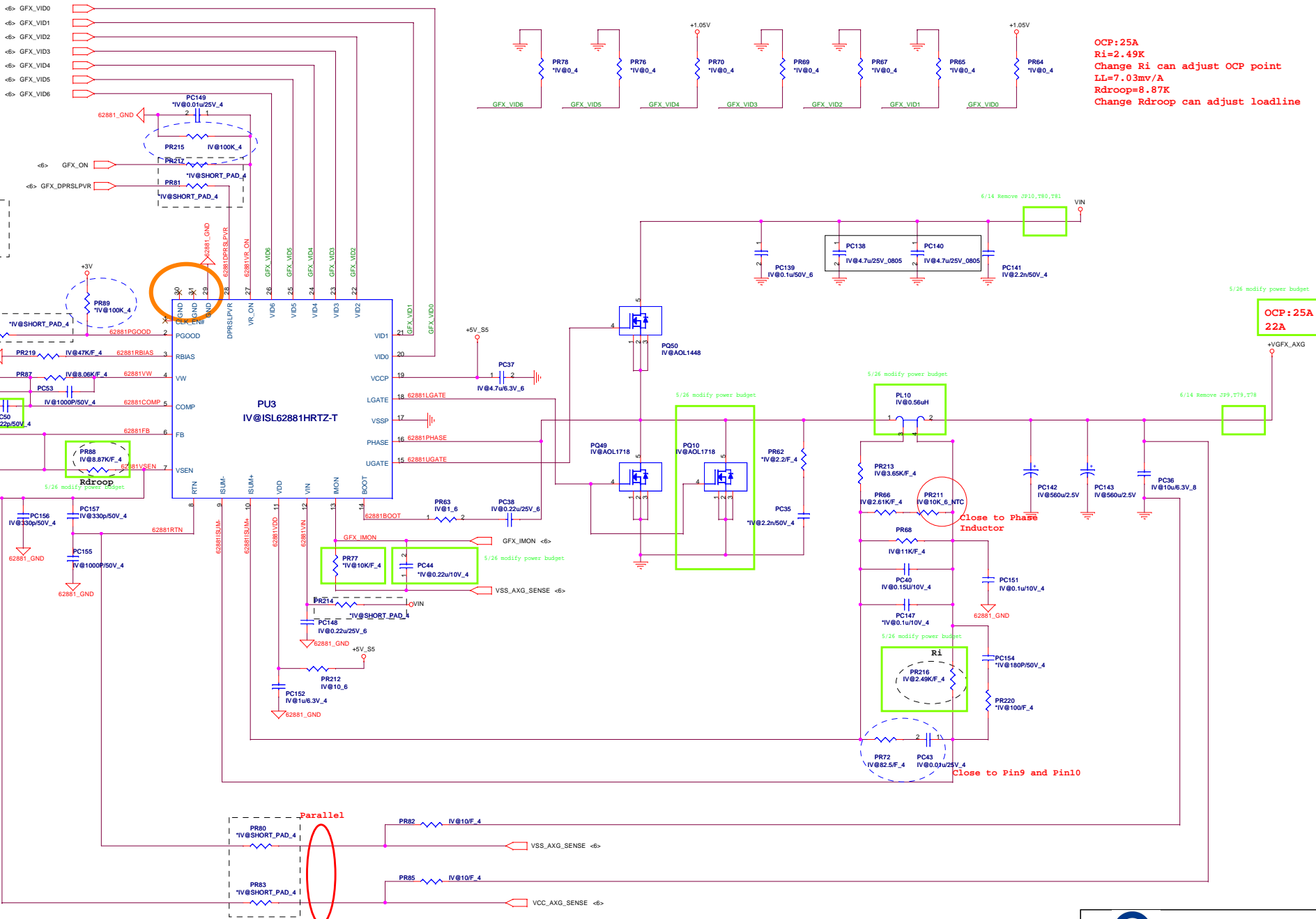
 Quanta Computer Inc. PROJECT : ZQ9		Size	Document Number	Rev
			+VTT (UP6111A)	1A
Date:	Tuesday, June 22, 2010	Sheet	39	of 9



$$V_{out} = (PR150/PR149) \times 0.75 + 0.75$$

AO1718 $R_{ds(on)}=3.8\sim 4.3m\Omega$
 $L(\text{ripple current}) = (19-1.5) \times 1.5 / (0.56\mu \times 400k \times 19)$
 $\sim 6.168A$
 $V_{trip} = (20 - 6.168 / 2) \times 4.3m\Omega = 0.072739V$
 $R_{ILIM} = V_{trip} / 10\mu = 7.273K$

	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

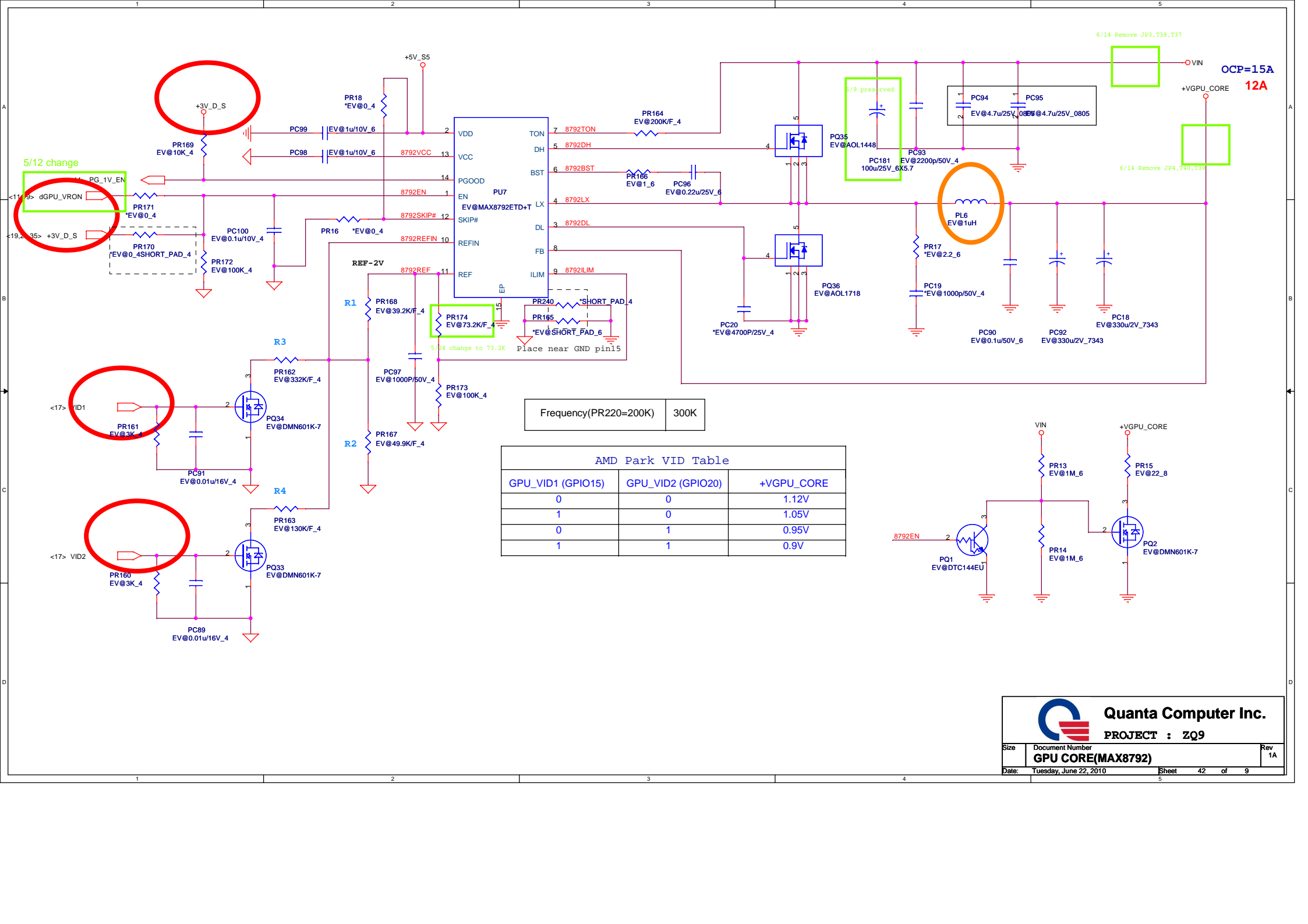


OCP:25A
 Ri=2.49K
 Change Ri can adjust OCP point
 LI=7.03mV/A
 Rdrops=8.87K
 Change Rdrops can adjust loadline

OCP: 25A
 22A

<p>Quanta Computer Inc. PROJECT : ZQ9</p>		
<p>Date: Tuesday, June 22, 2010</p>	<p>Sheet: 41 of 9</p>	<p>1A</p>

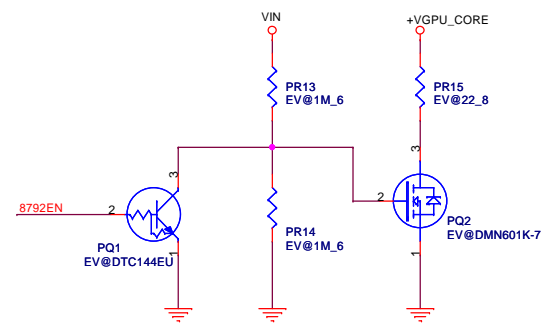
1. Level 1 Environment-related Substances should NEVER be used.
 2. Purchase Ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



OCP=1.5A
12A

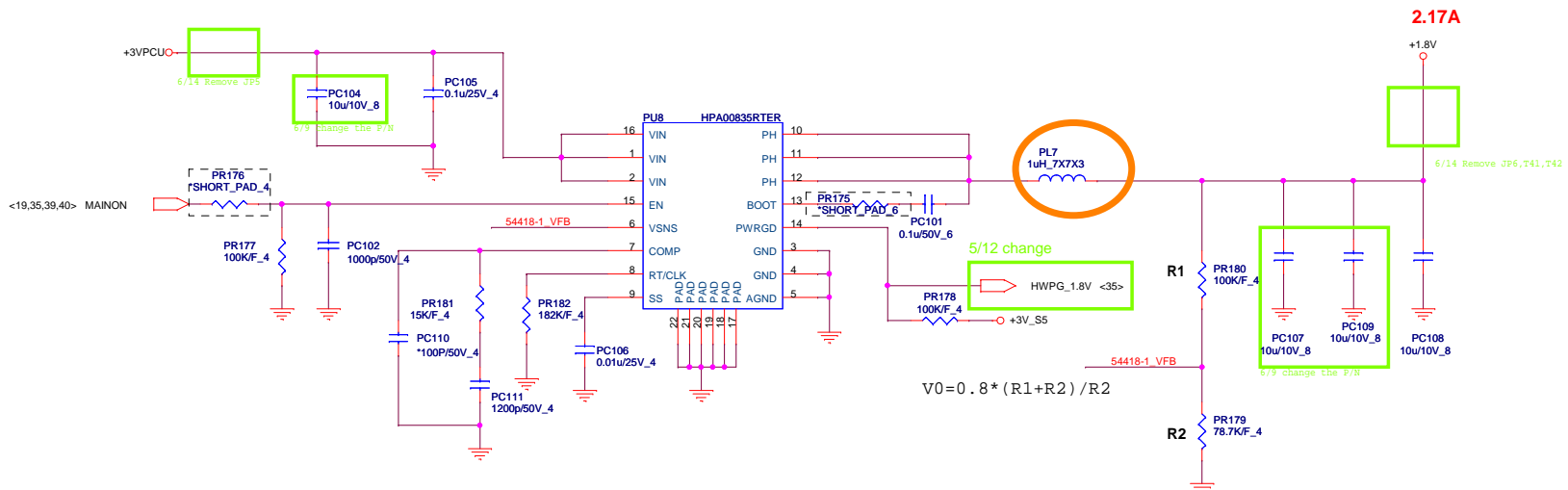
Frequency(PR220=200K) 300K

AMD Park VID Table		
GPU_VID1 (GPIO15)	GPU_VID2 (GPIO20)	+VGPU_CORE
0	0	1.12V
1	0	1.05V
0	1	0.95V
1	1	0.9V

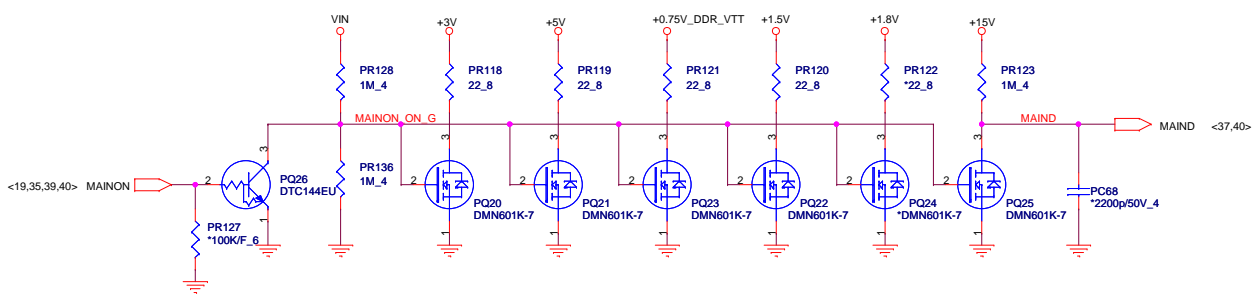
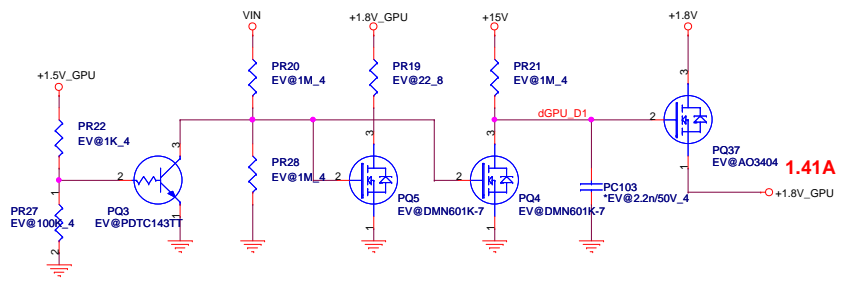
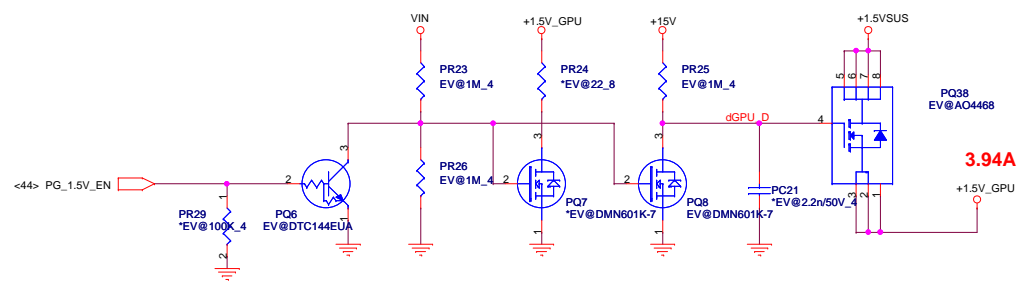


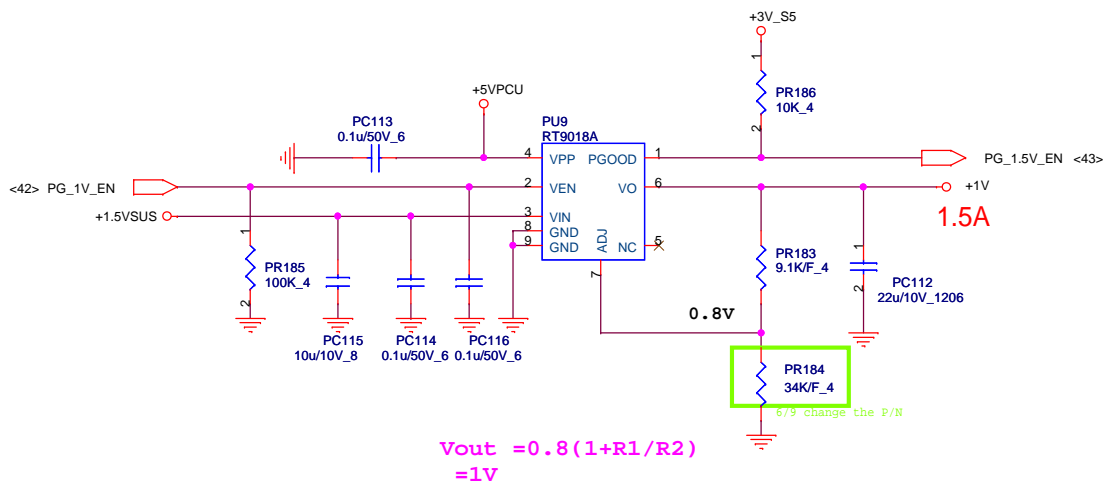
Quanta Computer Inc.
PROJECT : ZQ9

Size	Document Number GPU CORE(MAX8792)	Rev 1A
Date: Tuesday, June 22, 2010		Sheet 42 of 9

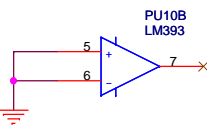


$$V0 = 0.8 * (R1 + R2) / R2$$





Thermal protection



For EC control thermal protection (output 3.3V)

Need fine tune for thermal protect point

