

Compal Confidential

NEW70 / 80 / 90 / 50 <LA-5892P> M/B Schematics Document
PEW51 <LA-5892P> M/B Schematics Document

Intel Arrandale Processor with DDRIII + Ibex Peak-M

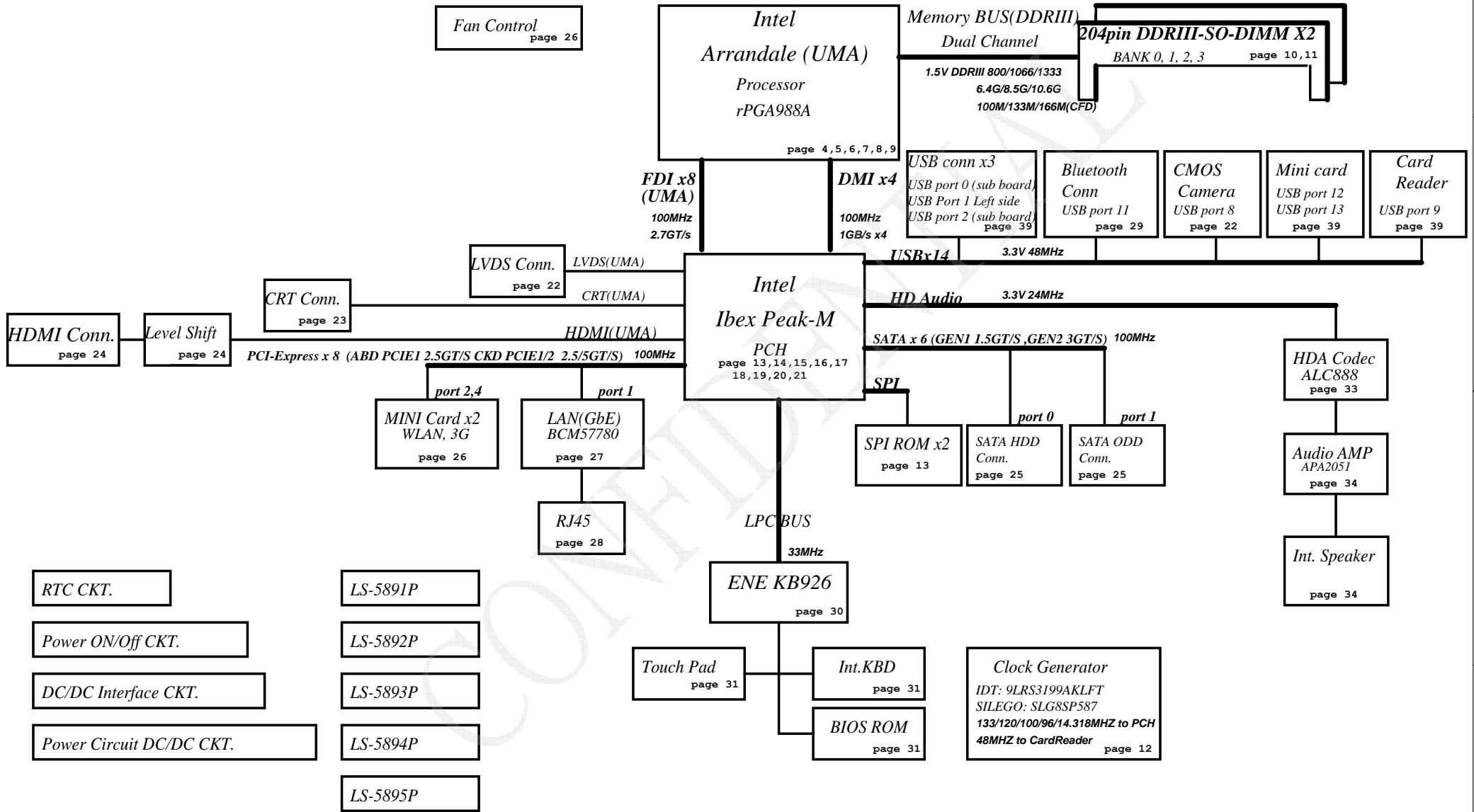
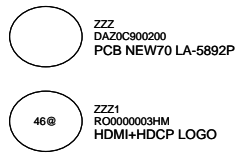
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Model Name NEW70 / 80 / 90 / 50

File Name : LA-5892P



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	ON	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for PCH	ON	OFF	OFF
+1.05VS_VTT	1.05V switched power rail (1.05 for AUB CPU)	ON	OFF	OFF
+1.5V	1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+5V	5V power rail for PCH	ON	ON	ON
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b		

EC SM Bus2 address

Ibex SM Bus address

Device	Address
Clock Generator (9LRS3199AKLFT, SLG8SP587)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3(Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5(Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Project ID / Board ID Table for EC-AD channel

Vcc	3.3V +/- 5%					
Ra/Rc	100K +/- 5%					
	Rb / Rd	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	Board ID	Project ID
0	0	0 V	0 V	0 V	0.1	NEWX0
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	0.2	PEW51
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	0.3	
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	1.0	
4	56K +/- 5%	1.036 V	1.185 V	1.264 V		
5	100K +/- 5%	1.453 V	1.650 V	1.759 V		
6	200K +/- 5%	1.935 V	2.200 V	2.341 V		
7	NC	2.500 V	3.300 V	3.300 V		

BTO Option Table

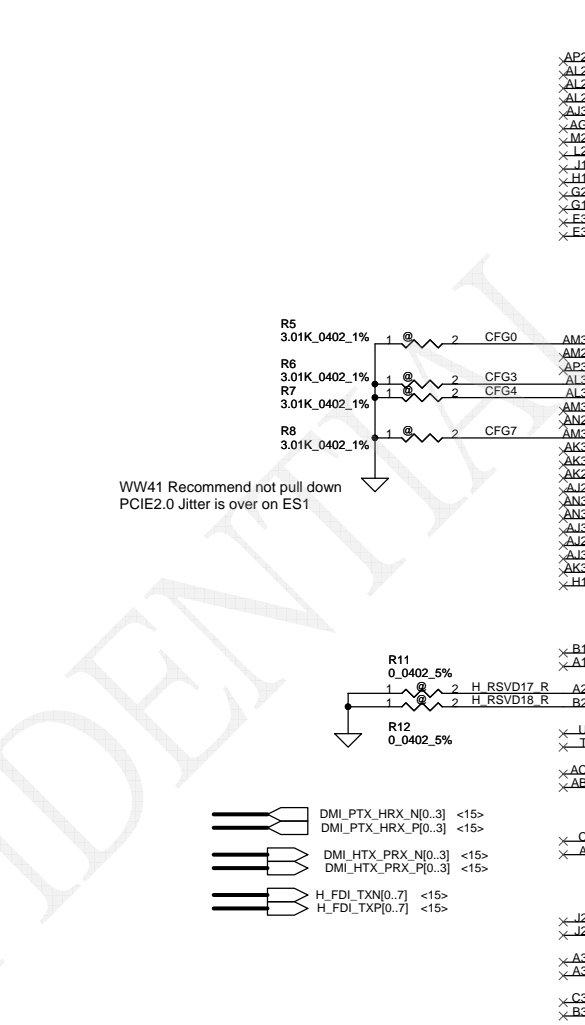
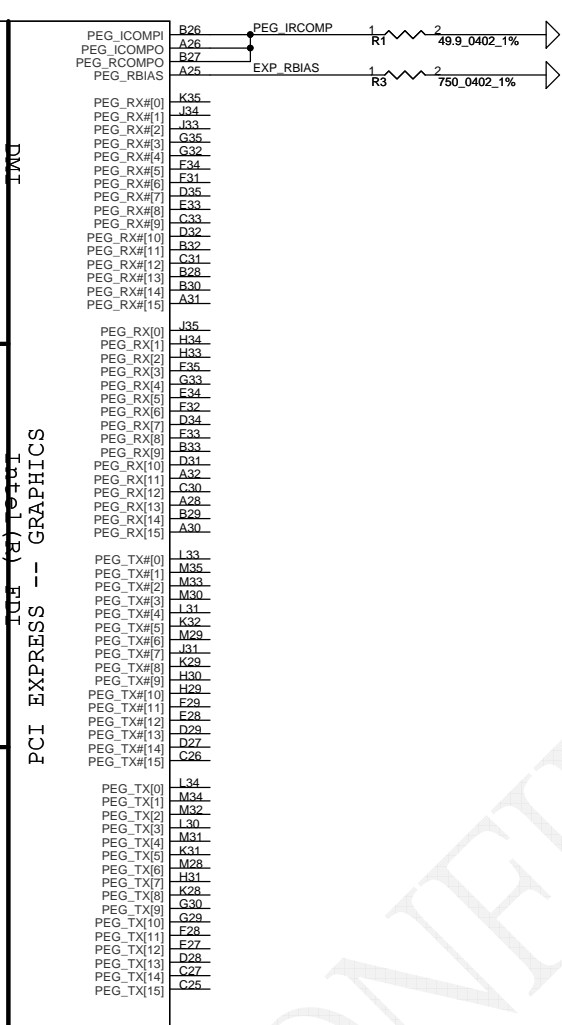
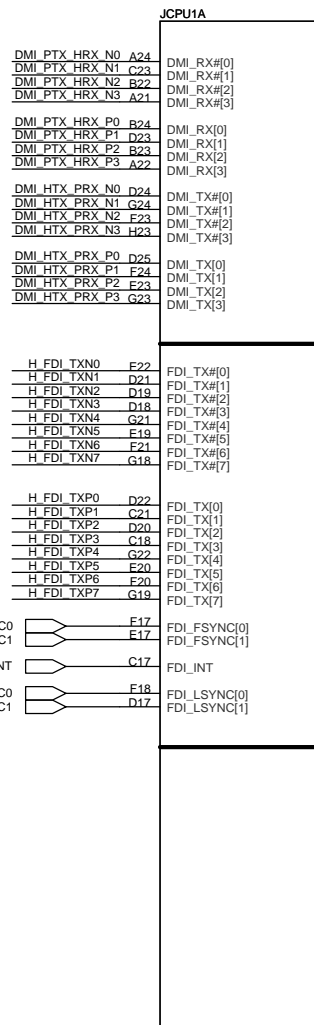
BTO Item	BOM Structure
HDMI	HDMI@
3G	3G@
9050@	NEW90 / NEW50
7080@	NEW70 / NEW80
For NEWX0 ID	NEWX0@
For PEW51 ID	PEW51@

BOM Config

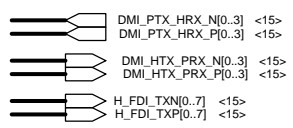
USB Port Table

USB 2.0	USB 1.1	Port	4 External USB Port	3 External USB Port	
EHCI1	UHCI0	0	Ext1 USB	Ext1 USB	
		1	Ext3 HS USB	Ext3 HS USB	
		2	Ext2 USB	Ext2 USB	
	UHCI1	3			
		UHCI2	4		
		5			
		6			
EHCI2	UHCI3	7			
		UHCI4	8	Camera	Camera
		9	Card Reader	Card Reader	
	UHCI5	10	SIM CARD	SIM CARD	
		11	Blue Tooth	Blue Tooth	
		12	1st Min-Card	1st Min-Card	
		13	2st Min-Card	2st Min-Card	

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WW41 Recommend not pull down
PCI-E2.0 Jitter is over on ES1



eDP Signals Mapping

eDP Signal	PEG Singals	Lane Reversal
eDP_TX0	PEG HTX C GRX P15	PEG HTX C GRX P0
eDP_TX#0	PEG HTX C GRX N15	PEG HTX C GRX N0
eDP_TX1	PEG HTX C GRX P14	PEG HTX C GRX P1
eDP_TX#1	PEG HTX C GRX N14	PEG HTX C GRX N1
eDP_TX2	PEG HTX C GRX P13	PEG HTX C GRX P2
eDP_TX#2	PEG HTX C GRX N13	PEG HTX C GRX N2
eDP_TX3	PEG HTX C GRX P12	PEG HTX C GRX P3
eDP_TX#3	PEG HTX C GRX N12	PEG HTX C GRX N3
eDP_AUX	PEG GTX C HRX P13	PEG GTX C HRX P2
eDP_AUX#	PEG GTX C HRX N13	PEG GTX C HRX N2
eDP_HPD#	PEG GTX C HRX P12	PEG GTX C HRX P3

CFG0 - PCI-Express Configuration Select

*1:Single PEG
0:Buffering enabled

CFG3 - PCI-Express Static Lane Reversal

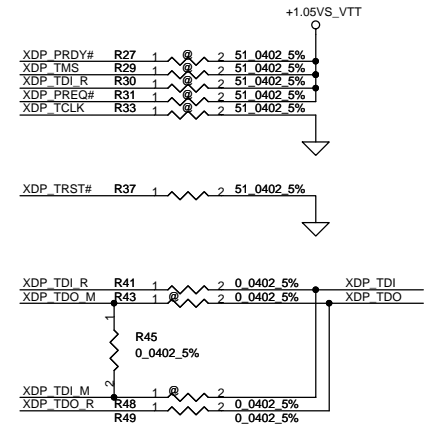
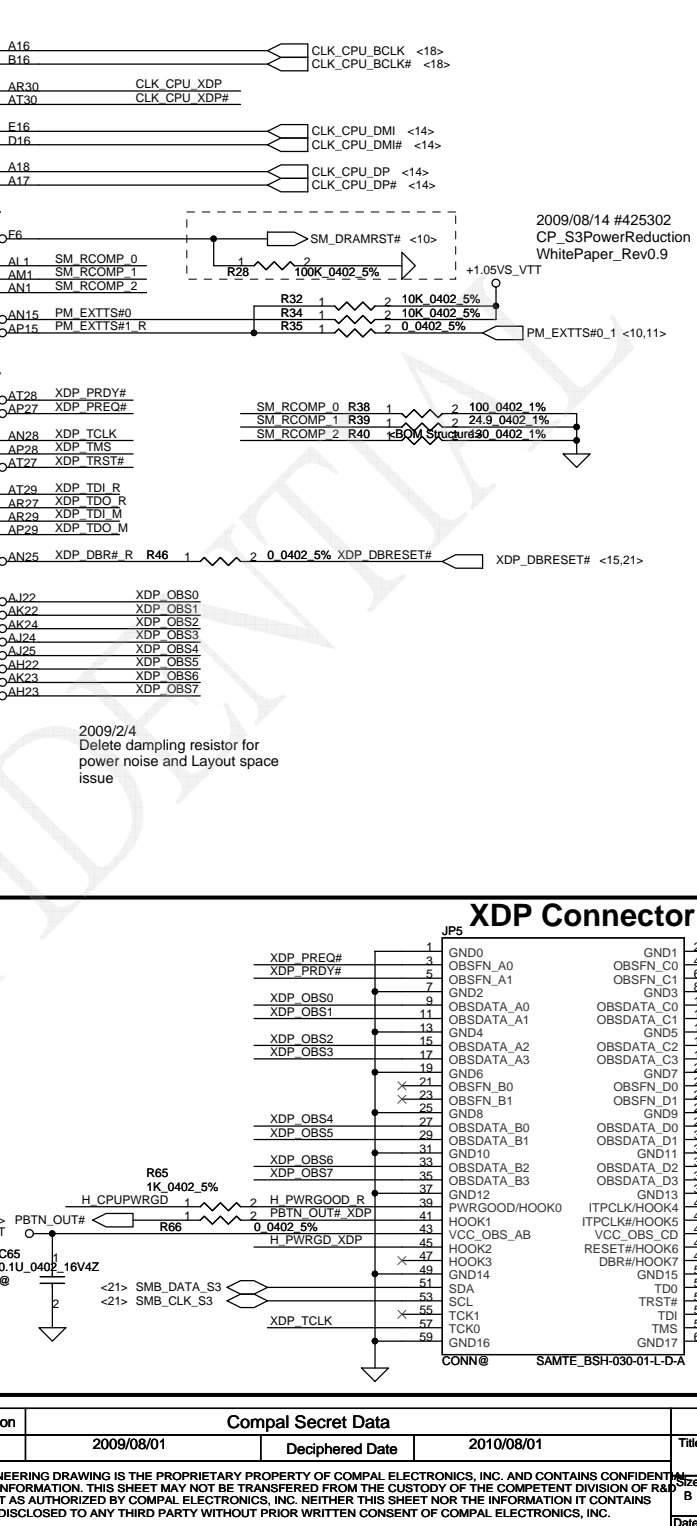
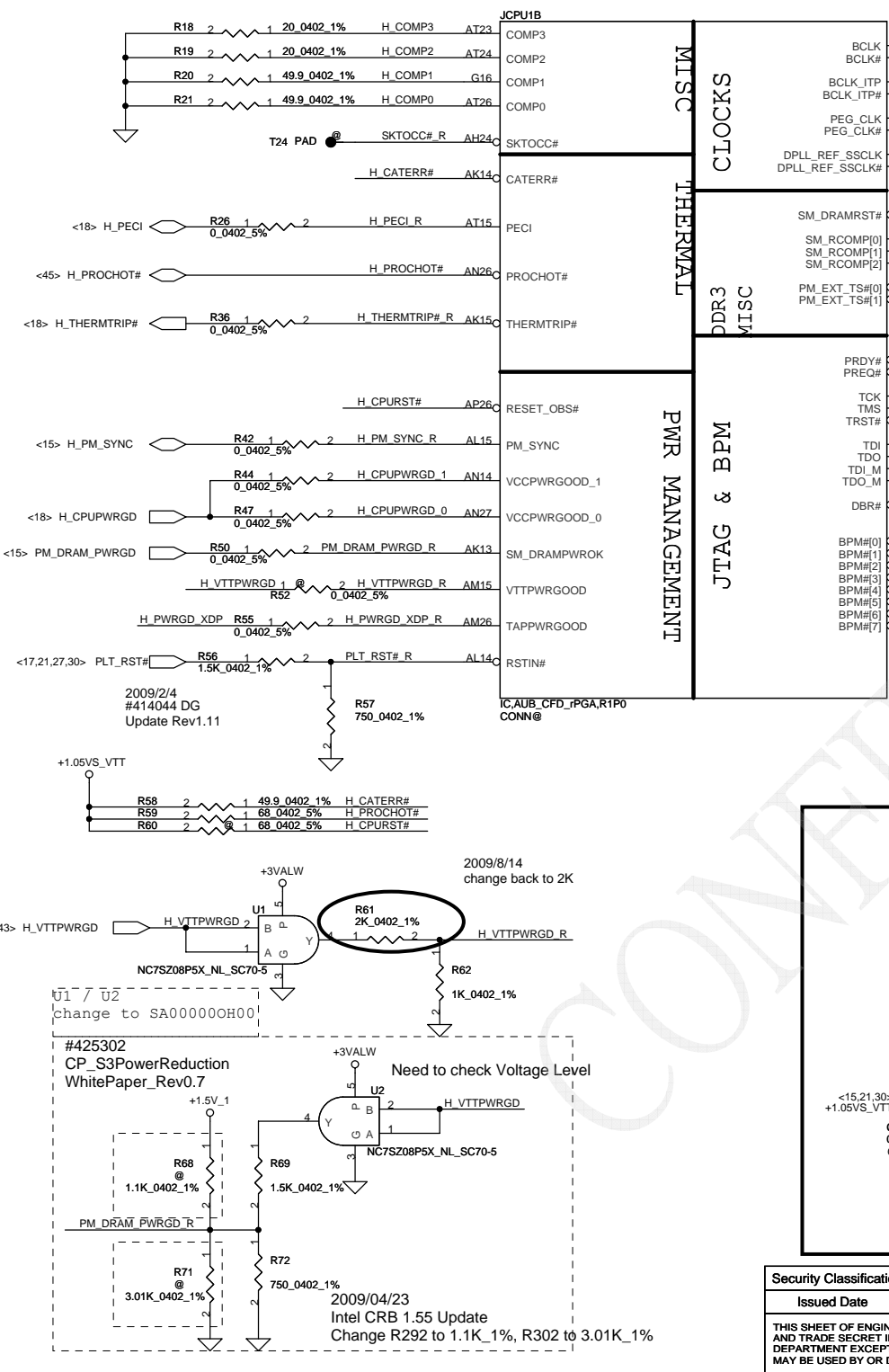
*1 :Normal Operation
0 :Lane Numbers Reversed
15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence

*1:Disabled; No Physical Display Port attached to Embedded Display Port
0:Enabled; An external Display Port device is connected to the Embedded Display Port

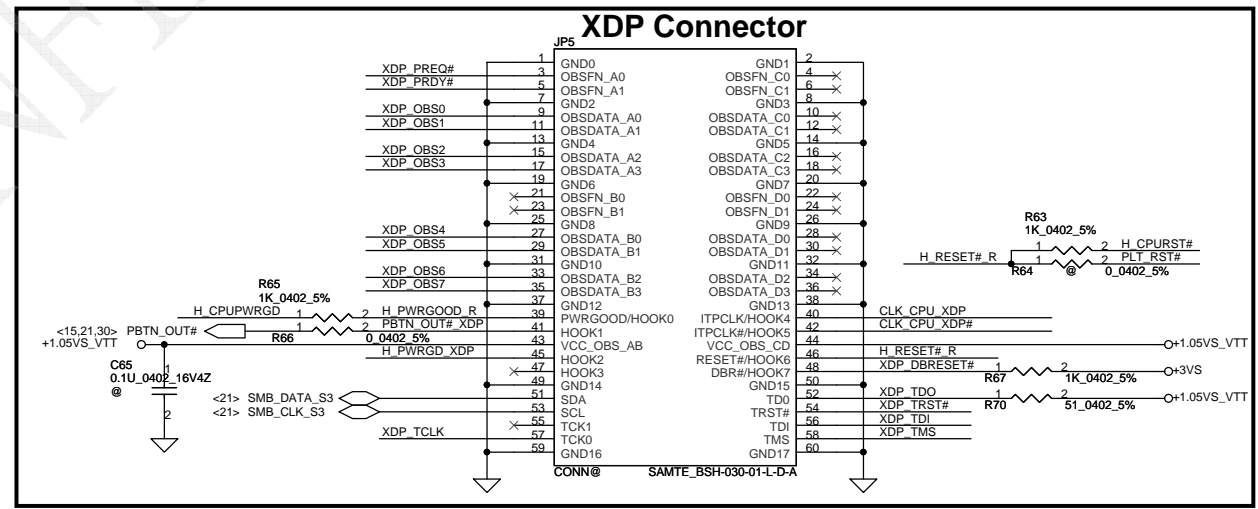
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JTAG MAPPING

Scan Chain (Default)	STUFF -> R653, R657, R662 NO STUFF -> R655, R660
CPU Only	STUFF -> R653, R655 NO STUFF -> R657, R660, R662
GMCH Only	STUFF -> R660, R662 NO STUFF -> R653, R655, R657



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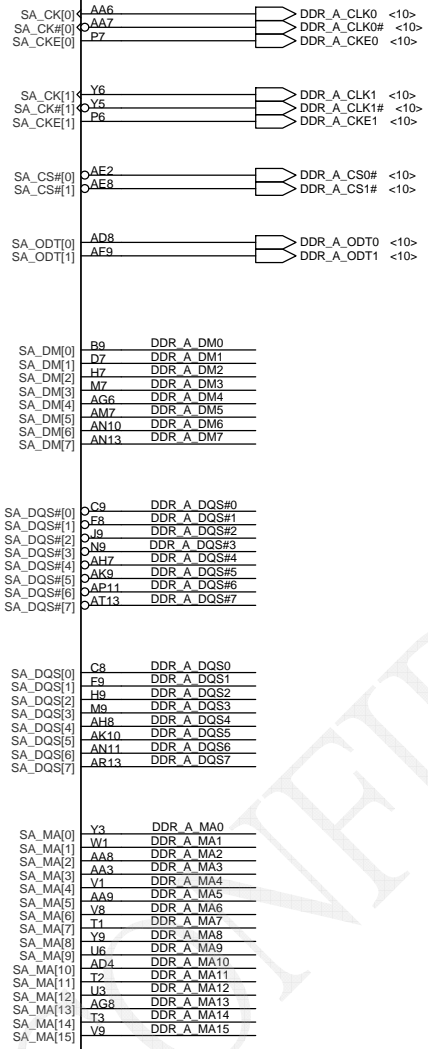
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 <10> DDR_A_DM[0..7]
 <10> DDR_A_DQS[0..7]
 <10> DDR_A_MA[0..15]

JCPU1C

- DDR A D0 A10
- DDR A D1 C10
- DDR A D2 C7
- DDR A D3 A7
- DDR A D4 B10
- DDR A D5 D10
- DDR A D6 E10
- DDR A D7 A8
- DDR A D8 D8
- DDR A D9 F10
- DDR A D10 E6
- DDR A D11 E7
- DDR A D12 E9
- DDR A D13 B7
- DDR A D14 E7
- DDR A D15 C6
- DDR A D16 H10
- DDR A D17 G8
- DDR A D18 K7
- DDR A D19 J8
- DDR A D20 G7
- DDR A D21 G10
- DDR A D22 J7
- DDR A D23 J10
- DDR A D24 L7
- DDR A D25 M6
- DDR A D26 M8
- DDR A D27 I9
- DDR A D28 L6
- DDR A D29 K8
- DDR A D30 K8
- DDR A D31 P9
- DDR A D32 AH5
- DDR A D33 AF5
- DDR A D34 AK6
- DDR A D35 AK7
- DDR A D36 AF6
- DDR A D37 AG5
- DDR A D38 A17
- DDR A D39 A16
- DDR A D40 A110
- DDR A D41 A19
- DDR A D42 AL10
- DDR A D43 AK12
- DDR A D44 AK8
- DDR A D45 A17
- DDR A D46 AK11
- DDR A D47 A18
- DDR A D48 AN8
- DDR A D49 AM10
- DDR A D50 AR11
- DDR A D51 AL11
- DDR A D52 AM9
- DDR A D53 AN9
- DDR A D54 AT11
- DDR A D55 AP12
- DDR A D56 AM12
- DDR A D57 AN12
- DDR A D58 AM13
- DDR A D59 AT14
- DDR A D60 AT12
- DDR A D61 AL13
- DDR A D62 AR14
- DDR A D63 AP14

<10> DDR_A_BS0
 <10> DDR_A_BS1
 <10> DDR_A_BS2

<10> DDR_A_CAS#
 <10> DDR_A_RAS#
 <10> DDR_A_WE#



IC_AUB_CFD_rPGA,R1P0
 CONN@

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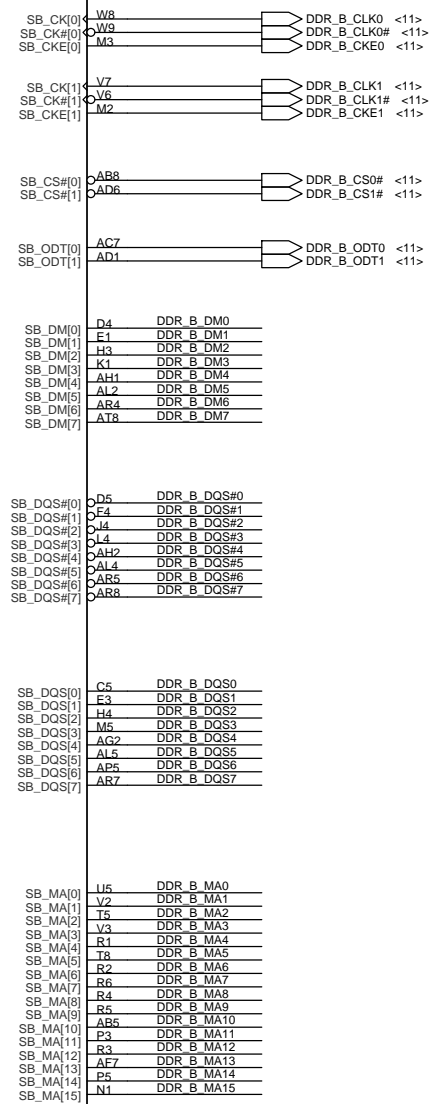
JCPU1D

- DDR B D0 B5
- DDR B D1 A5
- DDR B D2 C3
- DDR B D3 B3
- DDR B D4 E4
- DDR B D5 A6
- DDR B D6 C4
- DDR B D7 D1
- DDR B D8 D1
- DDR B D9 D2
- DDR B D10 F2
- DDR B D11 E1
- DDR B D12 C2
- DDR B D13 F3
- DDR B D14 F3
- DDR B D15 G4
- DDR B D16 H6
- DDR B D17 G2
- DDR B D18 J6
- DDR B D19 J3
- DDR B D20 G1
- DDR B D21 G5
- DDR B D22 J2
- DDR B D23 J1
- DDR B D24 J5
- DDR B D25 L2
- DDR B D26 K1
- DDR B D27 M2
- DDR B D28 K4
- DDR B D29 K4
- DDR B D30 M4
- DDR B D31 N5
- DDR B D32 AG1
- DDR B D33 AG1
- DDR B D34 AG1
- DDR B D35 AK1
- DDR B D36 AG4
- DDR B D37 AG3
- DDR B D38 AJ4
- DDR B D39 AH4
- DDR B D40 AK3
- DDR B D41 AK4
- DDR B D42 AM6
- DDR B D43 AN2
- DDR B D44 AK5
- DDR B D45 AK2
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- DDR B D49 AN5
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- DDR B D51 AN6
- DDR B D52 AN4
- DDR B D53 AN3
- DDR B D54 AT5
- DDR B D55 AT6
- DDR B D56 AN7
- DDR B D57 AP6
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- DDR B D59 AT9
- DDR B D60 AT7
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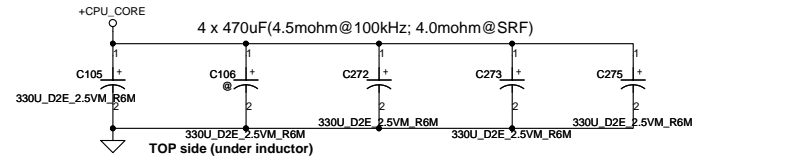
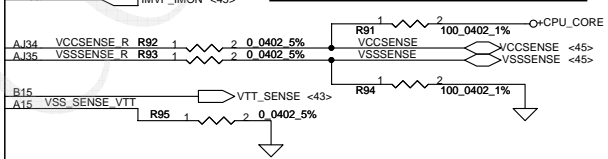
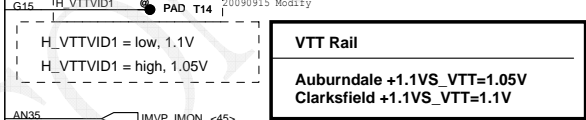
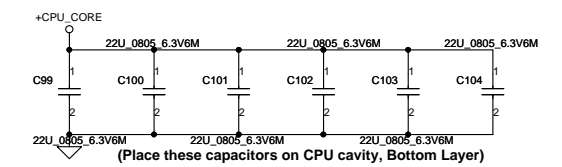
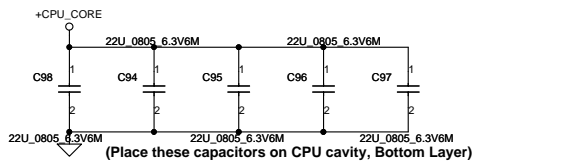
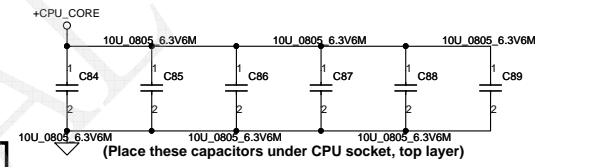
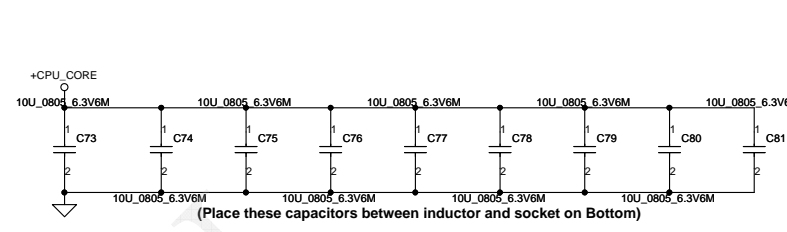
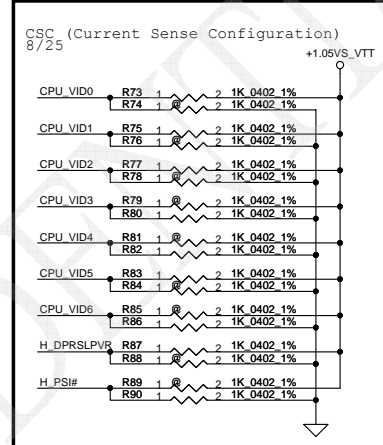
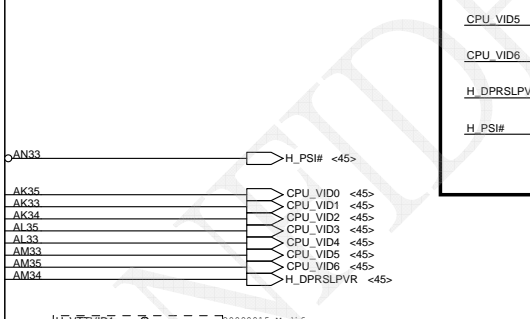
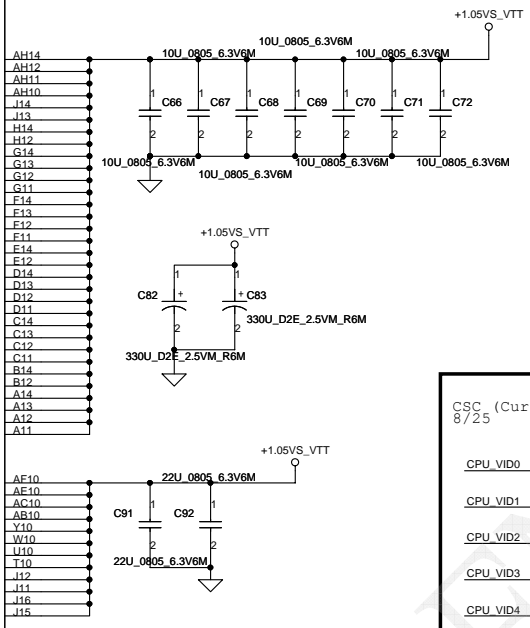
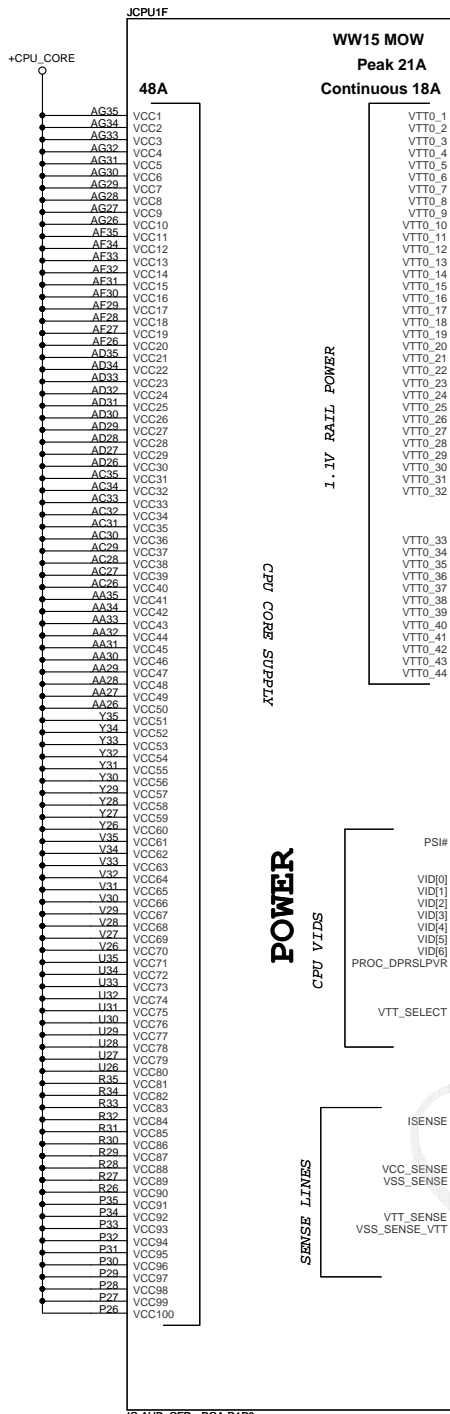
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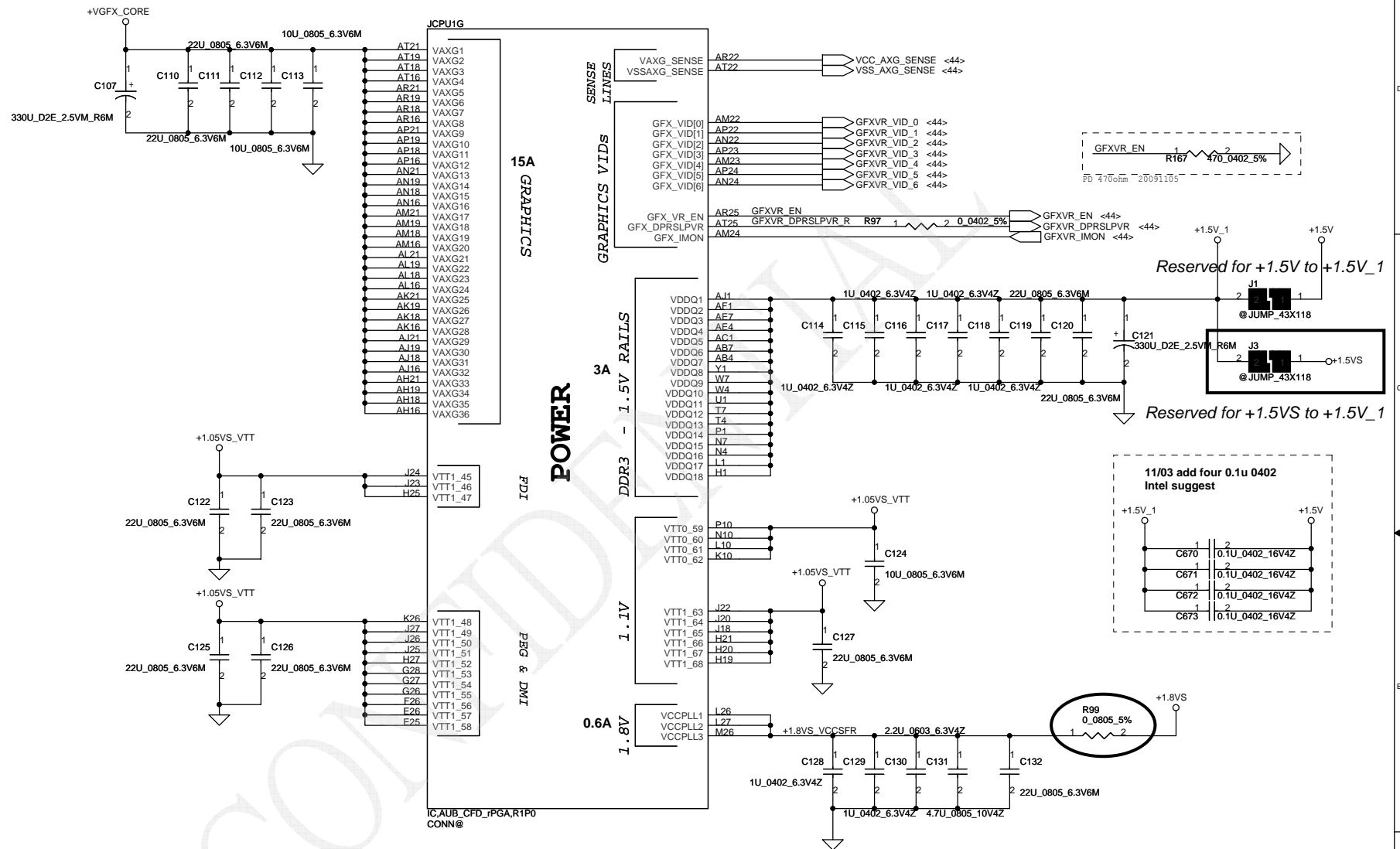
DDR SYSTEM MEMORY - B

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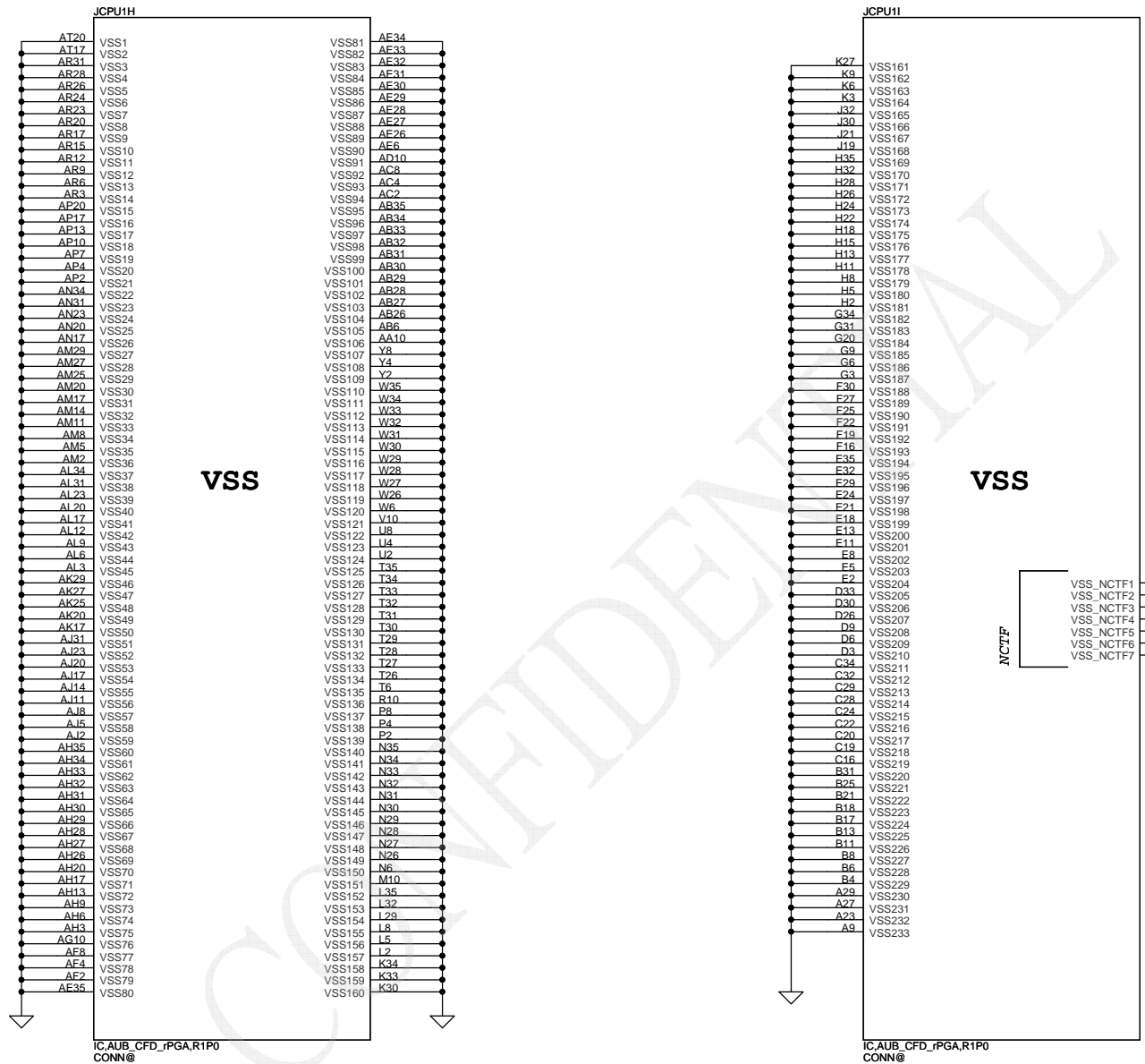


	C,uF	ESR, mohm	Stuffing Option
+CPU-CORE Decoupling	4X470uF	4m ohm/4	2X470uF
SPCAP, Polymer	16X22uF	3m ohm/12	
MLCC 0805 X5R	16X10uF	3m ohm/16	

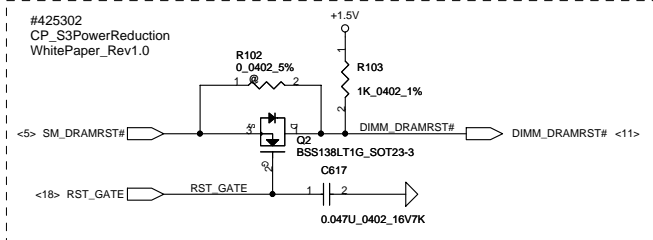
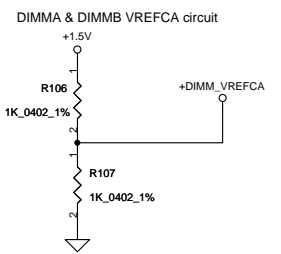
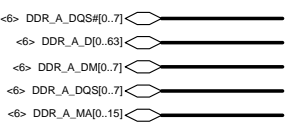
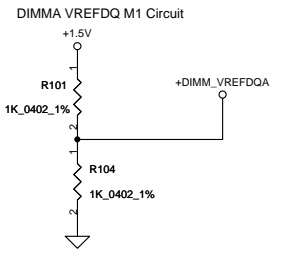
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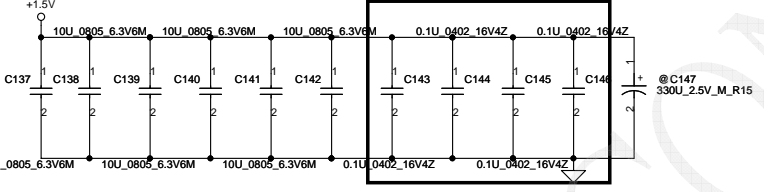


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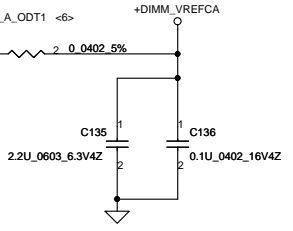
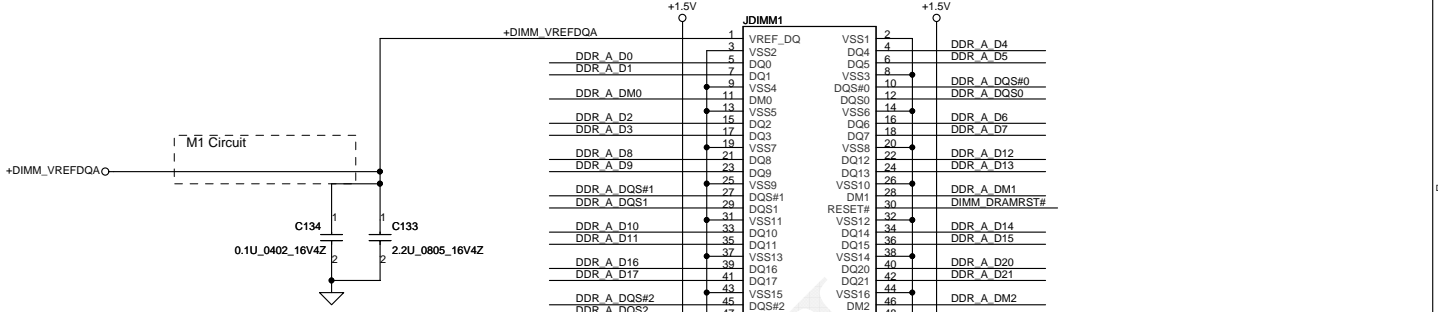
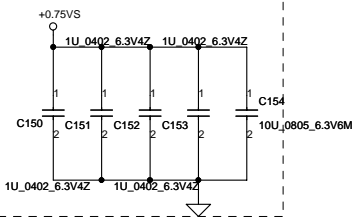


Layout Note:
Place near JDIMM1

Layout Note: Place these 4 Caps near Command and Control signals of DIMM A



Layout Note:
Place near JDIMM1.203 & JDIMM1.204

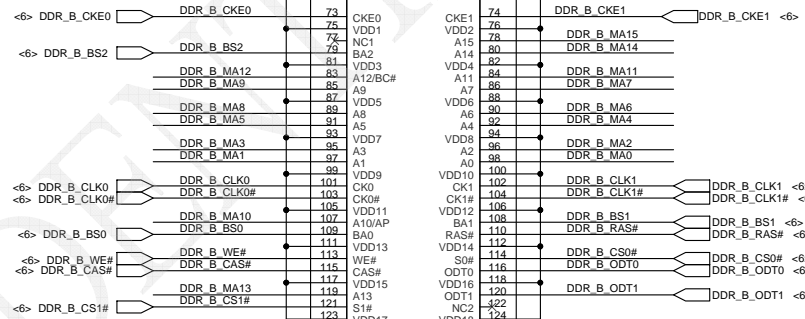
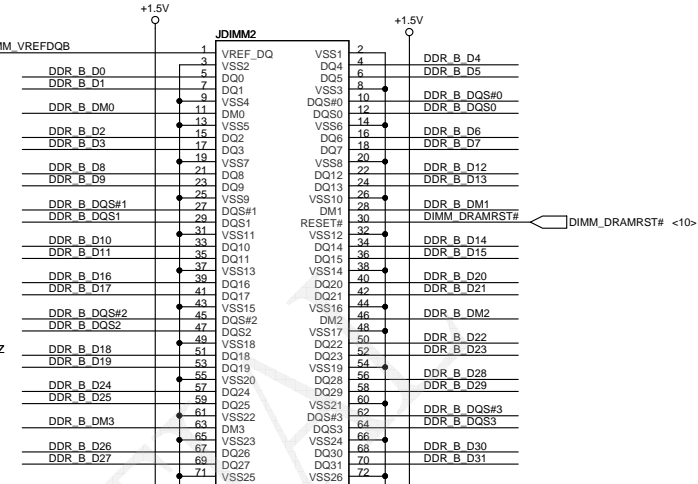
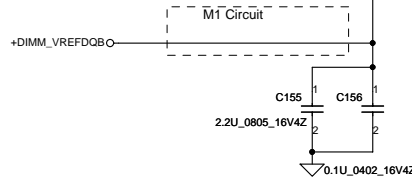
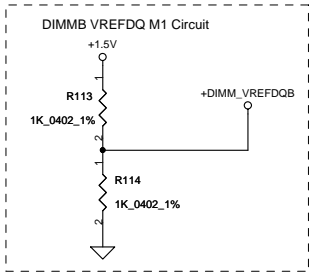


**DDR3 SO-DIMM A
Change to Reverse Type
8mm High**

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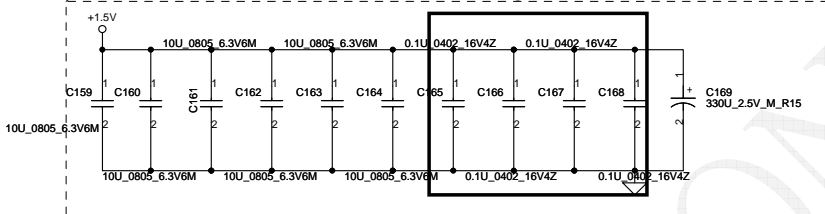
- <6> DDR_B_DQS#[0..7]
- <6> DDR_B_D[0..63]
- <6> DDR_B_DM[0..7]
- <6> DDR_B_DQS[0..7]
- <6> DDR_B_MA[0..15]

2008/9/8 #400755
 Calpella Clarksville
 DDR3 SO-DIMM
 VREFDQ Platform
 Design Guide Change Details

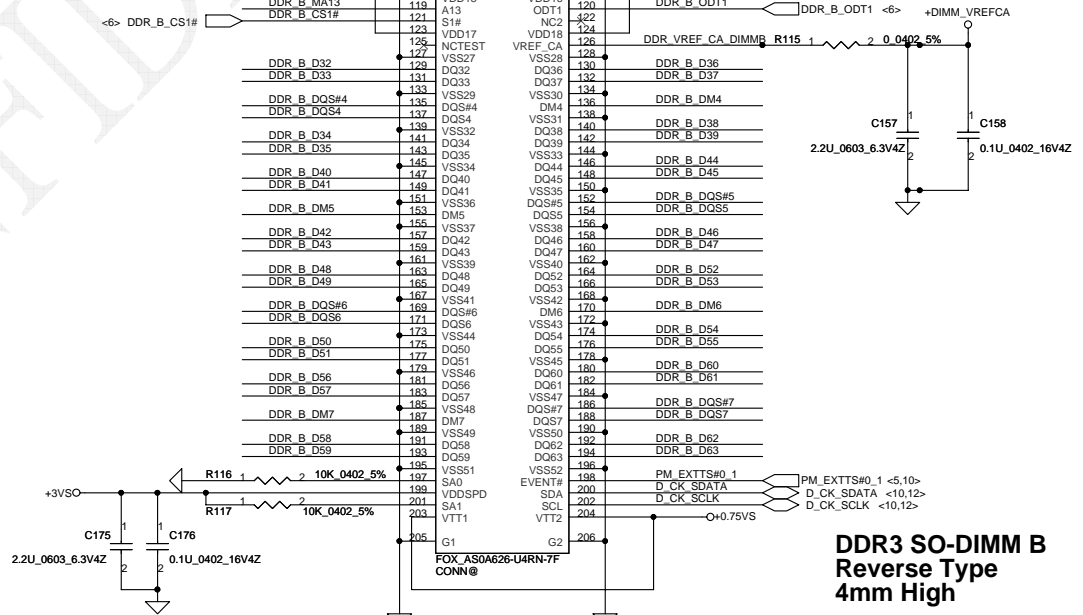
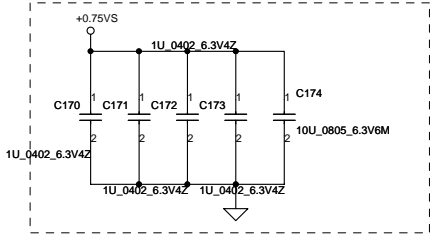


Layout Note:
Place near JDIMM2

Layout Note: Place these 4 Caps near Command and Control signals of DIMMB

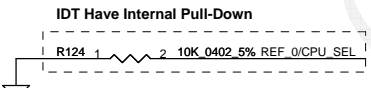
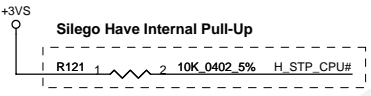
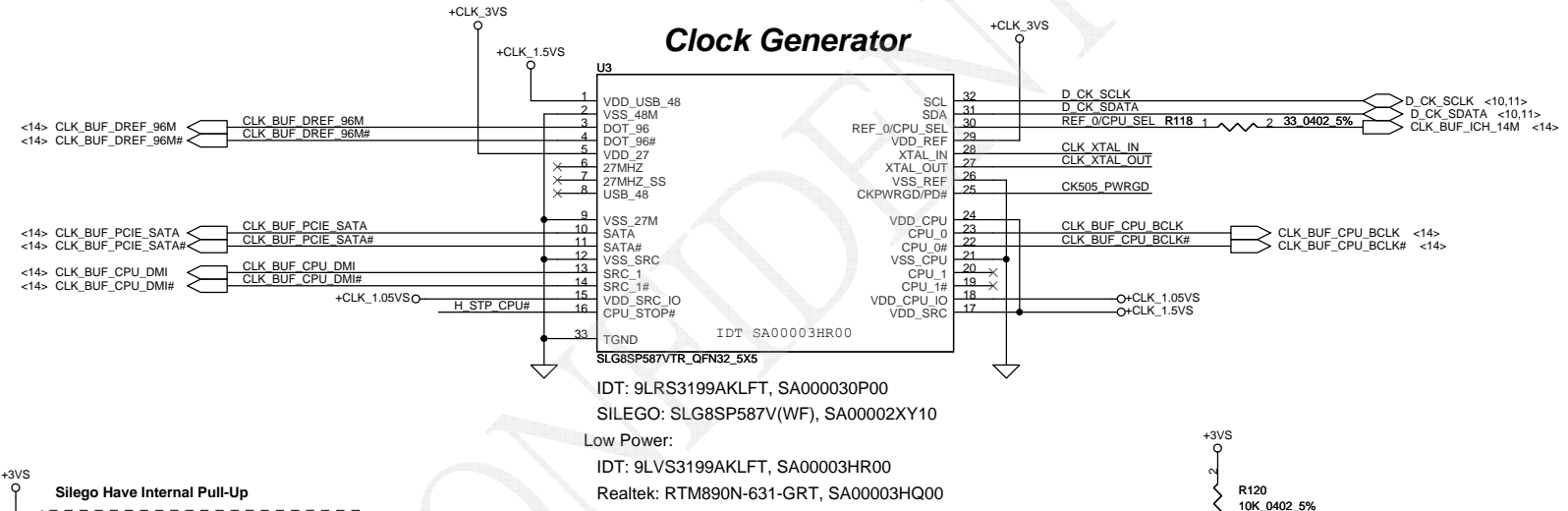
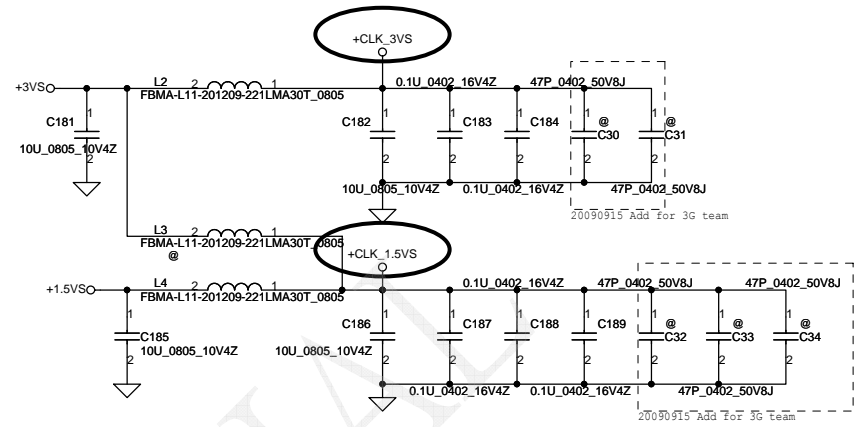
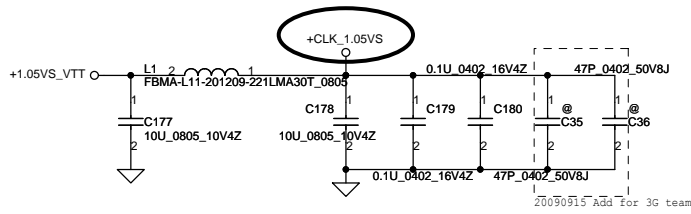


Layout Note:
Place near JDIMM2.203 & JDIMM2.204

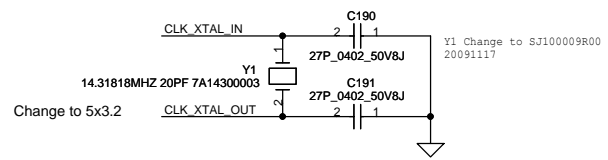
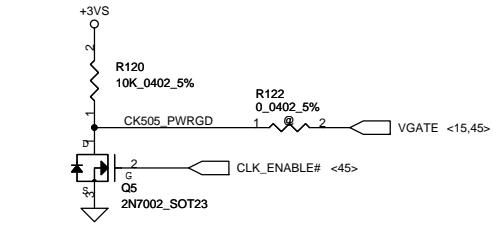
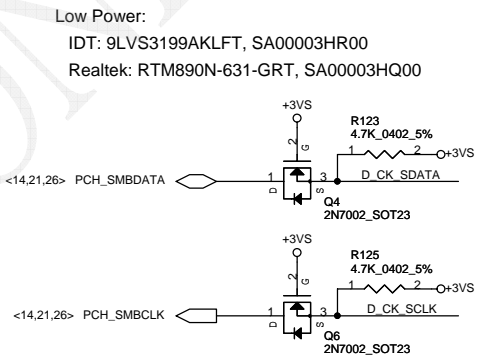


**DDR3 SO-DIMM B
Reverse Type
4mm High**

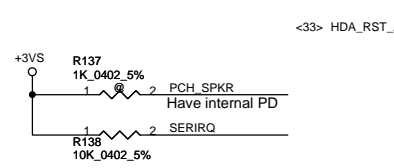
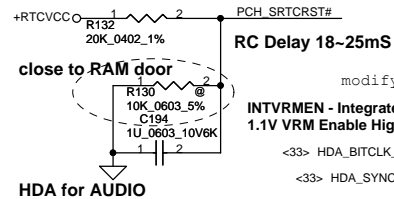
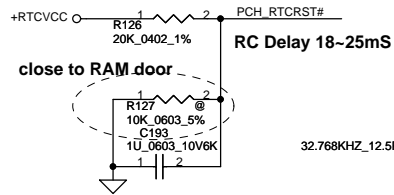
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PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

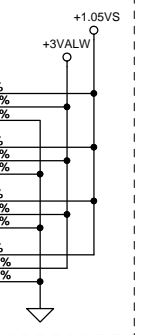
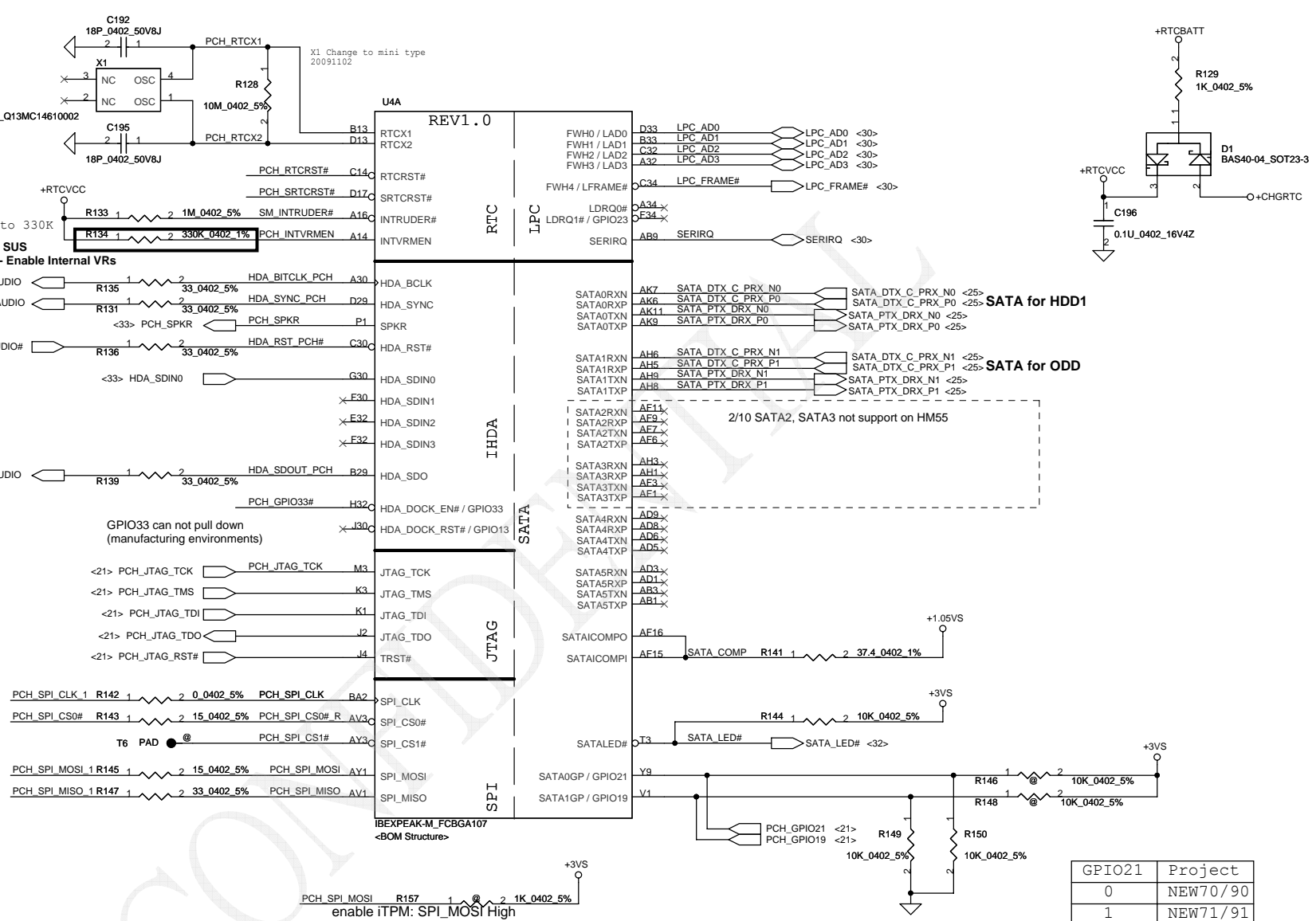


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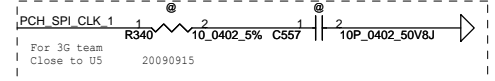
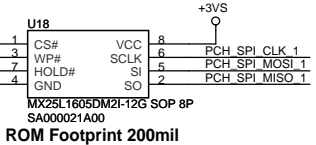
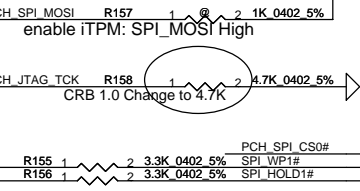


If GPIO33 pull down, ME will not working. For factory update ME, pull down resistor pull under door.

GPIO33 has a weak internal pull-up
NOTE: Asserting the GPIO33 low on the rising edge of PWROK will also halt Intel Management Engine after chipset bringup and disable runtime Intel Management Engine features. This is a debug mode and must not be asserted after manufacturing/ debug.



20090923 Update
2008 Intel MOW36/MOW50
TDO:
Reserved on ES1 Sample
Mount R516, R517 on ES2 Sample
MP mount R689, R690, R691, R692 and remove others

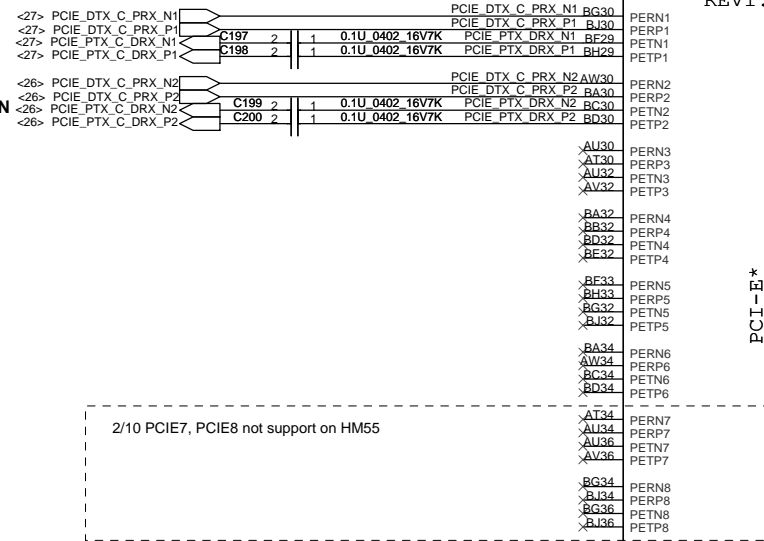


GPIO21	Project
0	NEW70/90
1	NEW71/91

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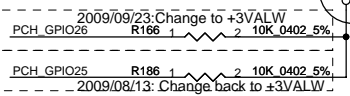
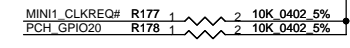
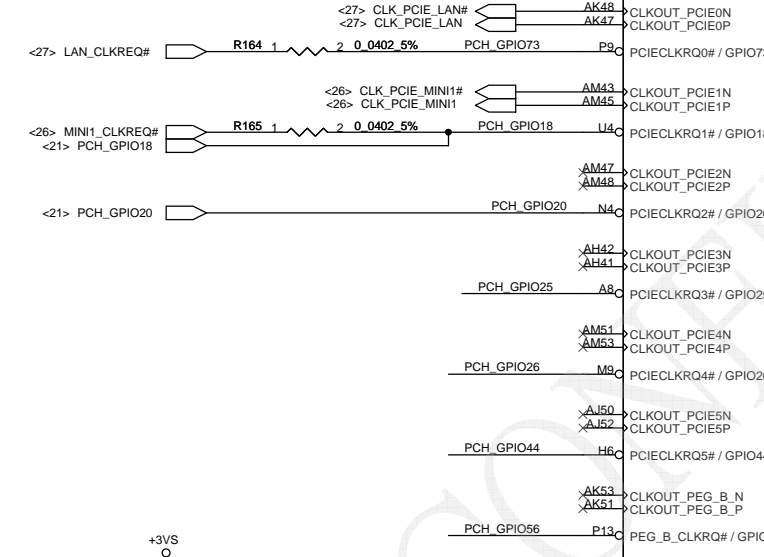
For PCIE LAN

For Wireless LAN



For PCIE LAN

For Wireless LAN

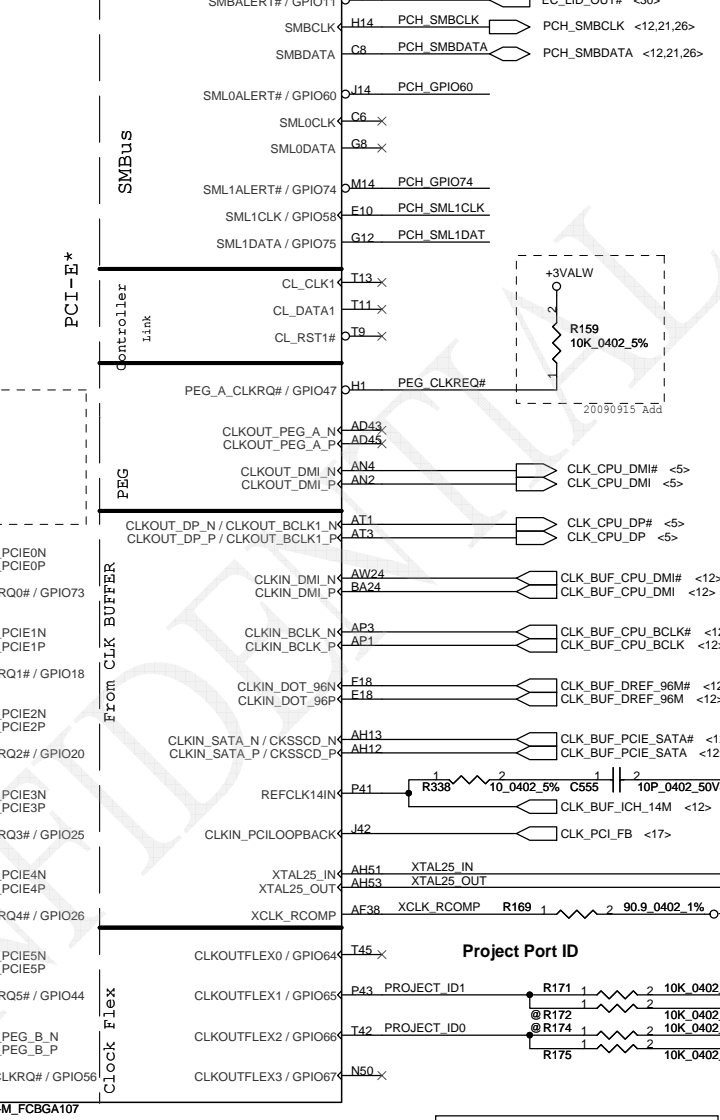


2009/09/23: Change to +3VALW
2009/08/13: Change back to ±3VALW



U4B

REV1.0



Board ID

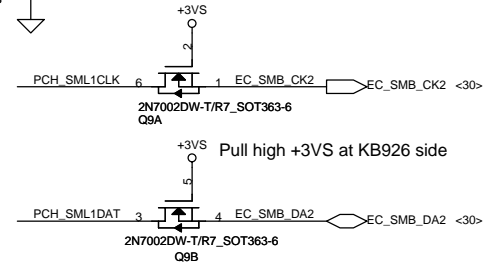
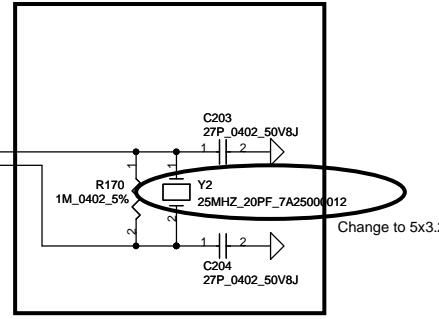
	LOW	HIGH
ID1	A & B	C test
GPI065	test	

PROJECT ID

ID2	ID1	ID0	PROJECT
GPI021	GPI065	GPI066	NEW70
0	0	0	NEW80
0	0	1	NEW90
0	1	0	
0	1	1	
1	0	0	

1. Connect Directly EXPRESS CARD, MINI1, MINI2
2. Level Shift1, Pull-Up to +3VS CLOCK GEN, DIMM1, DIMM2
3. Level Shift2, Pull-Up to +3VS LAN
4. Level Shift3, Pull-Up to +3VS CPU & PCH XDP

6/9 MOW23 Request add 25MHz crystal supporting Integrated Graphics



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<4> DMI_HTX_PRX_N[0..3] DMI_HTX_PRX_N[0..3]

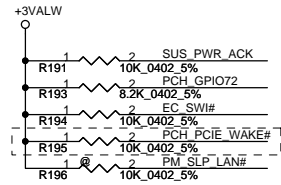
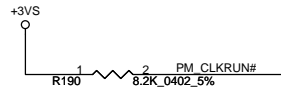
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<4> DMI_PTX_HRX_N[0..3] DMI_PTX_HRX_N[0..3]

<4> DMI_PTX_HRX_P[0..3] DMI_PTX_HRX_P[0..3]

<4> H_FDI_TXN[0..7] H_FDI_TXN[0..7]

<4> H_FDI_TXP[0..7] H_FDI_TXP[0..7]



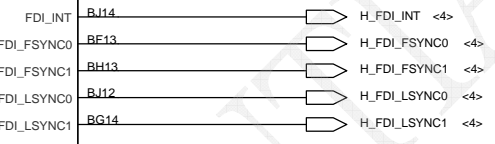
R195 Change to 10K for W37
20090916

U4C

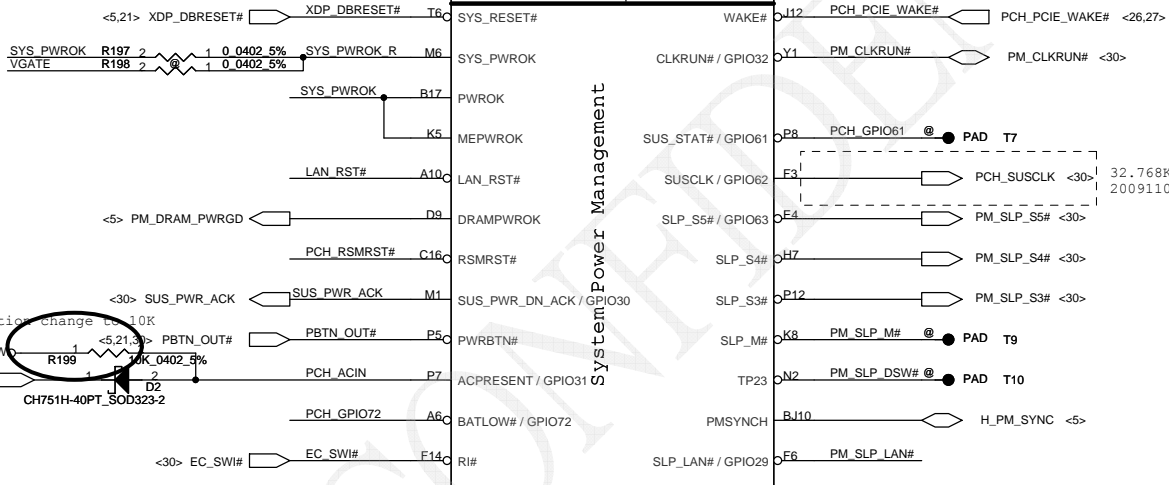
REV1.0

DMI_HTX_PRX_N0	BC24	DMI0RXN
DMI_HTX_PRX_N1	BJ22	DMI1RXN
DMI_HTX_PRX_N2	AW20	DMI2RXN
DMI_HTX_PRX_N3	BJ20	DMI3RXN
DMI_HTX_PRX_P0	BD24	DMI0RXP
DMI_HTX_PRX_P1	BC22	DMI1RXP
DMI_HTX_PRX_P2	BA20	DMI2RXP
DMI_HTX_PRX_P3	BG20	DMI3RXP
DMI_PTX_HRX_N0	BE22	DMI0TXN
DMI_PTX_HRX_N1	BF21	DMI1TXN
DMI_PTX_HRX_N2	BD20	DMI2TXN
DMI_PTX_HRX_N3	BE18	DMI3TXN
DMI_PTX_HRX_P0	BD22	DMI0TXP
DMI_PTX_HRX_P1	BH21	DMI1TXP
DMI_PTX_HRX_P2	BC20	DMI2TXP
DMI_PTX_HRX_P3	BD18	DMI3TXP

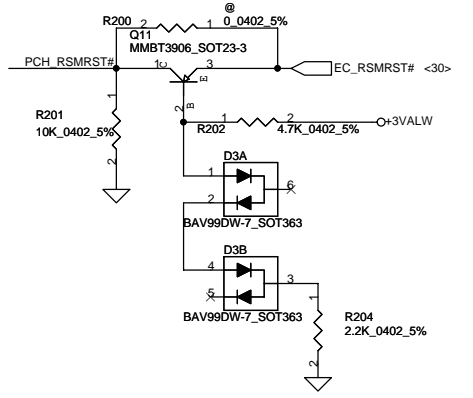
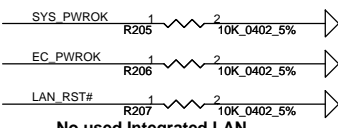
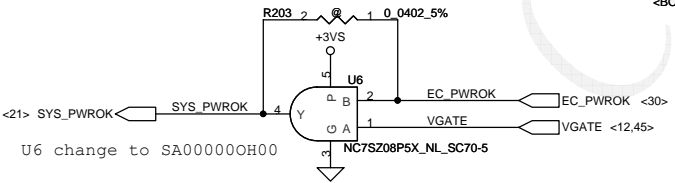
FDI_RXN0	BA18	H_FDI_TXN0
FDI_RXN1	BA17	H_FDI_TXN1
FDI_RXN2	BD16	H_FDI_TXN2
FDI_RXN3	BJ16	H_FDI_TXN3
FDI_RXN4	BA16	H_FDI_TXN4
FDI_RXN5	BE14	H_FDI_TXN5
FDI_RXN6	BA14	H_FDI_TXN6
FDI_RXN7	BC12	H_FDI_TXN7
FDI_RXP0	BB18	H_FDI_TXP0
FDI_RXP1	BE17	H_FDI_TXP1
FDI_RXP2	BC16	H_FDI_TXP2
FDI_RXP3	BG16	H_FDI_TXP3
FDI_RXP4	AW16	H_FDI_TXP4
FDI_RXP5	BD14	H_FDI_TXP5
FDI_RXP6	BB14	H_FDI_TXP6
FDI_RXP7	BD12	H_FDI_TXP7



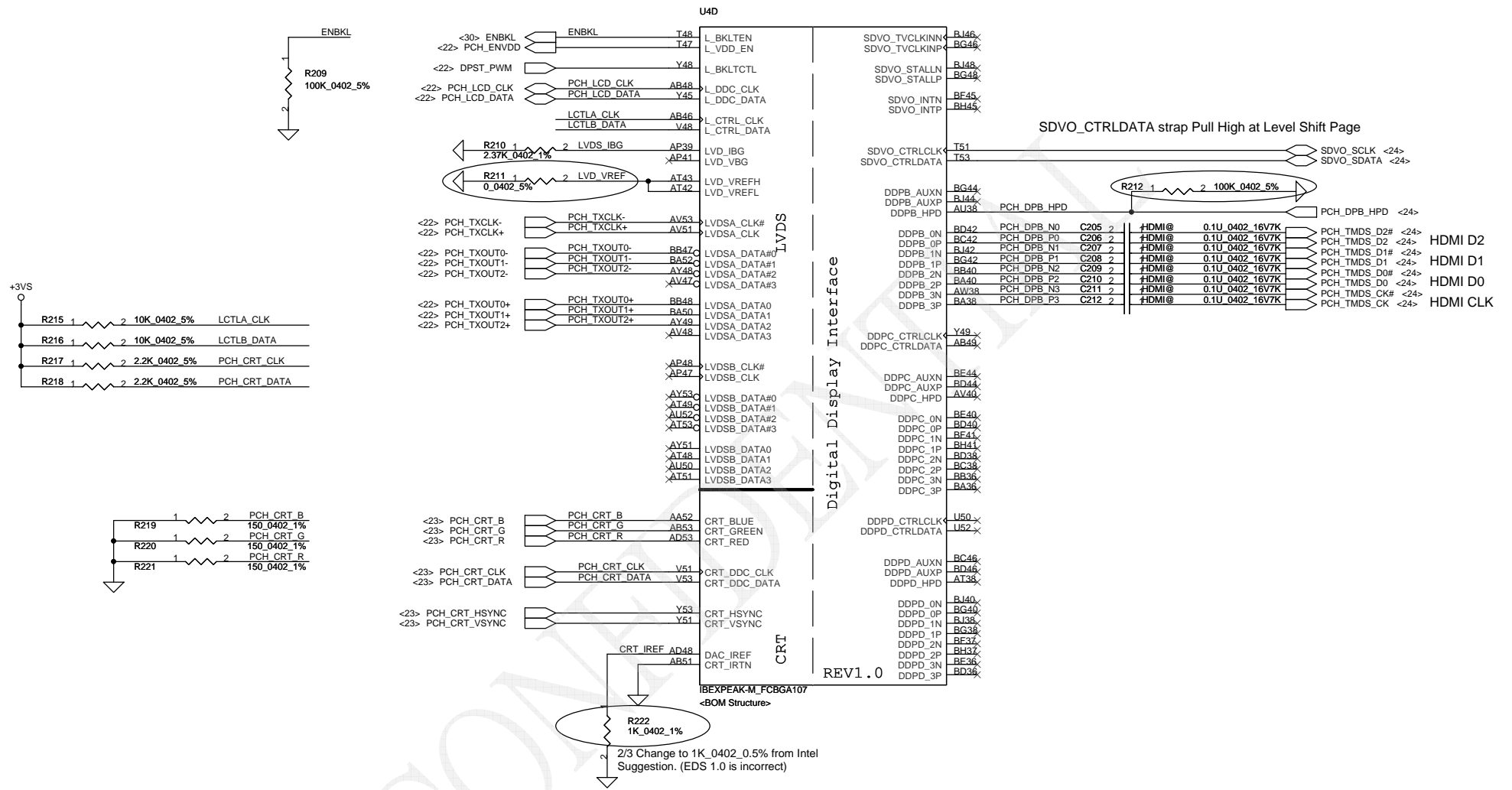
System Power Management



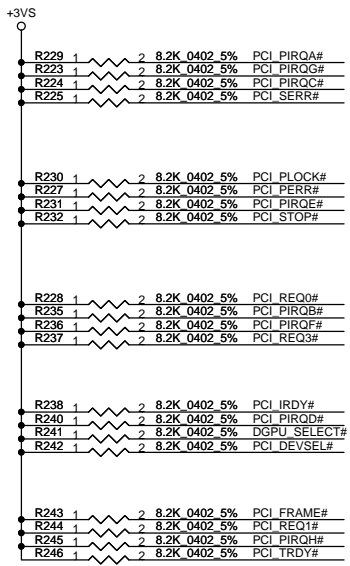
32.768KHZ ouput for remove EC crystal
20091103



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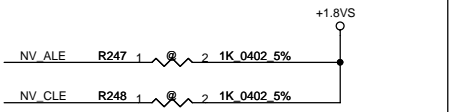
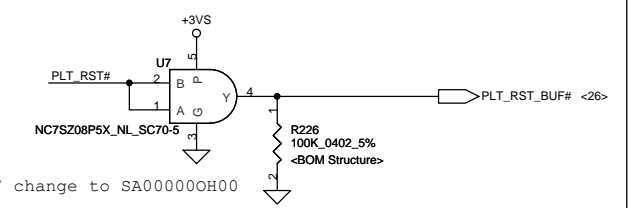
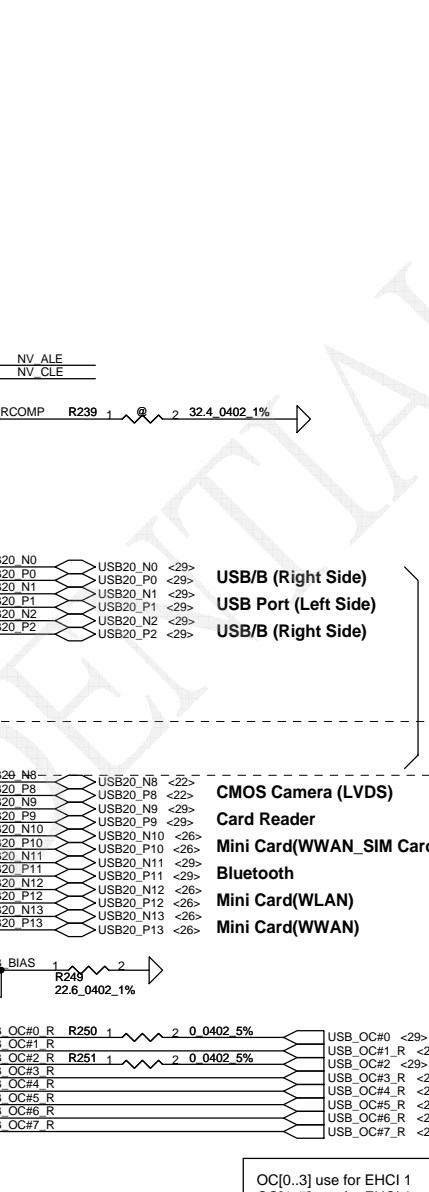
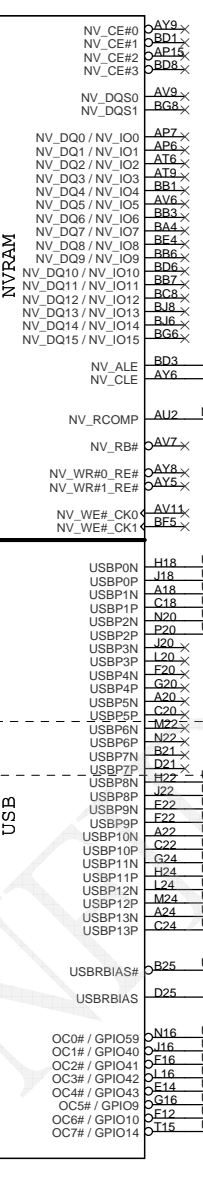
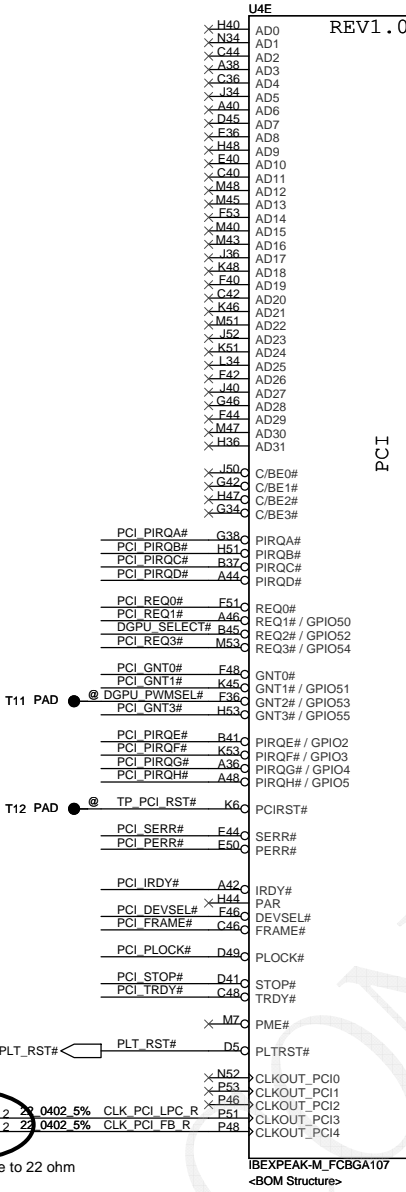


A16 swap override Strap/Top-Block Swap Override jumper

Low=A16 swap override/Top-Block Swap Override enabled
High=Default *

PCI_GNT3#

Low=A16 swap override/Top-Block Swap Override enabled
High=Default *



Intel Anti-Theft Technology	
NV_ALE	High=Enabled Low=Disableable(floating) *

DMI Termination Voltage	
NV_CLE	Set to Vcc when HIGH Set to Vss when LOW

NV_ALE
Enable Intel Anti-Theft Technology: 8.2K PU to +3VS

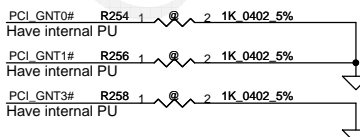
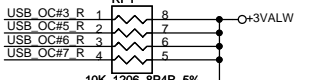
Disable Intel Anti-Theft Technology: floating(internal PD)

NV_CLE
DMI termination voltage.
weak internal PU, don't PD

EHCI 1

2/10 USB6, USB7 not support on HM55

EHCI 2



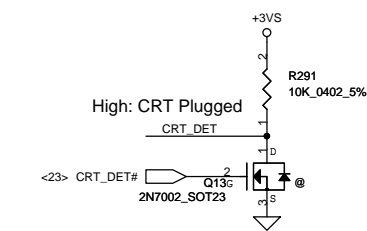
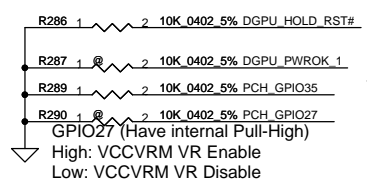
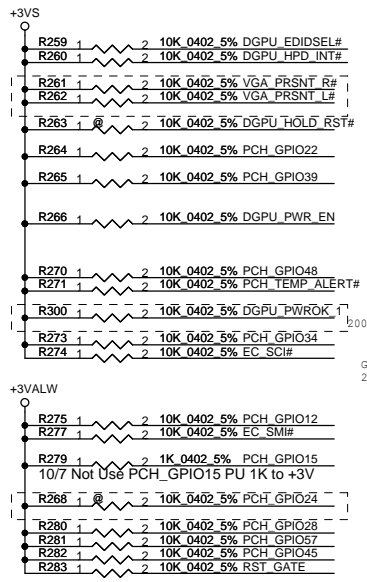
Boot BIOS Strap		
PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

A16 swap override Strap/Top-Block Swap Override jumper

PCI_GNT#3 Low = A16 swap High = Default

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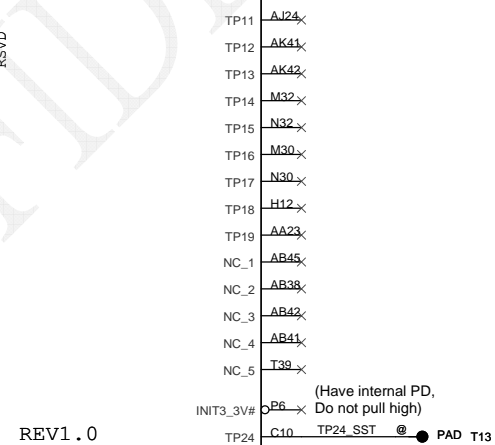
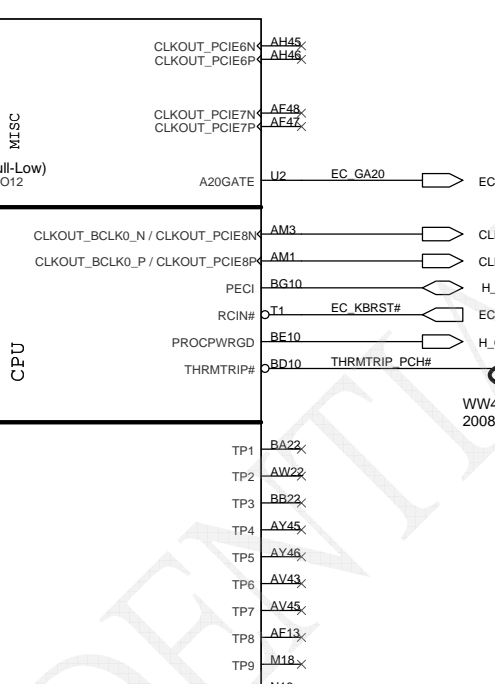
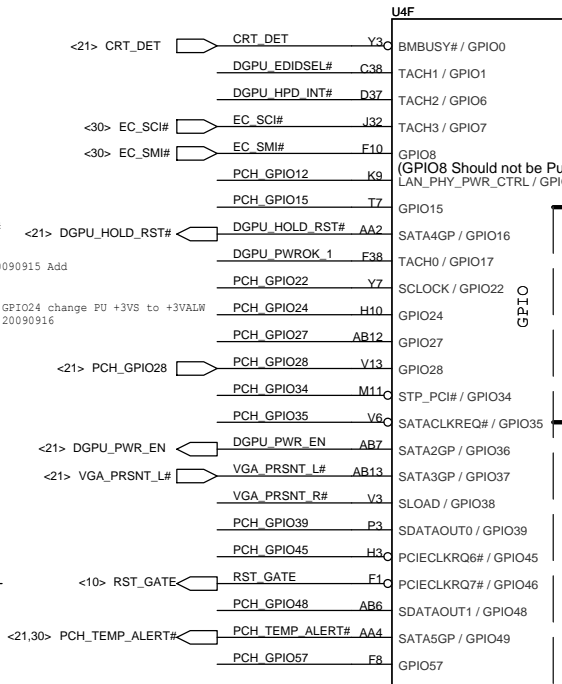
Compal Electronics, Inc.	
Title	SCHMATICS,MB A5892
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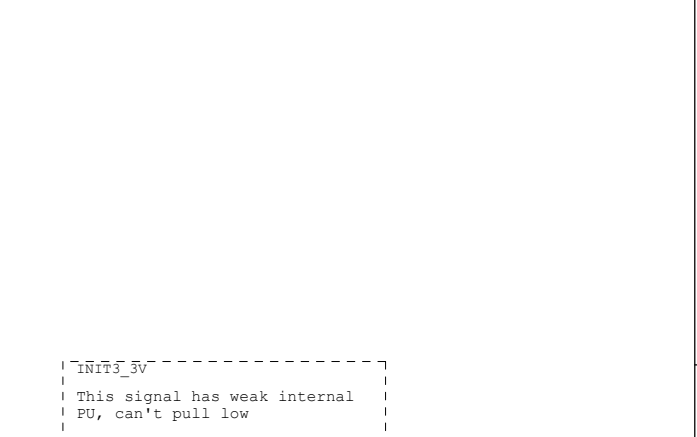
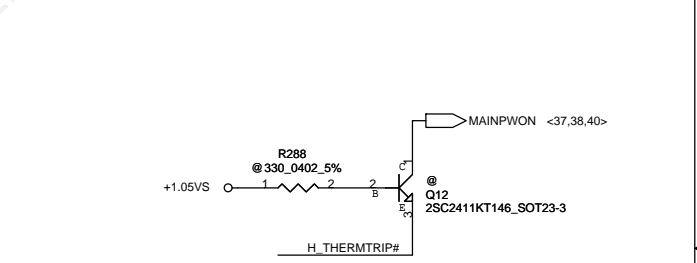
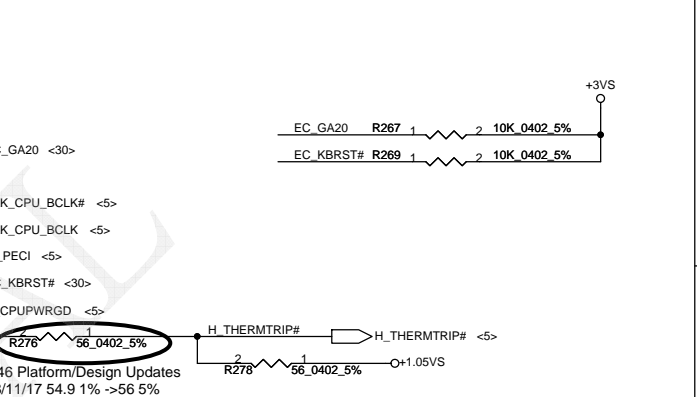
GPI027
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
* H: On-Die voltage regulator enable
L: On-Die PLL Voltage Regulator disable

GPI08
This signal has a weak internal pull up
can't Pull low

GPI015
L: Intel ME Crypto Transport Layer Security(TLS) chiper suite with no confidentiality
H: Intel ME Crypto Transport Layer Security(TLS) chiper suite with confidentiality
It have weak internal PU 20K

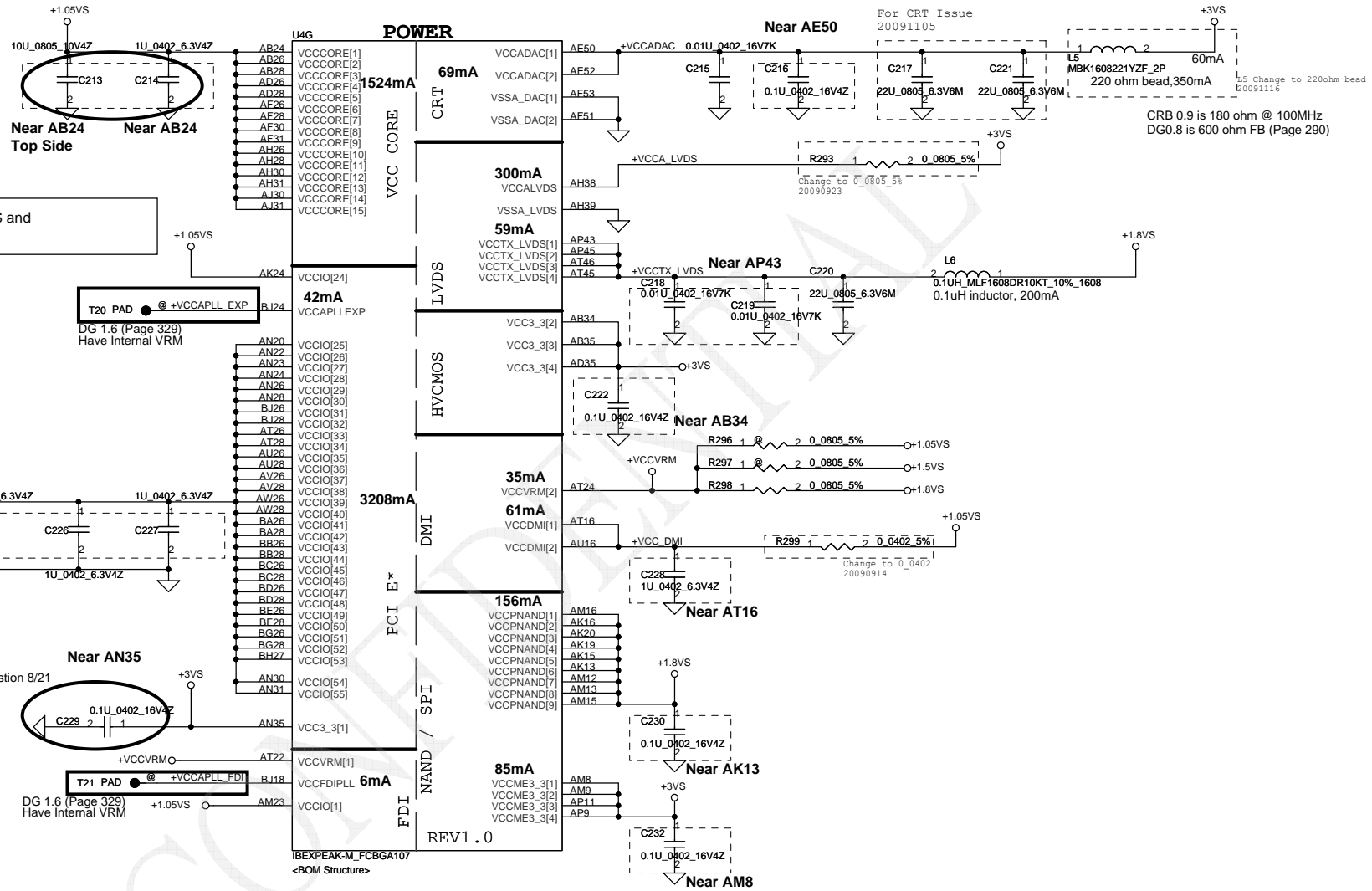


IBEXPEAK-M_FCBGA107
REV1.0
<BOM Structure>



INIT3_3V
This signal has weak internal PU, can't pull low

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Intel suggest follow CRB 8/21

All Ibox Peak-M Power rails with netnames +1.1VS and +1.1V rails are actually +1.05VS and +1.05V rails

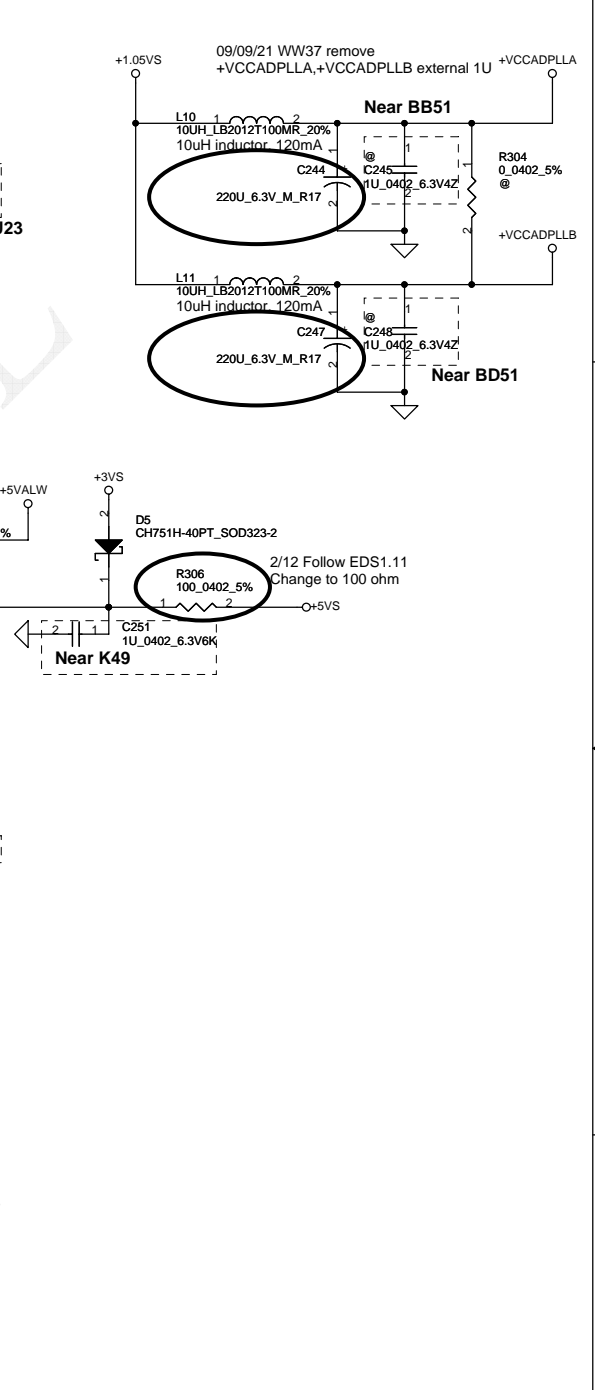
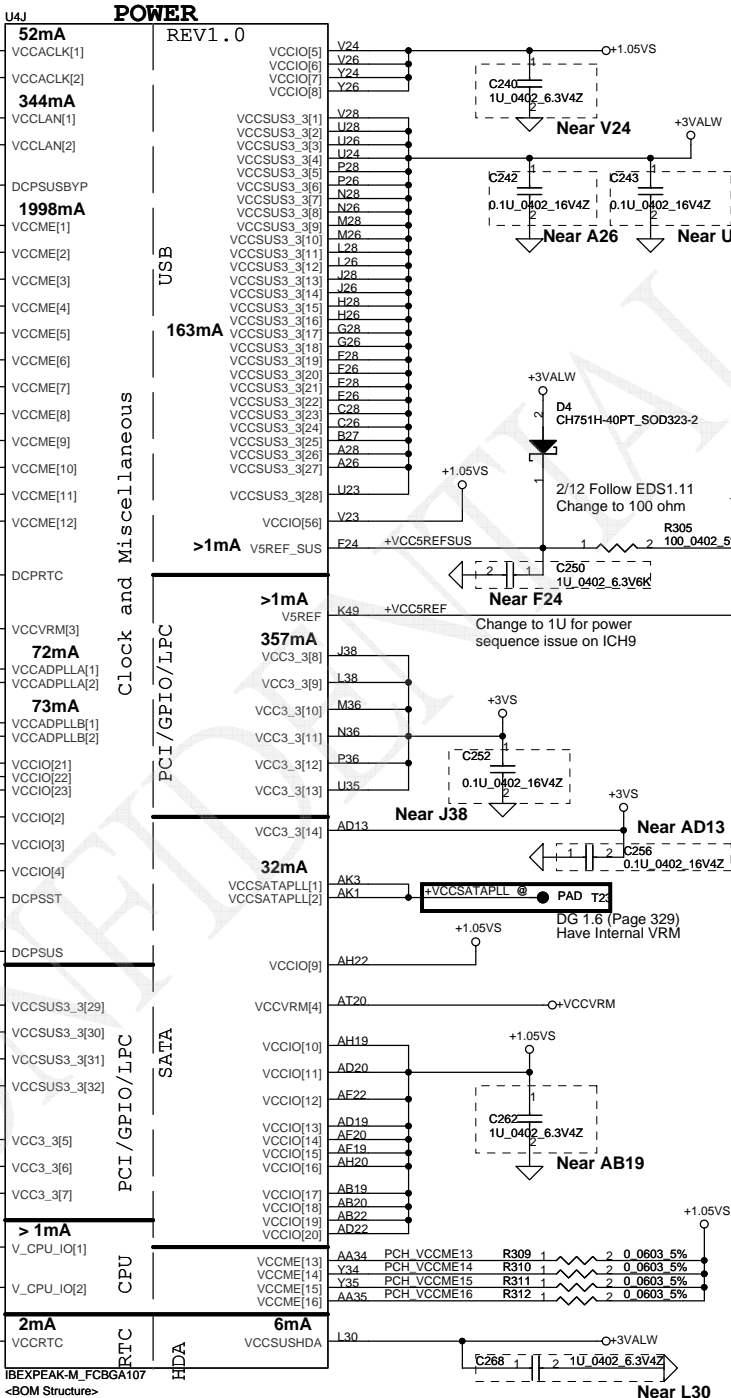
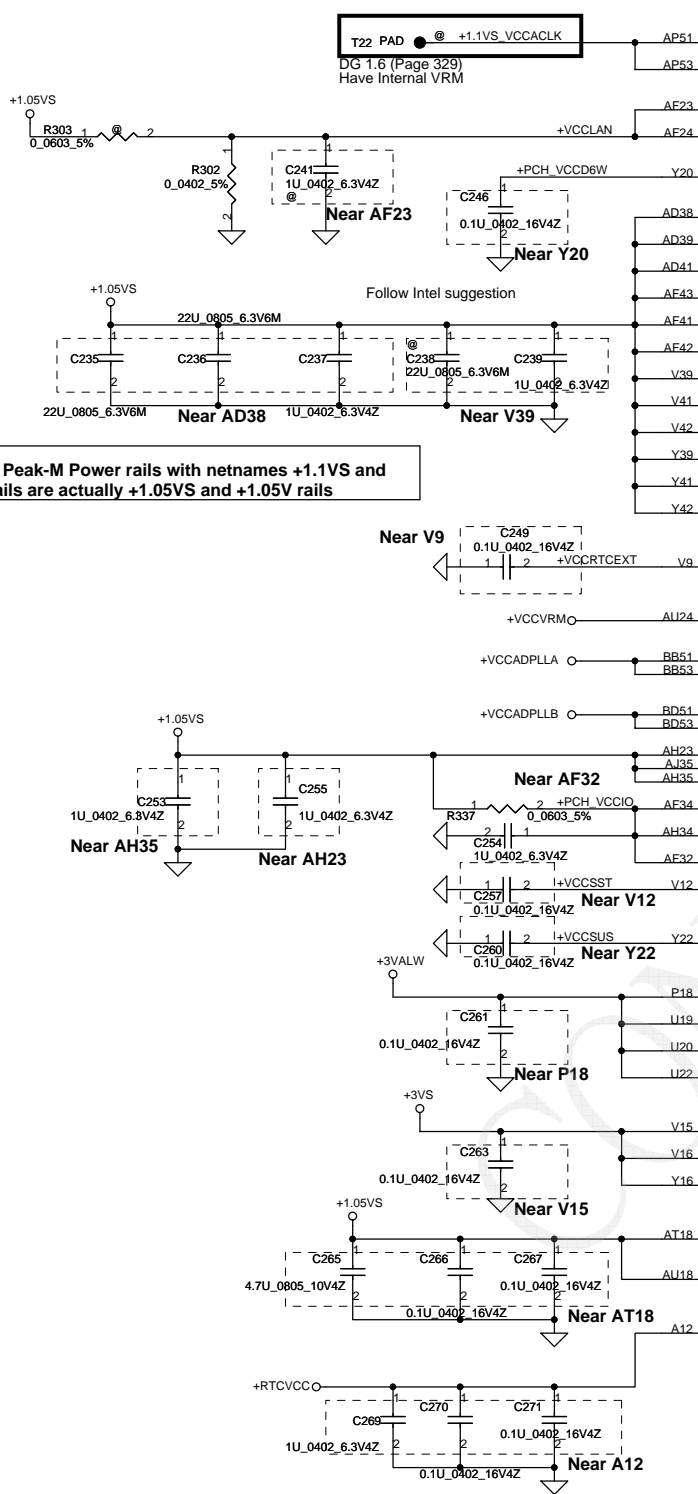
T20 PAD @ +VCCAPLL EXP
 DG 1.6 (Page 329)
 Have Internal VRM

Near AN35
 Follow Intel suggestion 8/21
 T21 PAD @ +VCCAPLL FDI
 DG 1.6 (Page 329)
 Have Internal VRM

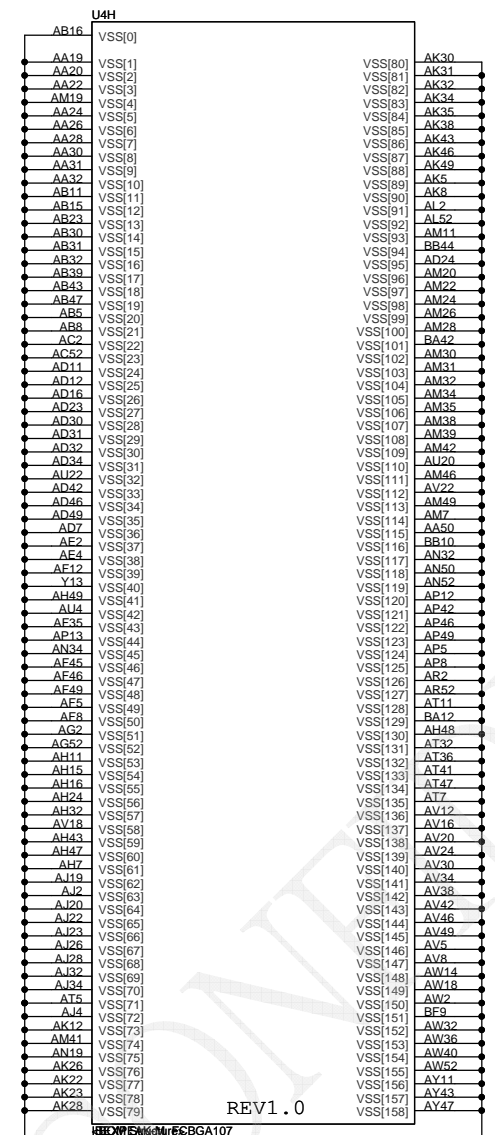
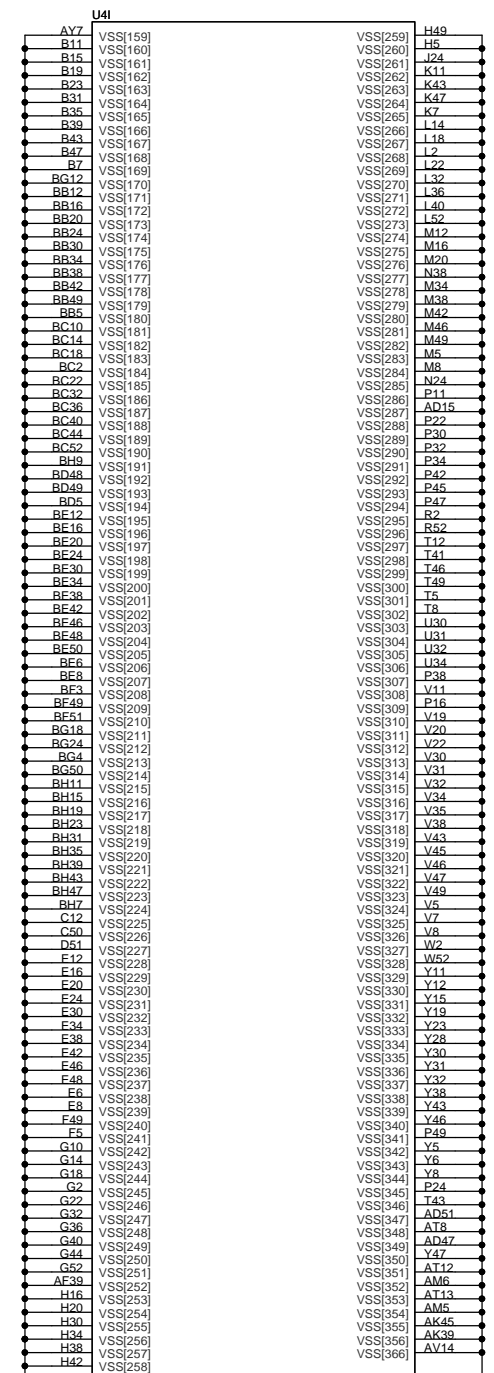
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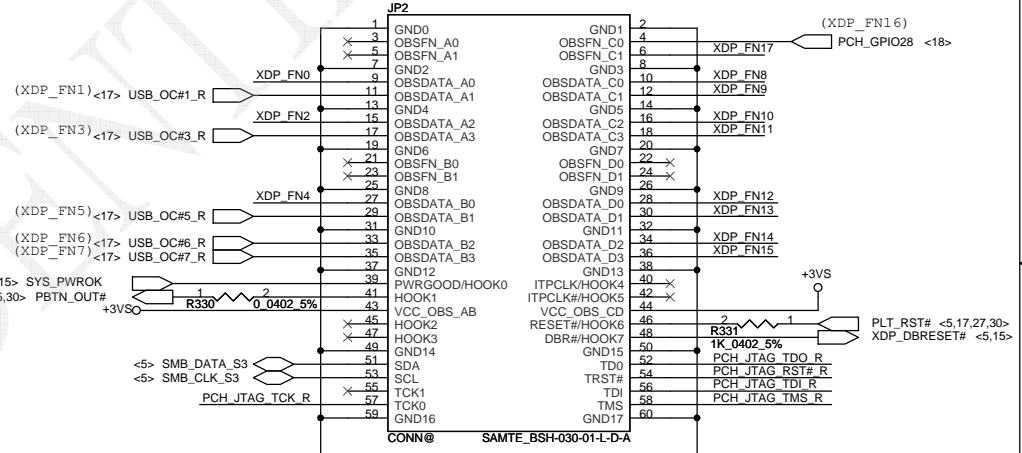
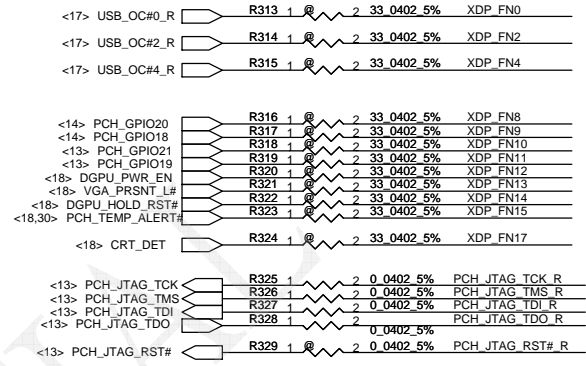
All Ibox Peak-M Power rails with netnames +1.1VS and +1.1V rails are actually +1.05VS and +1.05V rails



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PCH XDP Port

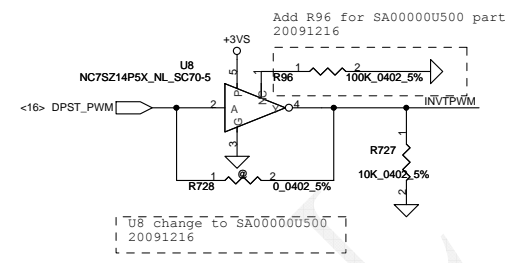
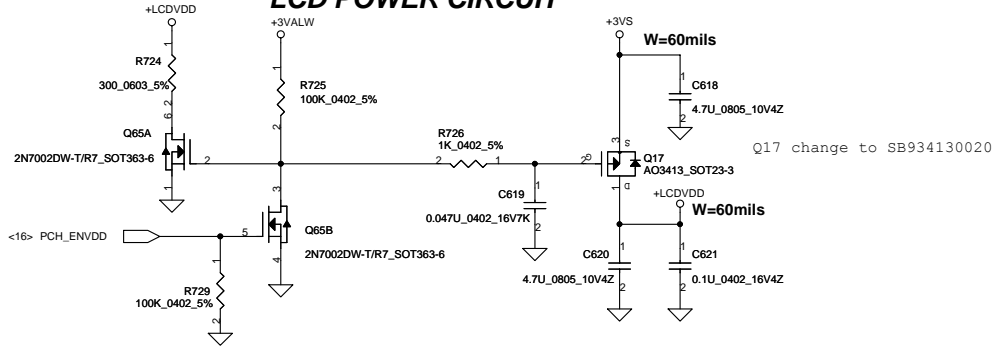


REV1.0

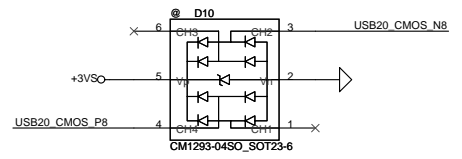
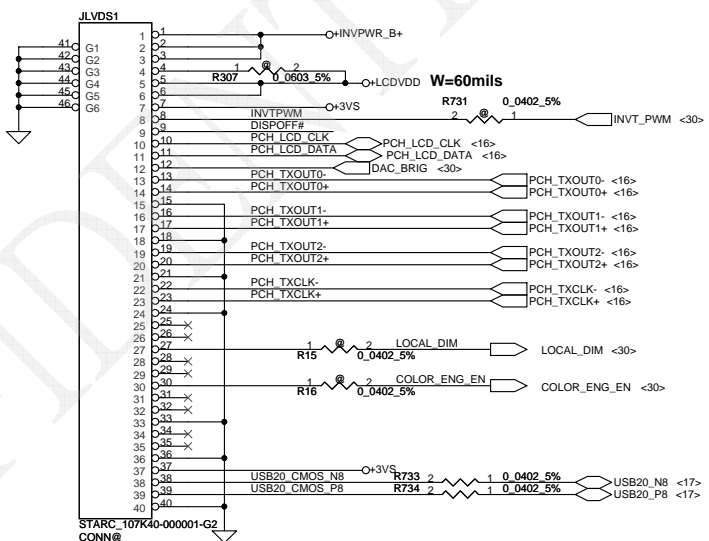
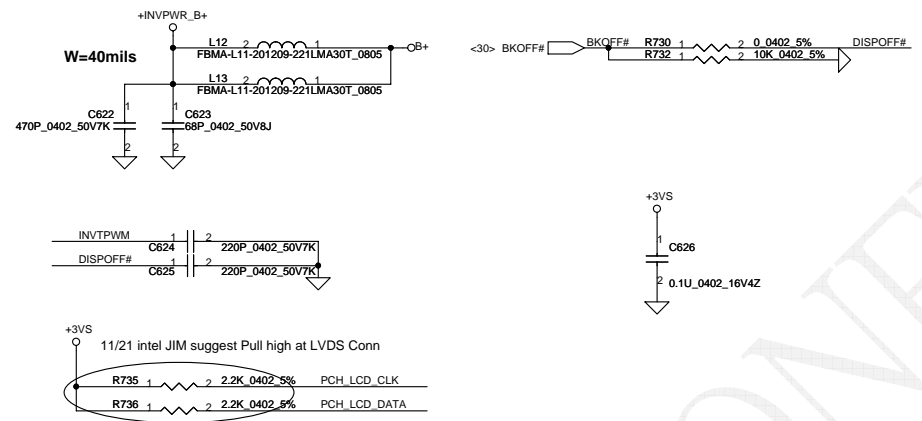
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LCD POWER CIRCUIT

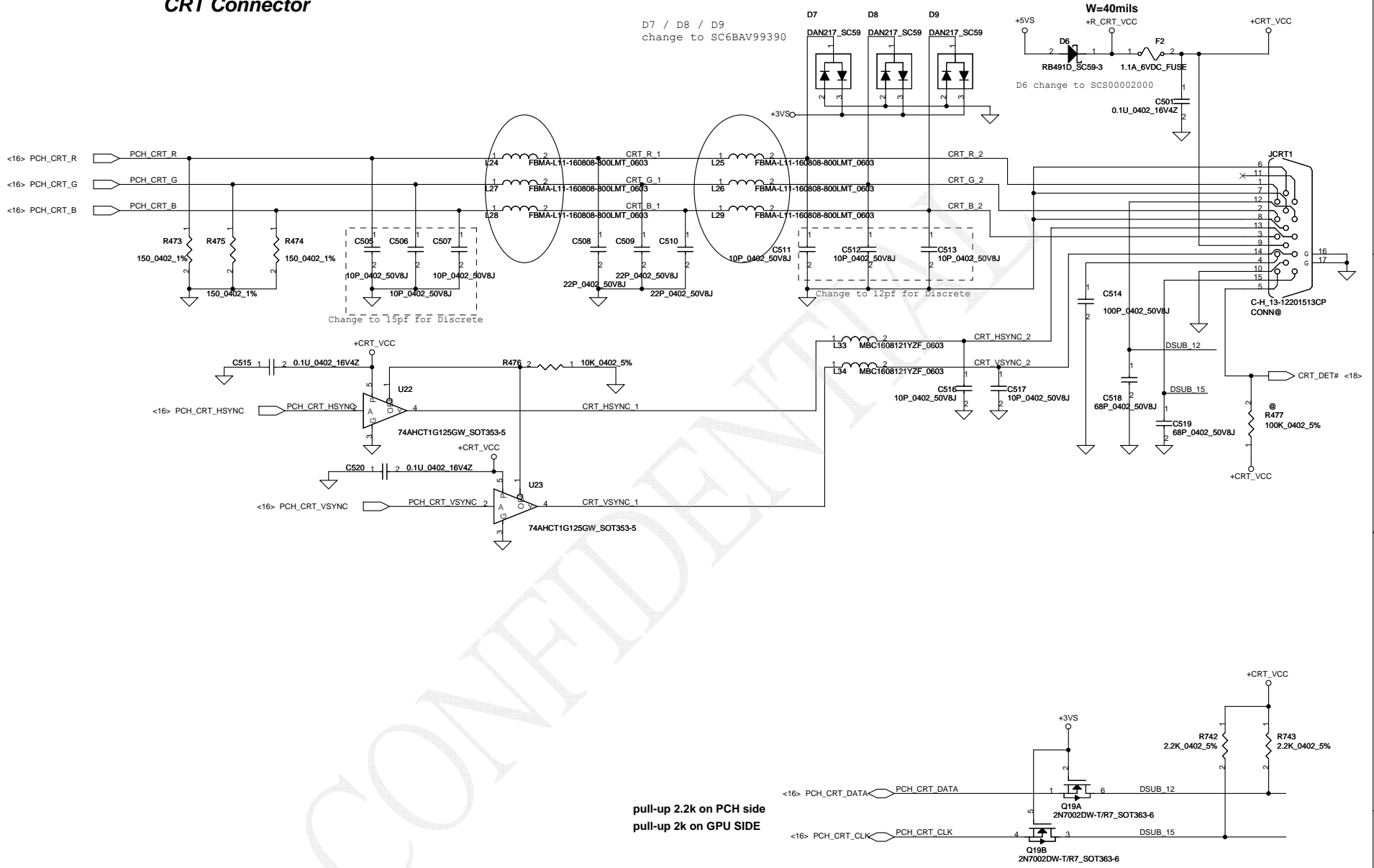


LED PANEL Conn.

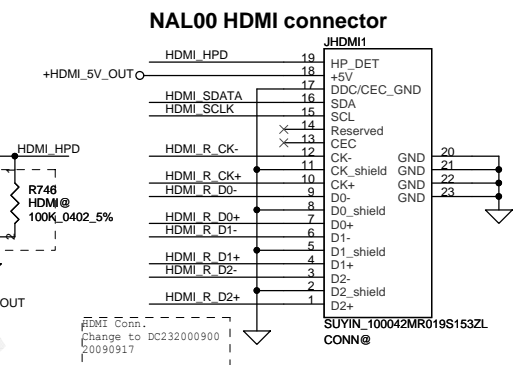
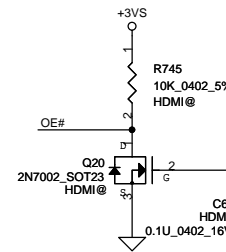
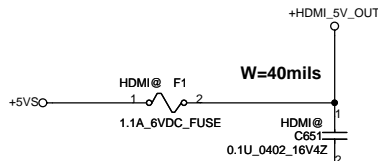
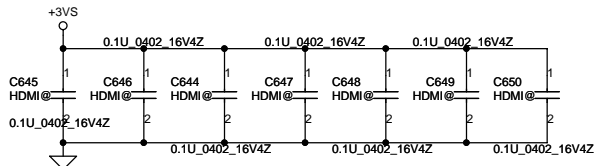


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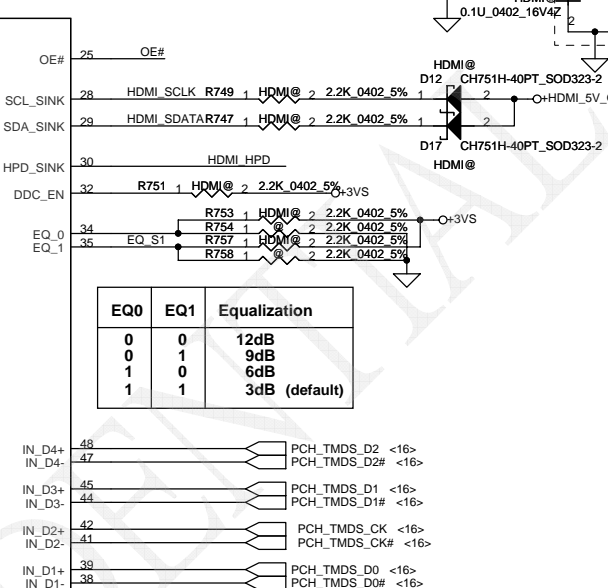
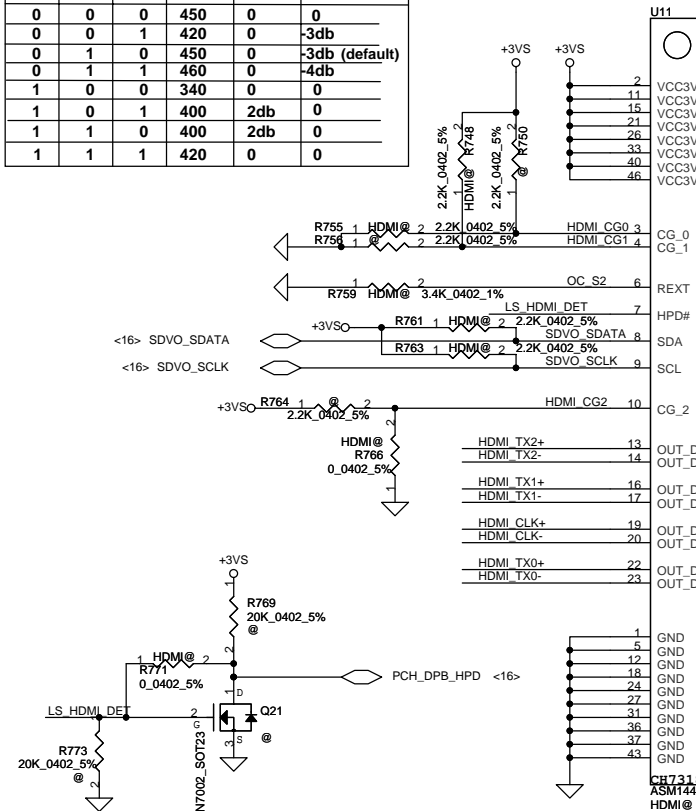
CRT Connector



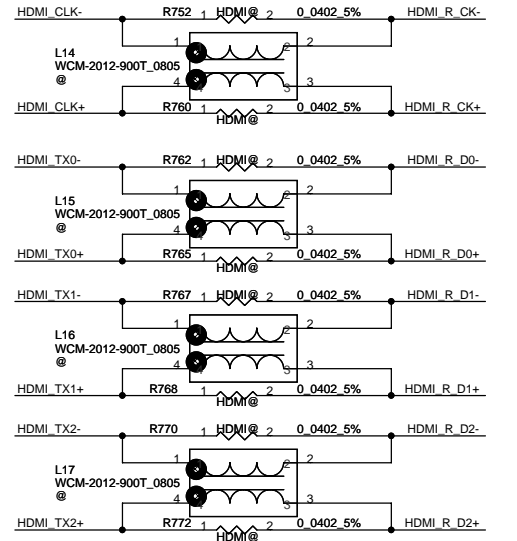
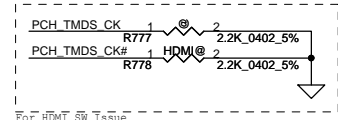
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CG0	CG1	CG2	Swing	Pre-amp	Slew-rate
0	0	0	450	0	0
0	0	1	420	0	-3db
0	1	0	450	0	-3db (default)
0	1	1	460	0	-4db
1	0	0	340	0	0
1	0	1	400	2db	0
1	1	0	400	2db	0
1	1	1	420	0	0

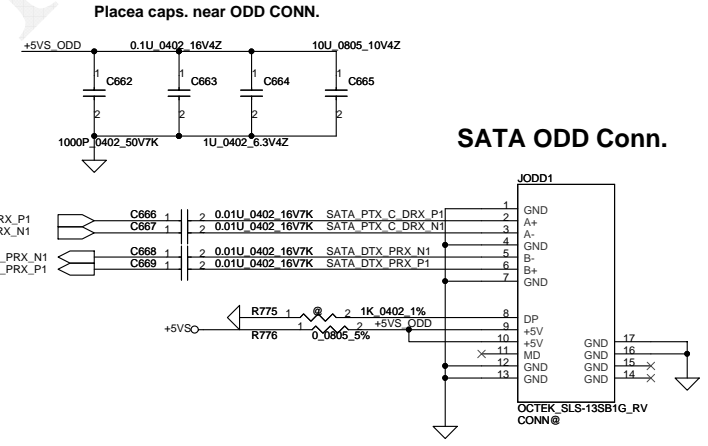
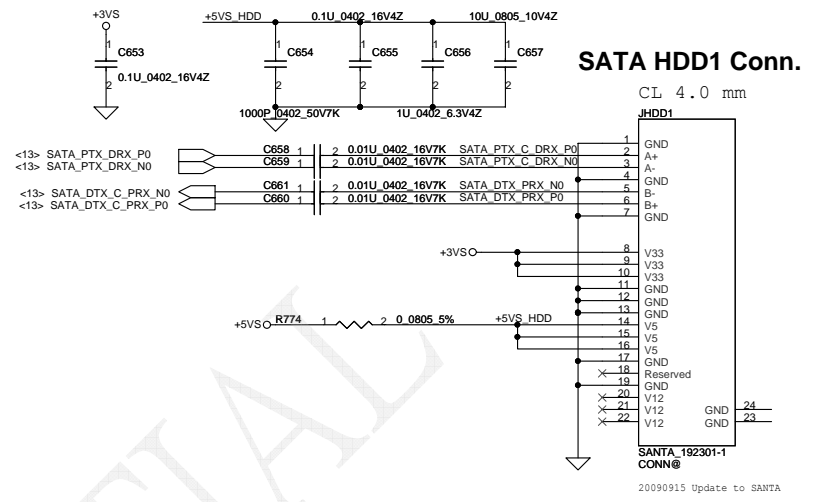
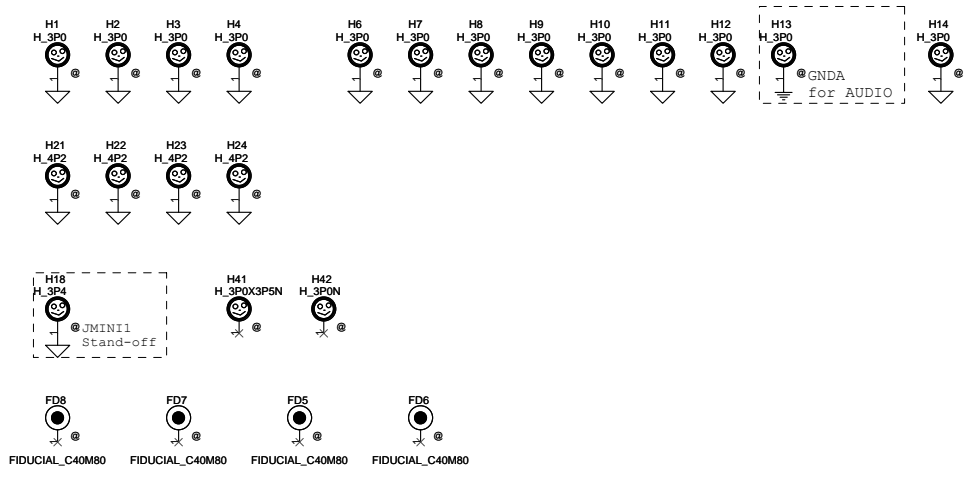


EQ0	EQ1	Equalization
0	0	12dB
0	1	9dB
1	0	6dB
1	1	3dB (default)



CH7319C-BF PN: SA00001U920
 ASM1442T_QFN48_TX1
 HDMI@ default is ASM1442 p/n: SA00003GT00

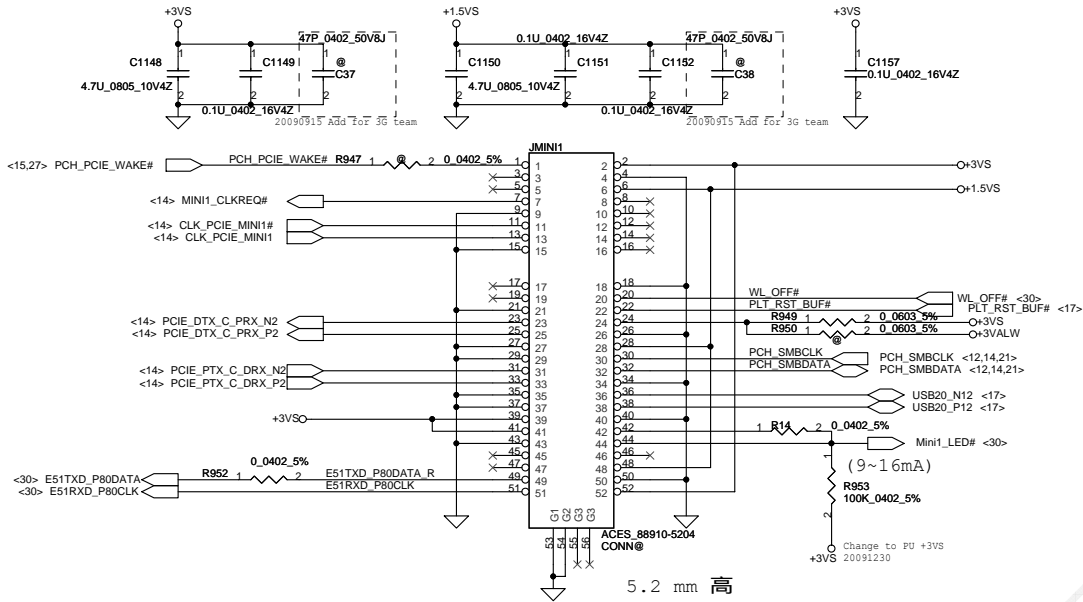
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CONFIDENTIAL

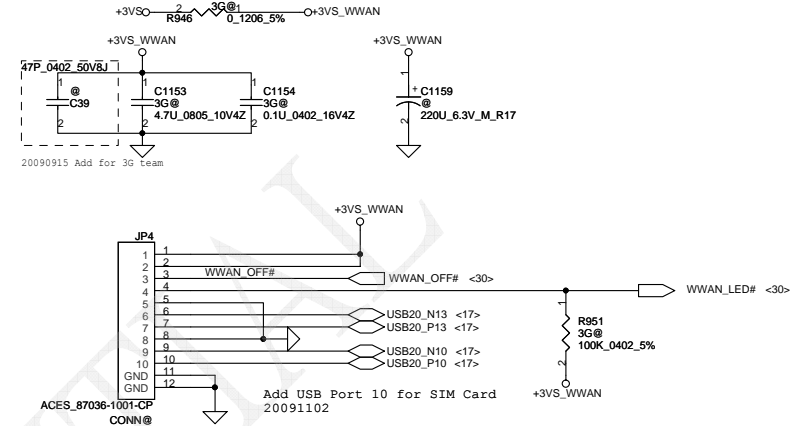
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For Wireless LAN

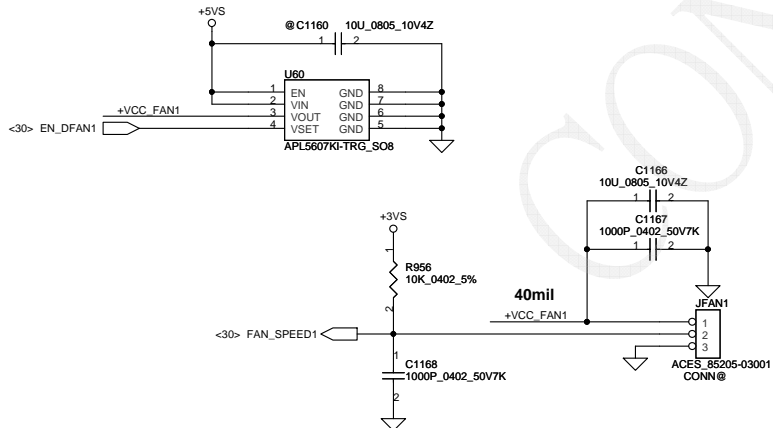


Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

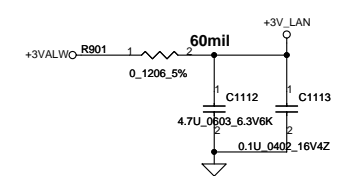
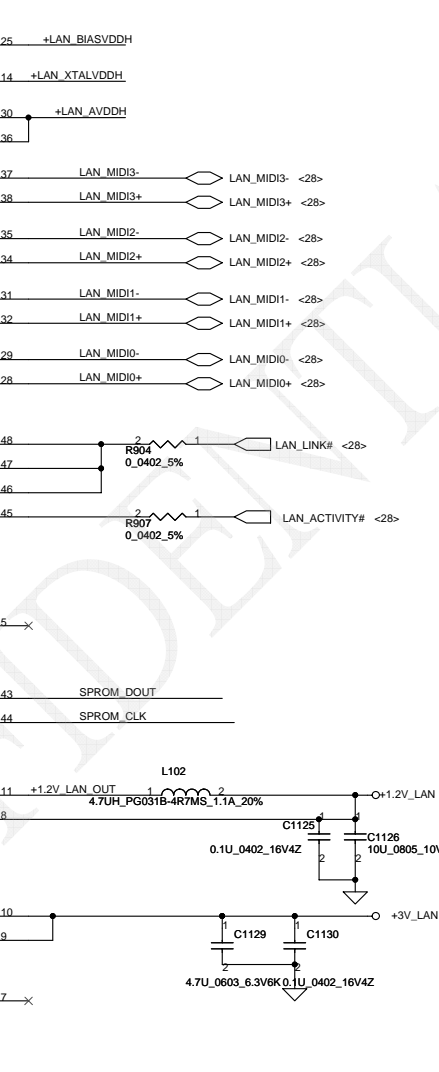
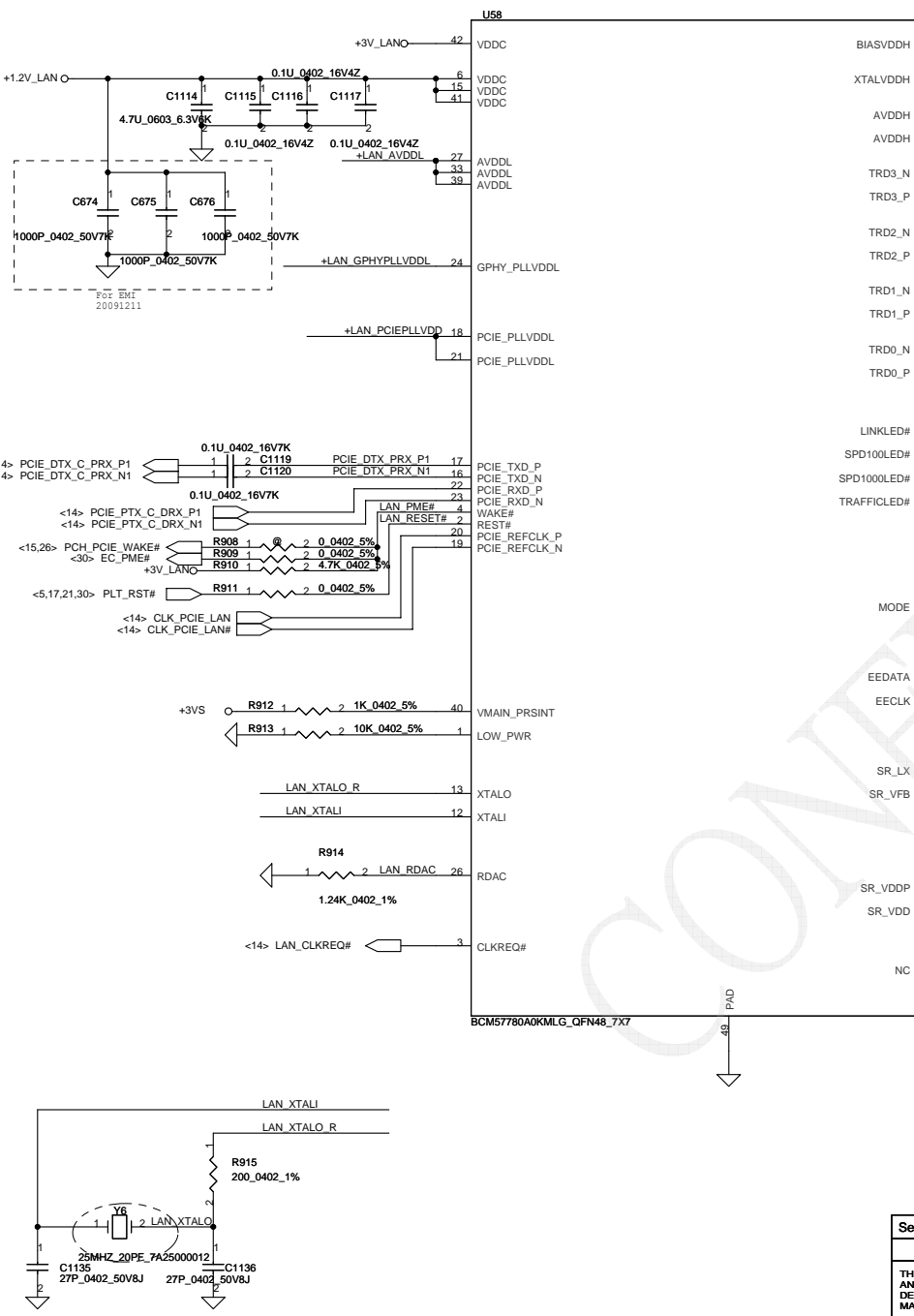
To 3G / GPS Module Connect



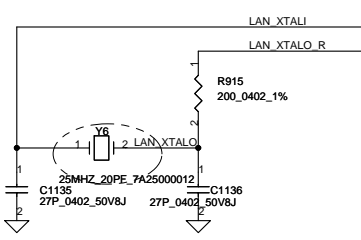
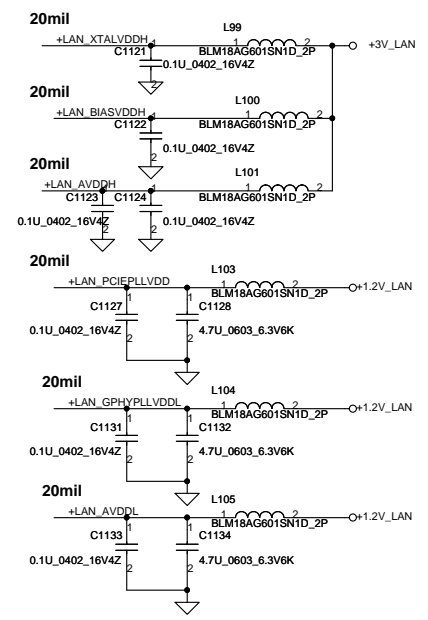
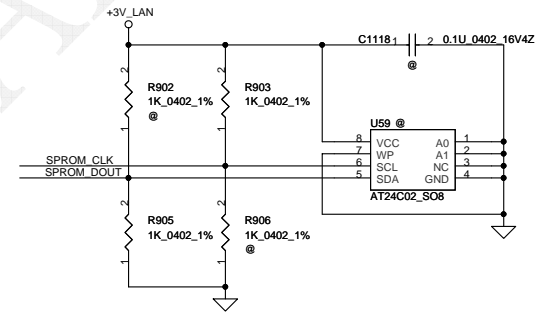
FAN1 Conn



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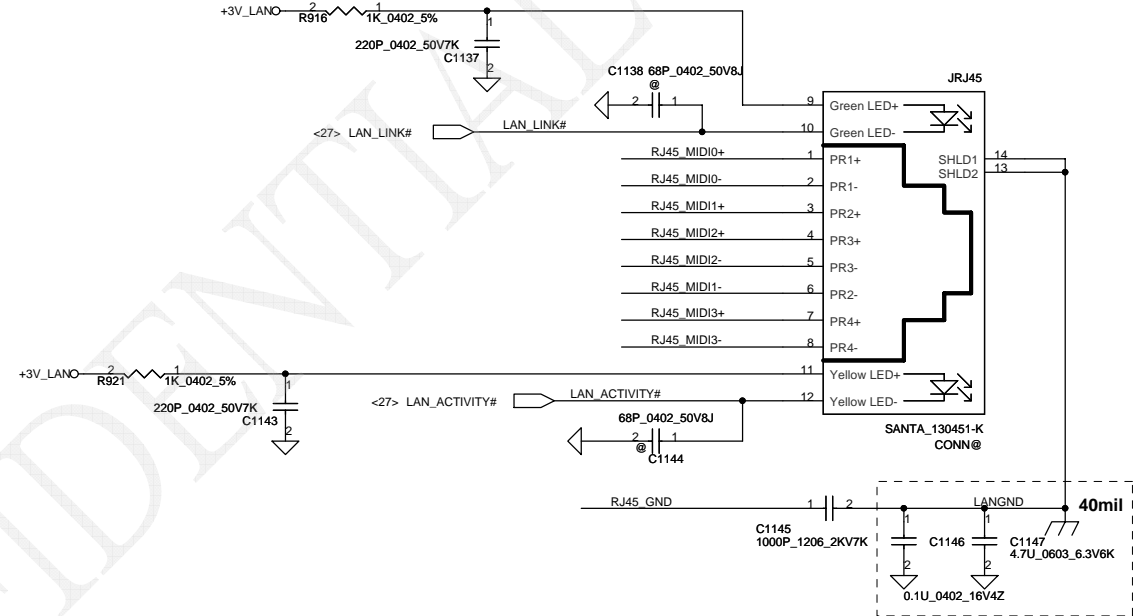
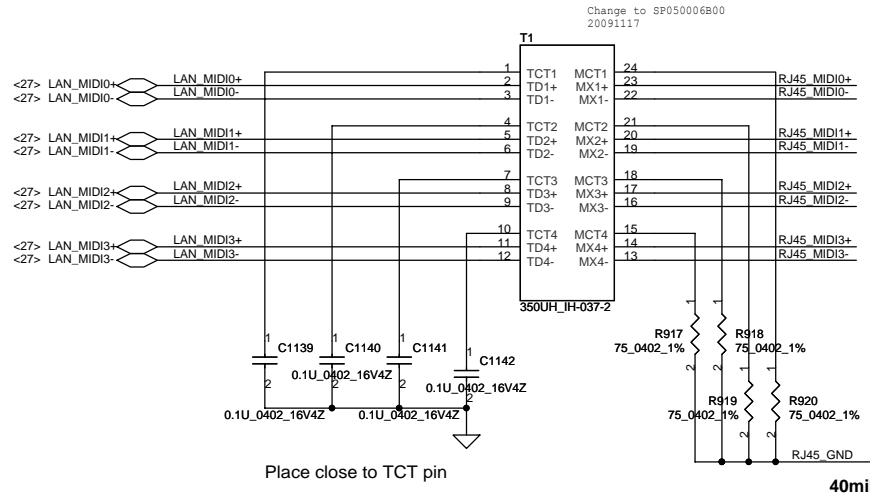


	SPROM_CLK (RECLK)	SPROM_DOUT (EEDATA)
On chip	1	0
AT24C02	1	1



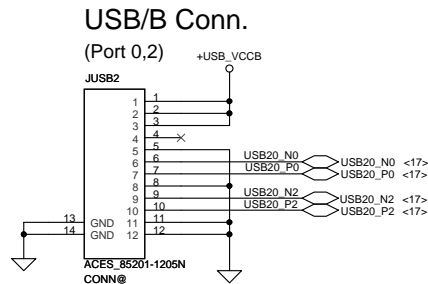
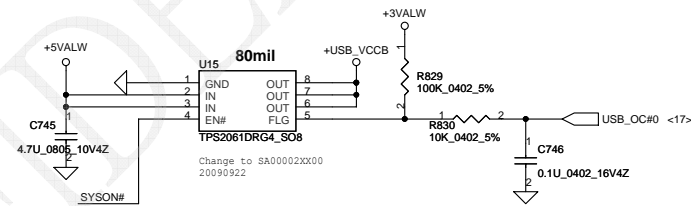
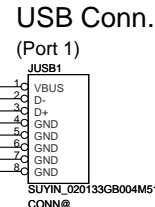
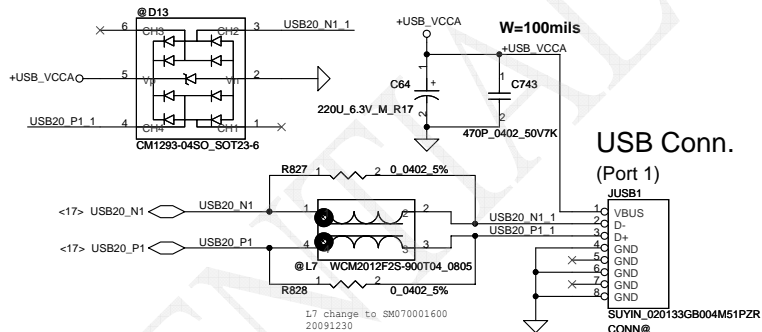
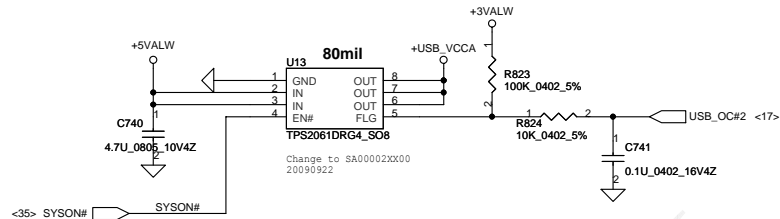
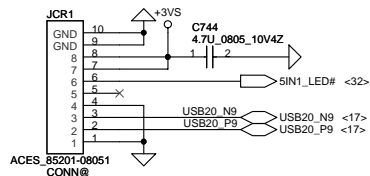
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LAN Connector

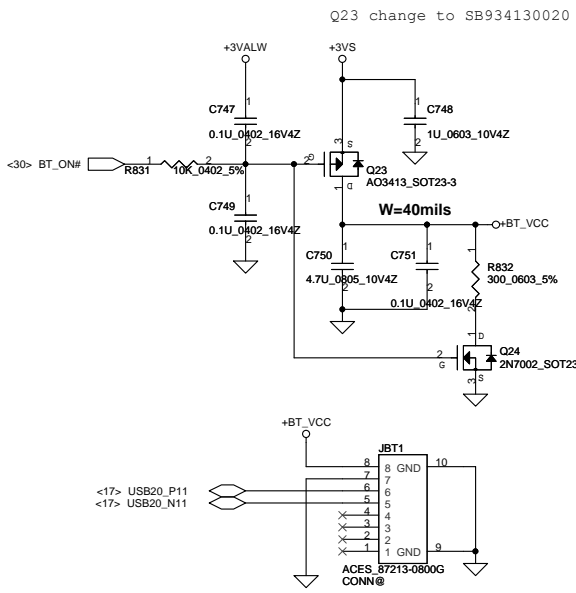


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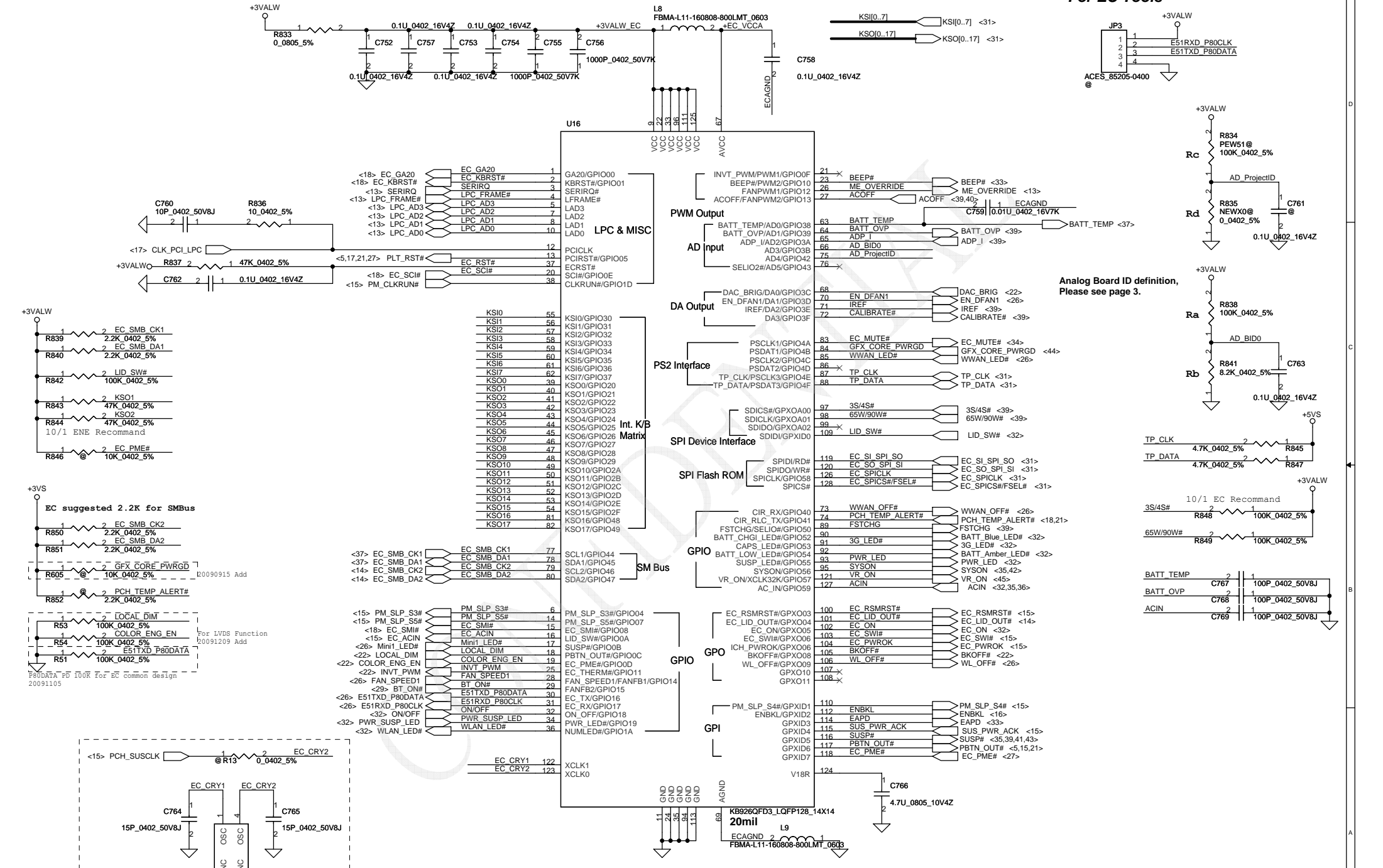
Card Reader Conn.



Bluetooth Conn.

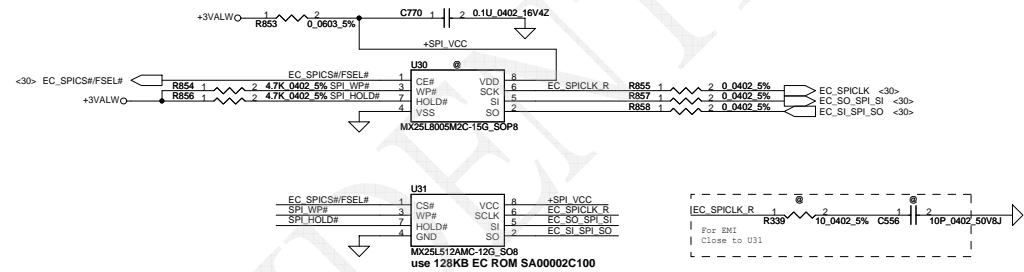
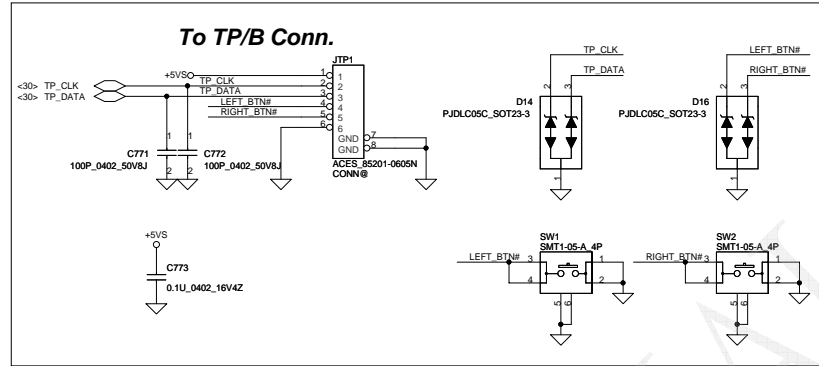
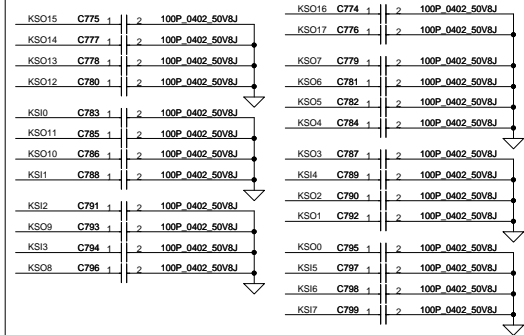
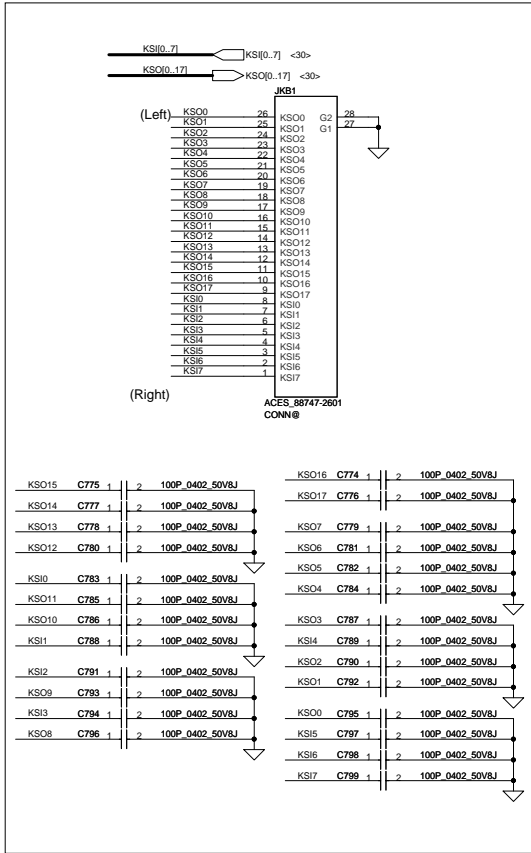


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Analog Board ID definition, Please see page 3.

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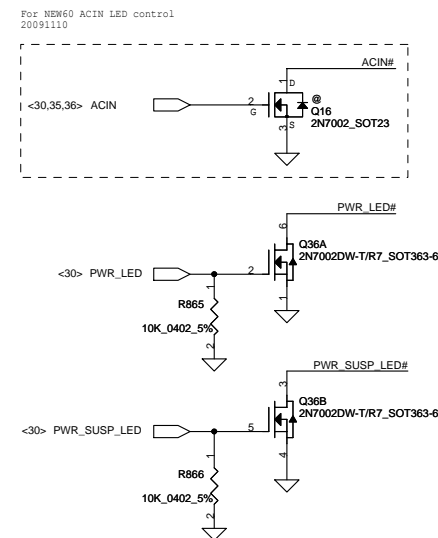
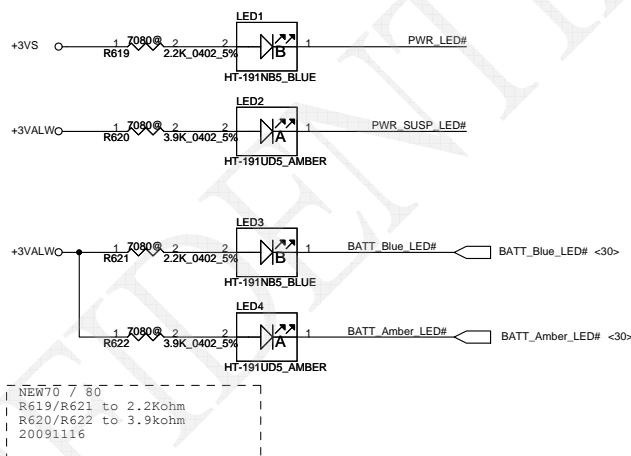
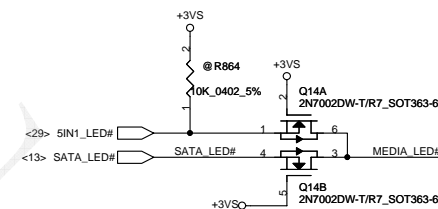
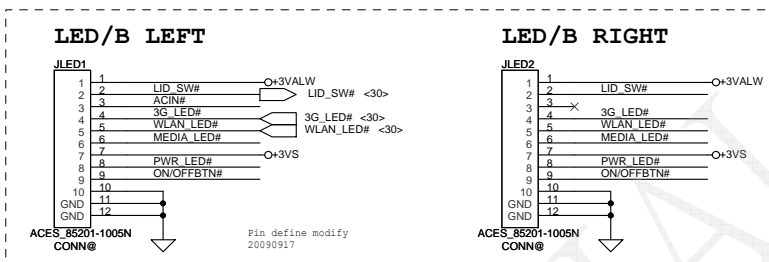
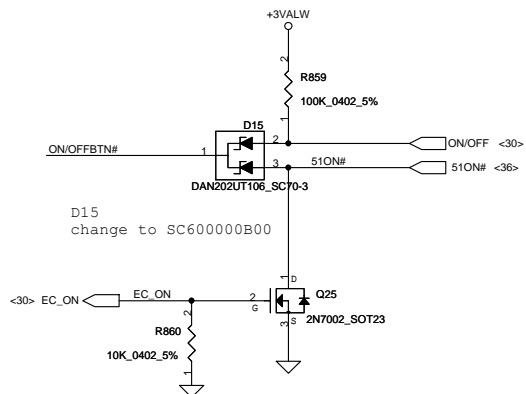


ENE suggestion SPI Frequency over 66MHz
SST: 50MHz
MXIC: 70MHz
ST: 40MHz

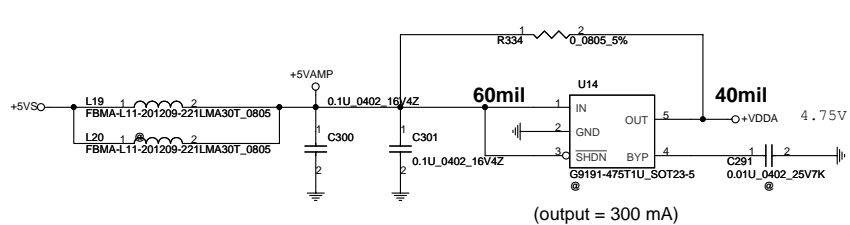
To BTN/B Conn.

KSO0	KSO3
KSI1 WL_BTN#	Program_BTN#
KSI2 T/P lock_BTN#	
KSI3 Back up_BTN#	Volum up_BTN#
KSI4 BT_BTN#	Volum down_BTN#
KSI5 Power save_BTN#	

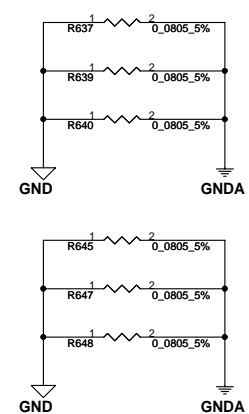
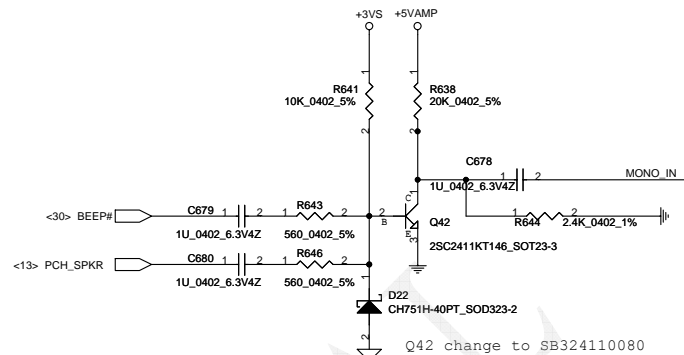
Power Button



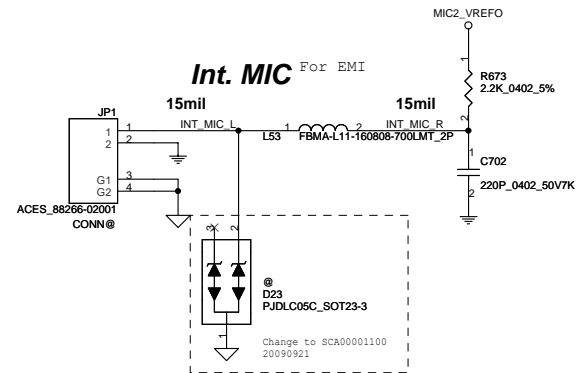
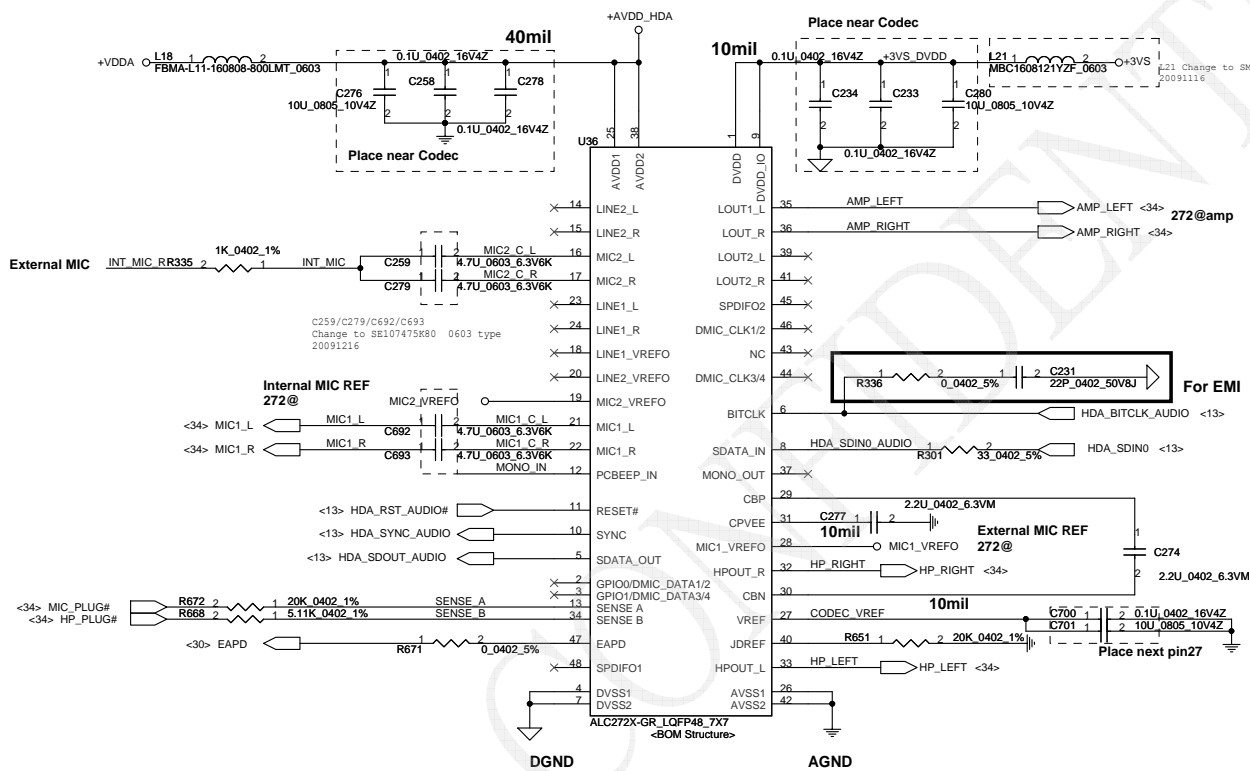
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(output = 300 mA)

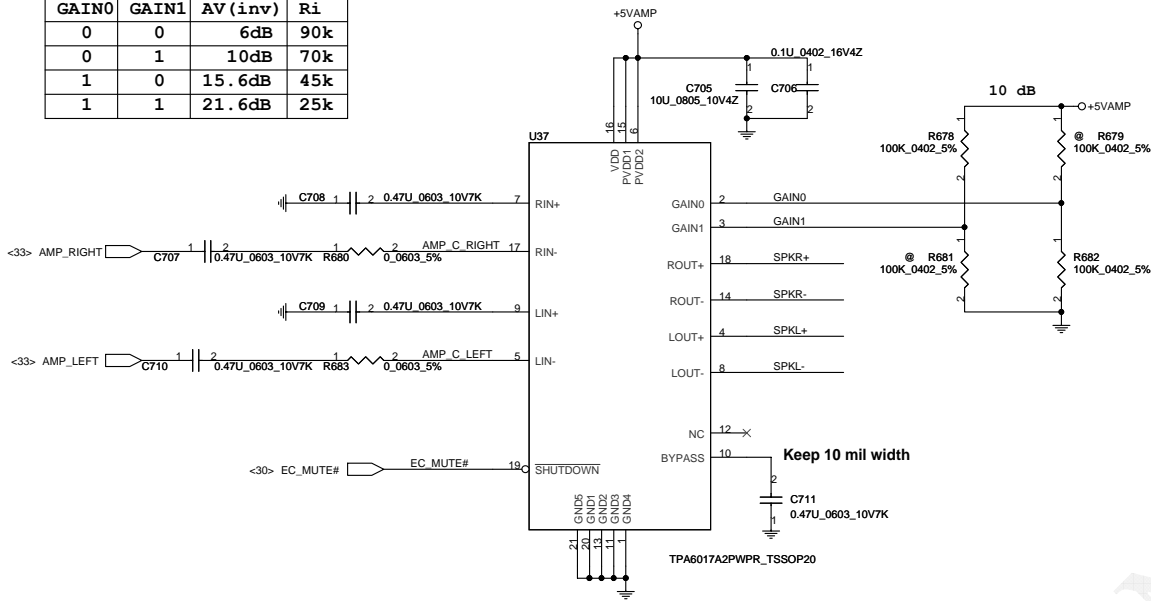


HD Audio Codec

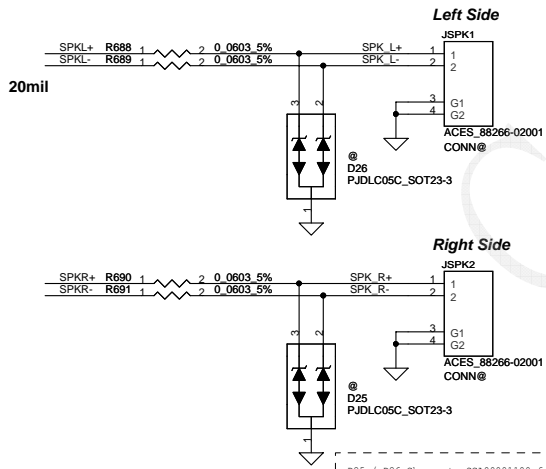


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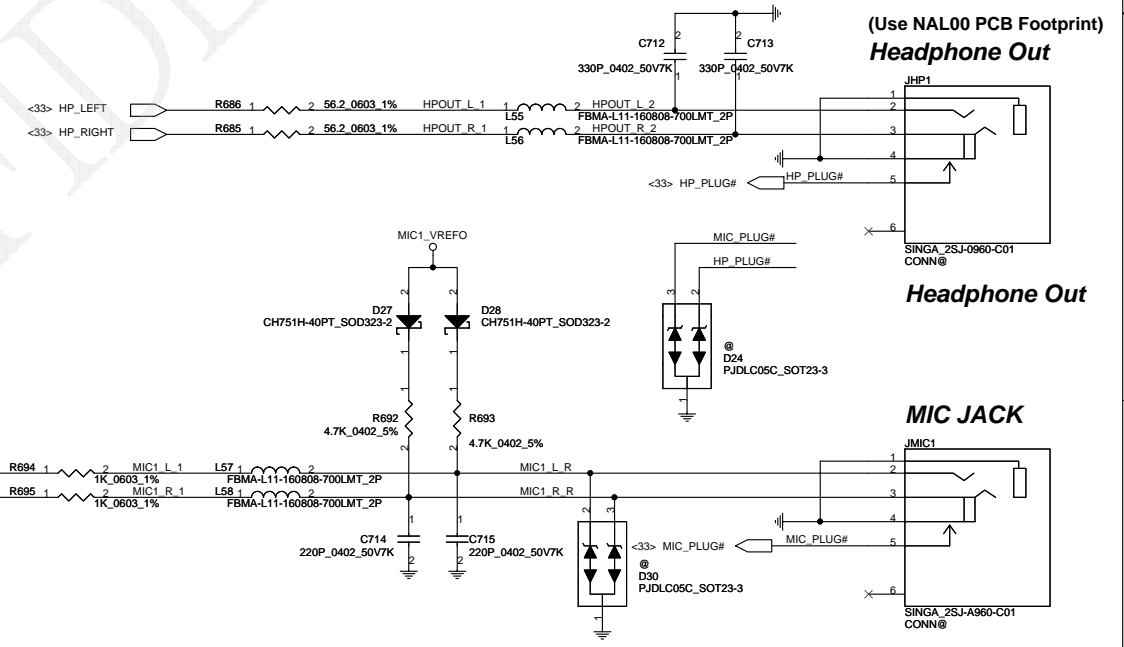
GAIN0	GAIN1	AV (inv)	Ri
0	0	6dB	90k
0	1	10dB	70k
1	0	15.6dB	45k
1	1	21.6dB	25k



Int. Speaker Conn.

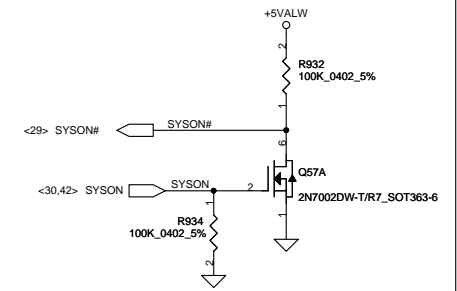
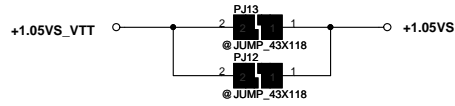
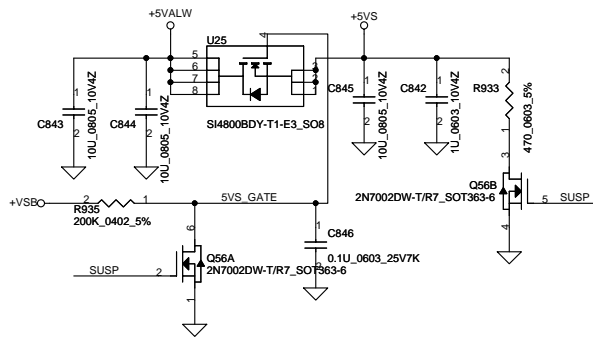


D25 / D26 Change to SCA00001100 for ESD 20090921

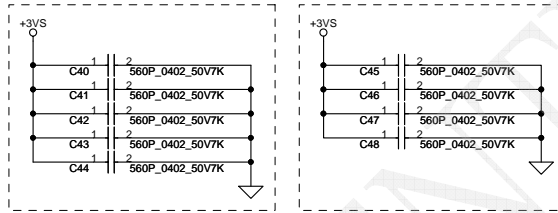
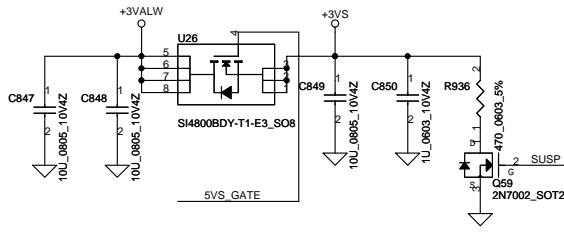


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+5VALW TO +5VS

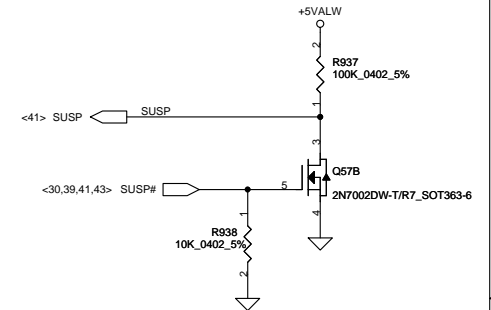


+3VALW TO +3VS

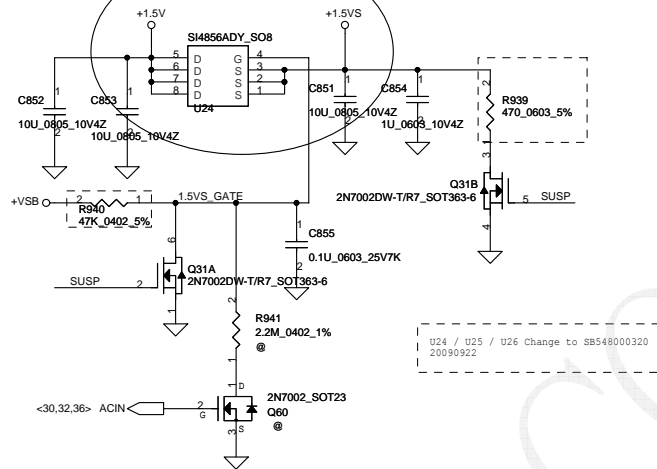


For EMI
200911092130

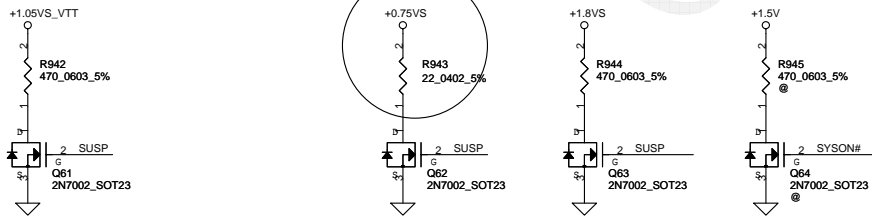
For LAM Common mode noise
200911102330



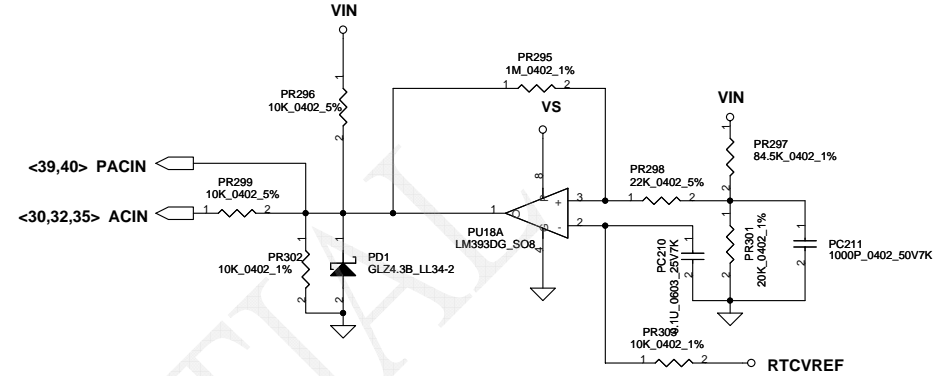
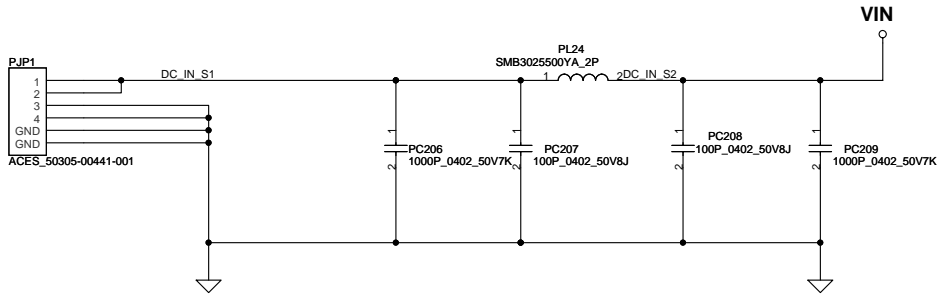
+1.5V to +1.5VS



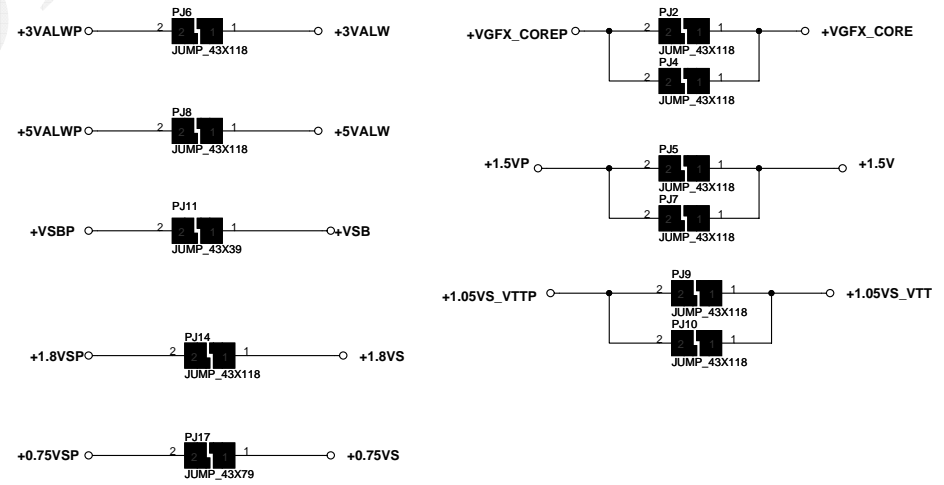
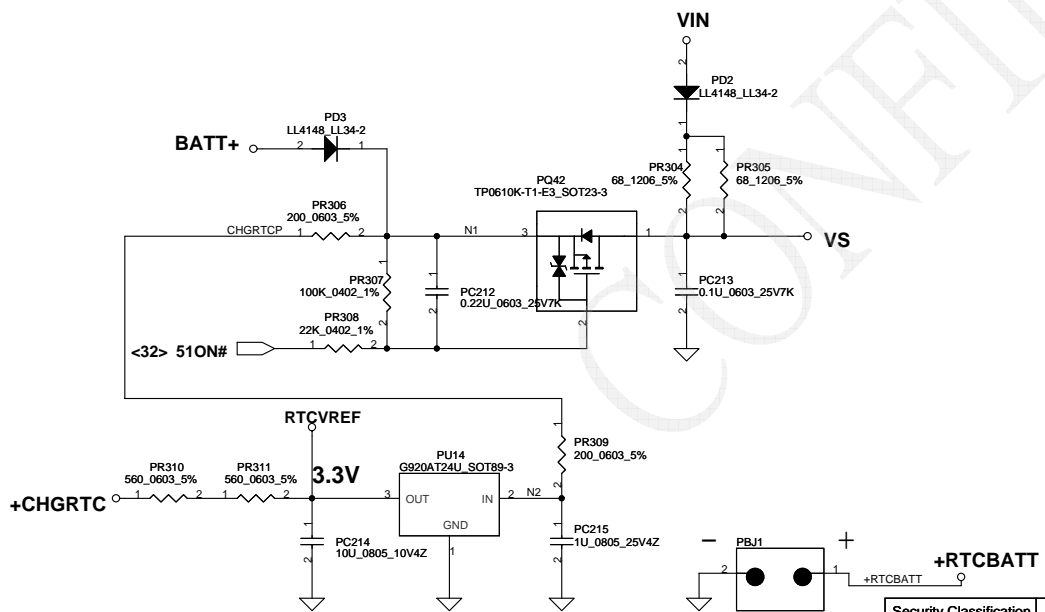
U24 / U25 / U26 Change to sb548000320
20090922



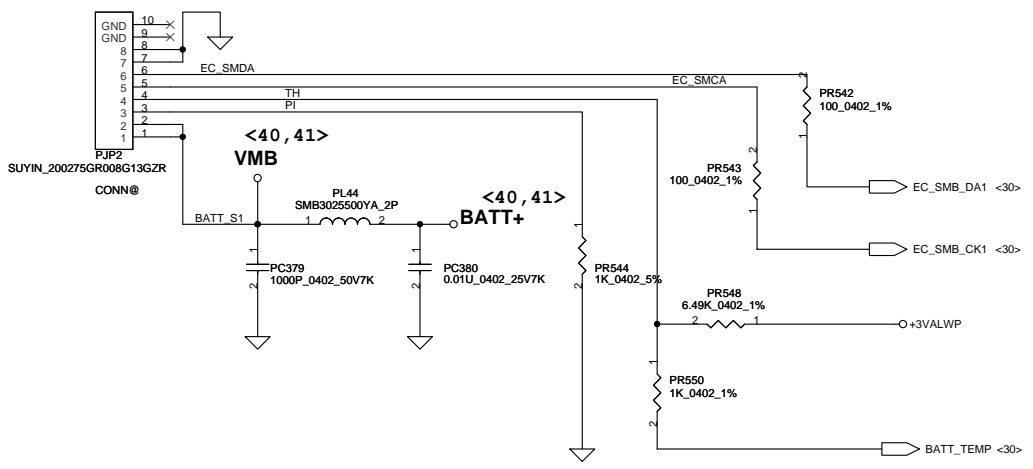
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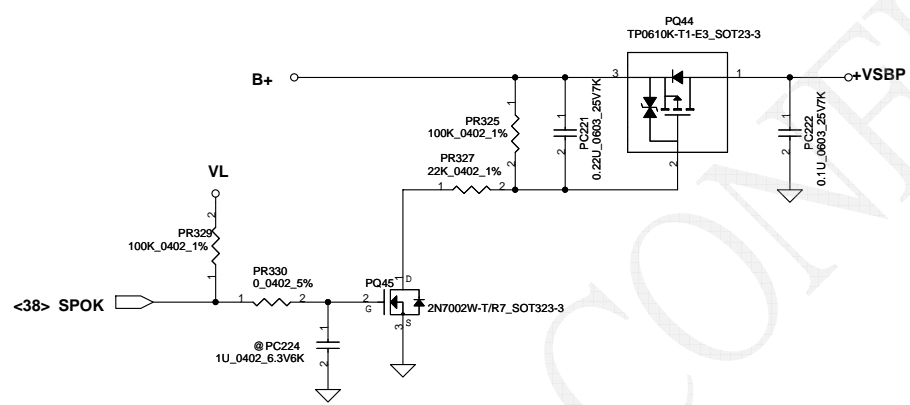
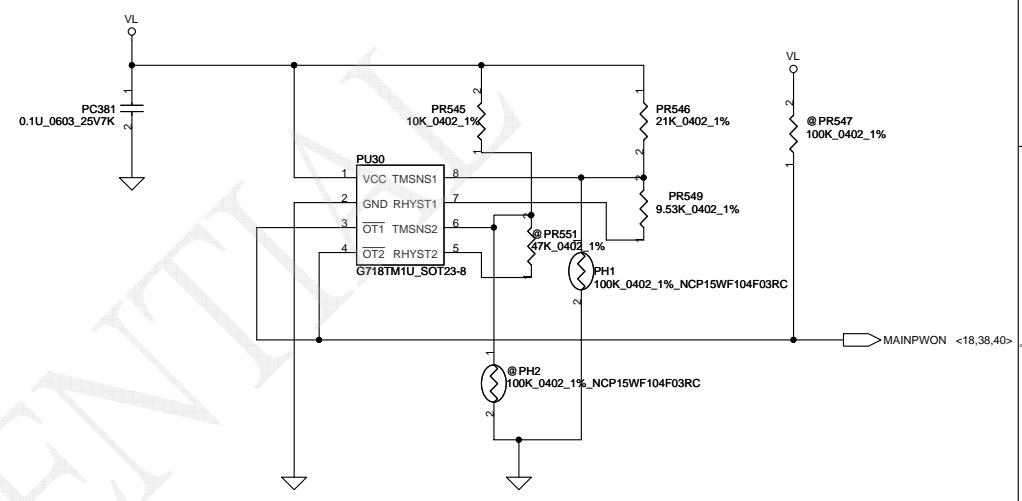
Vin Dectector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V



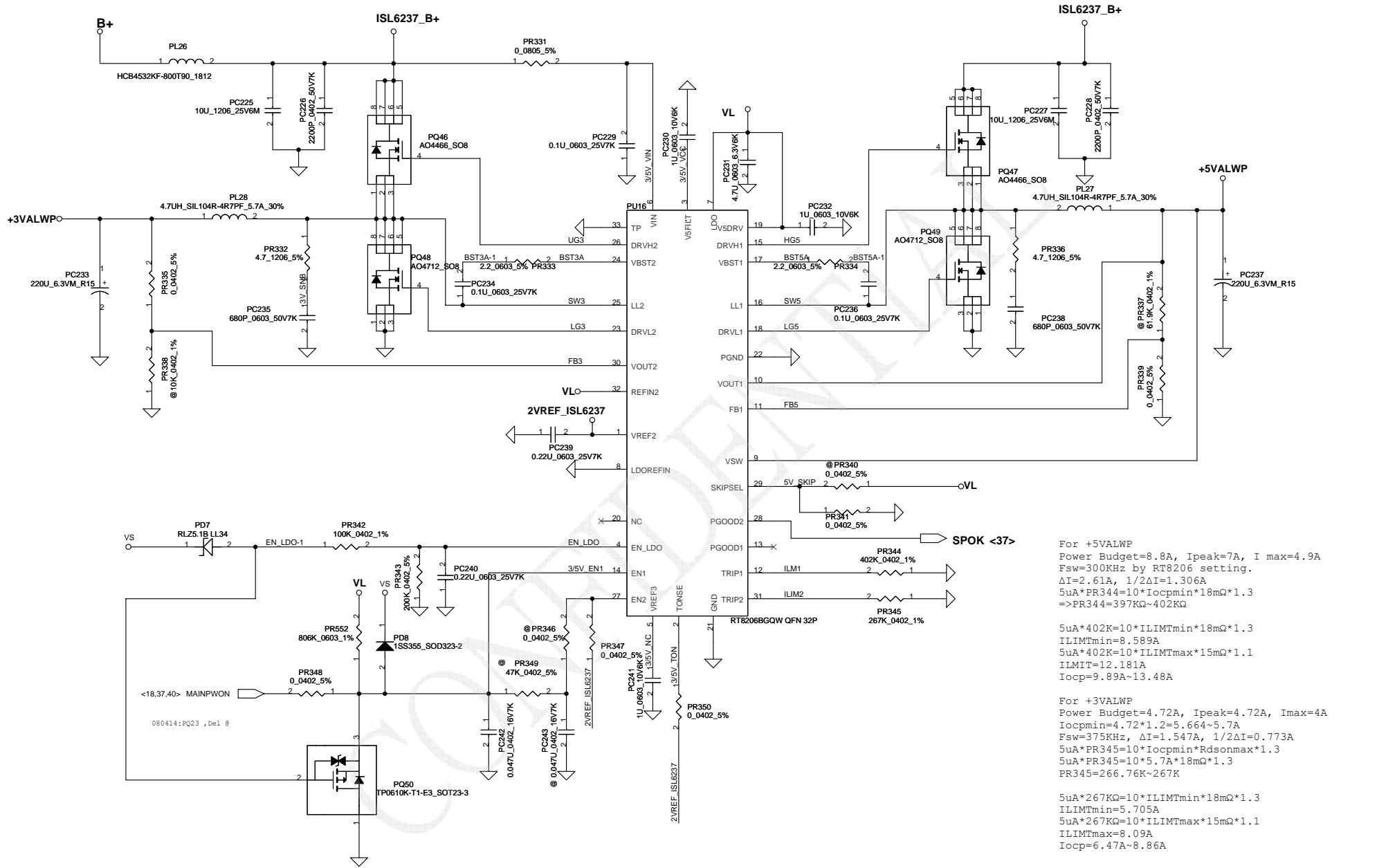
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PH1 under CPU bottom side :
 CPU thermal protection at 92 degree C
 Recovery at 56 degree C



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For +5VALWP
 Power Budget=8.8A, Ipeak=7A, I max=4.9A
 Fsw=300KHz by RT8206 setting.
 $\Delta I=2.61A$, $1/2\Delta I=1.306A$
 $5uA*PR344=10*Iocpmin*18m\Omega*1.3$
 $\Rightarrow PR344=397K\Omega-402K\Omega$

$5uA*402K=10*ILIMTmin*18m\Omega*1.3$
 $ILIMTmin=8.589A$
 $5uA*402K=10*ILIMTmax*15m\Omega*1.1$
 $ILIMIT=12.181A$
 $Iocp=9.89A-13.48A$

For +3VALWP
 Power Budget=4.72A, Ipeak=4.72A, I max=4A
 $Iocpmin=4.72*1.2=5.664-5.7A$
 $Fsw=375KHz$, $\Delta I=1.547A$, $1/2\Delta I=0.773A$
 $5uA*PR345=10*Iocpmin*Rdsonmax*1.3$
 $5uA*PR345=10*5.7A*18m\Omega*1.3$
 $PR345=266.76K-267K$

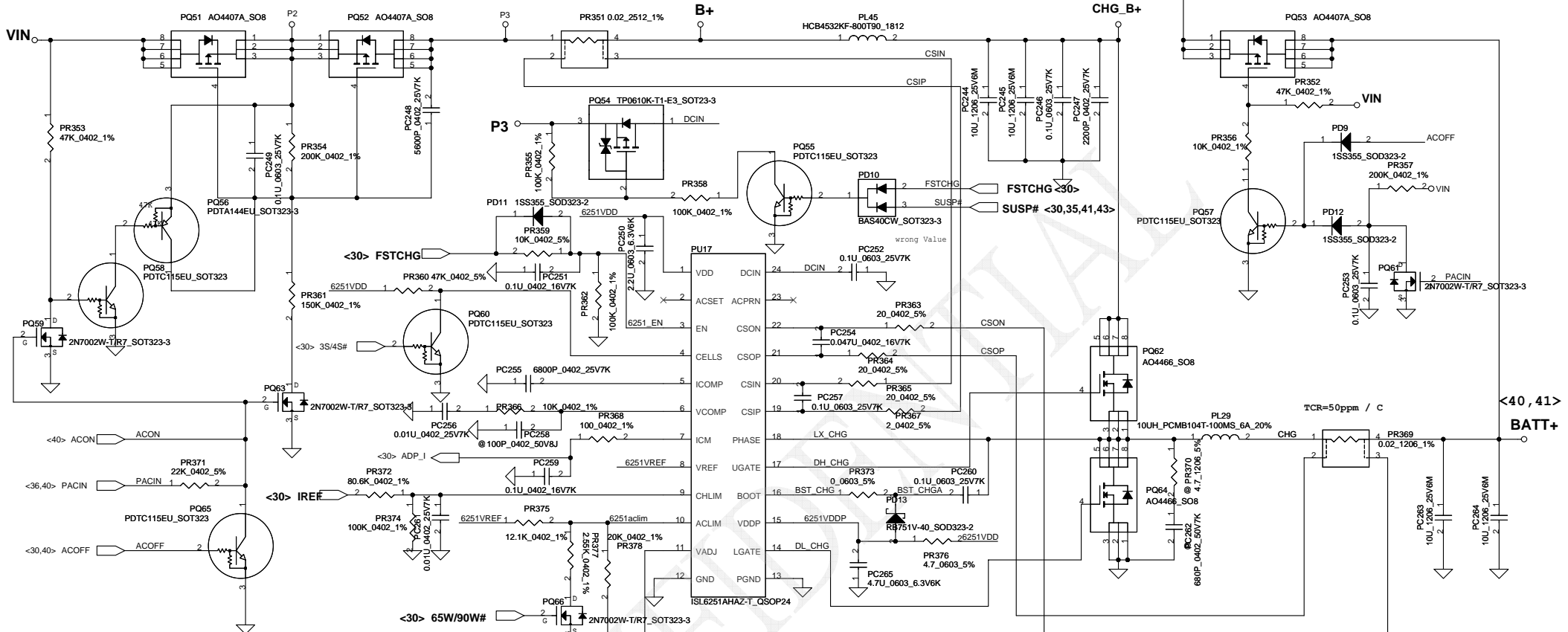
$5uA*267K\Omega=10*ILIMTmin*18m\Omega*1.3$
 $ILIMTmin=5.705A$
 $5uA*267K\Omega=10*ILIMTmax*15m\Omega*1.1$
 $ILIMTmax=8.09A$
 $Iocp=6.47A-8.86A$

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Iada=0~4.74A (90W/19V=4.736A)
 Iada=0~3.42A (90W/19V=3.421A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 4.07A
 CP = 85%*Iada ; CP = 2.91A



CP mode
 $I_{input} = (1/0.02) (0.05 * V_{ac1m} / 2.39 + 0.05)$
 where $V_{ac1m} = 1.502V$, $I_{input} = 4.07A$

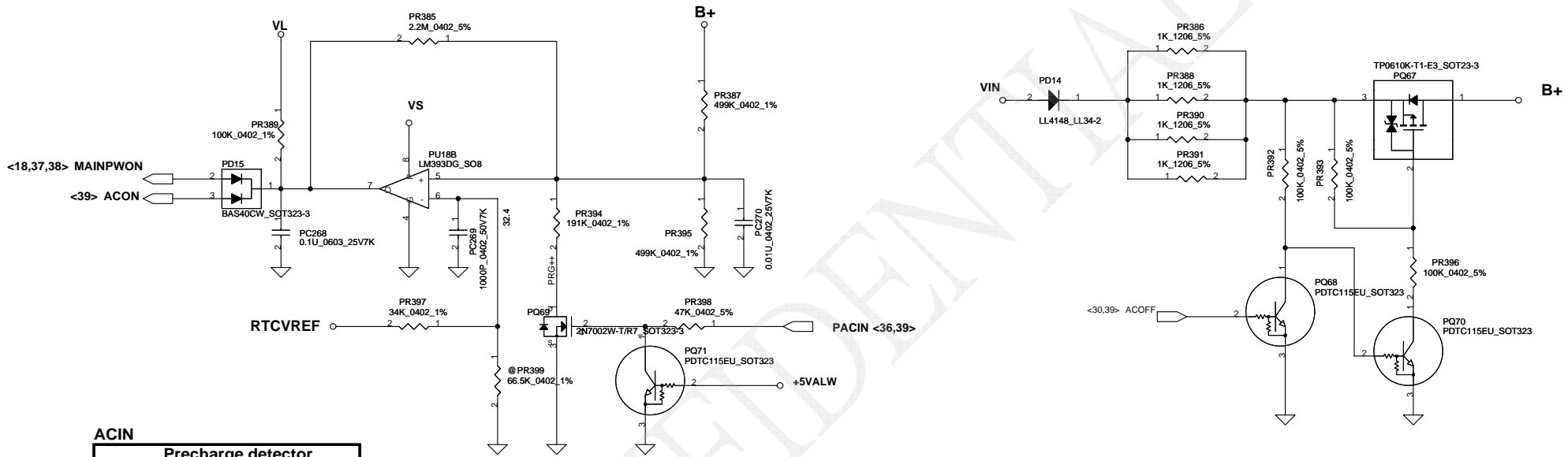
CC=0.6~4.48A
 $I_{REF} = 0.7224 * I_{charge}$
 $K_i = 0.7224$
 $I_{REF} = 0.43V \sim 3.24V$

K_i
 $V_{ch1m} = I_{ref} * (PR374 / (PR372 + PR374))$
 $= I_{ref} * (100K / (80.6K + 100K))$
 $= I_{ref} * 0.5537$
 $I_{charge} = (165mV / PR369) * (V_{ch1m} / 3.3V)$
 $= (165m / 20m) * (1/3.3V) * I_{ref} * 0.5537$
 $= 1.3842 * I_{ref}$
 $I_{ref} = 0.7224 * I_{charge} \Rightarrow K_i = 0.7224$

K_v
 $R_{internal} = 514K$ $R_{ec} = 3K$ $R_1 = PR379 = 15.4K$ $R_2 = PR381 = 31.6K$
 $R = 514K // 31.6K // (15.4K + 3K) = 11.372K$
 $r = 514K // 514K // 31.6K = 28.14K$
 $V_{cell0} = 1.75 * V_{adj} + 3.99V$
 $4.2V = 0.175 * V_{adj} + 3.99V \Rightarrow V_{adj} = 1.2V$
 $V_{adj} = V_{ref} * (R / (R + 514K)) + CALIBRATE * (r / (r + 514K))$
 $1.1483 = CALIBRATE * 0.6046 \Rightarrow CALIBRATE = 1.899$
 $1.899 = (4.2 - (V_{cell0} + A * 0.175)) * K_v = (4.2 - (4.2 * A * 0.175)) * K_v$
 $A * V_{ref} * (R / (R + 514K)) = 0.052$
 $K_v = 9.451$

LI-3S : 1.3.5V --- BATT-OVP=1.5012V
 $BATT-OVP = 0.1112 * V_{MB}$
 Per cell=3.5V

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V



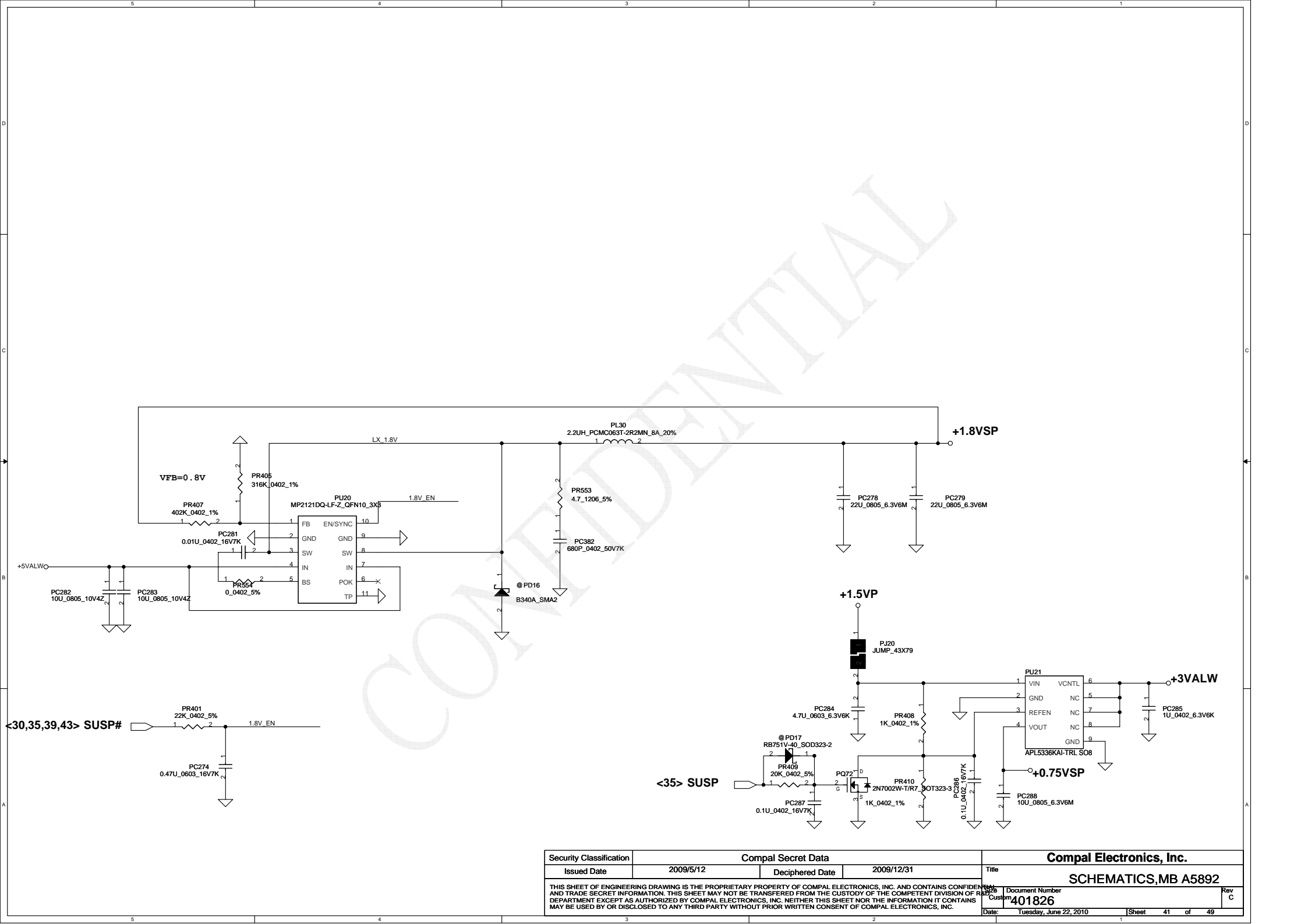
ACIN

Precharge detector		
Min.	typ.	Max
H-->L 14.589V	14.84V	15.243V
L-->H 15.562V	15.97V	16.388V

BATT ONLY

Precharge detector		
Min.	typ.	Max
H-->L 6.138V	6.214V	6.359V
L-->H 7.196V	7.349V	7.505V

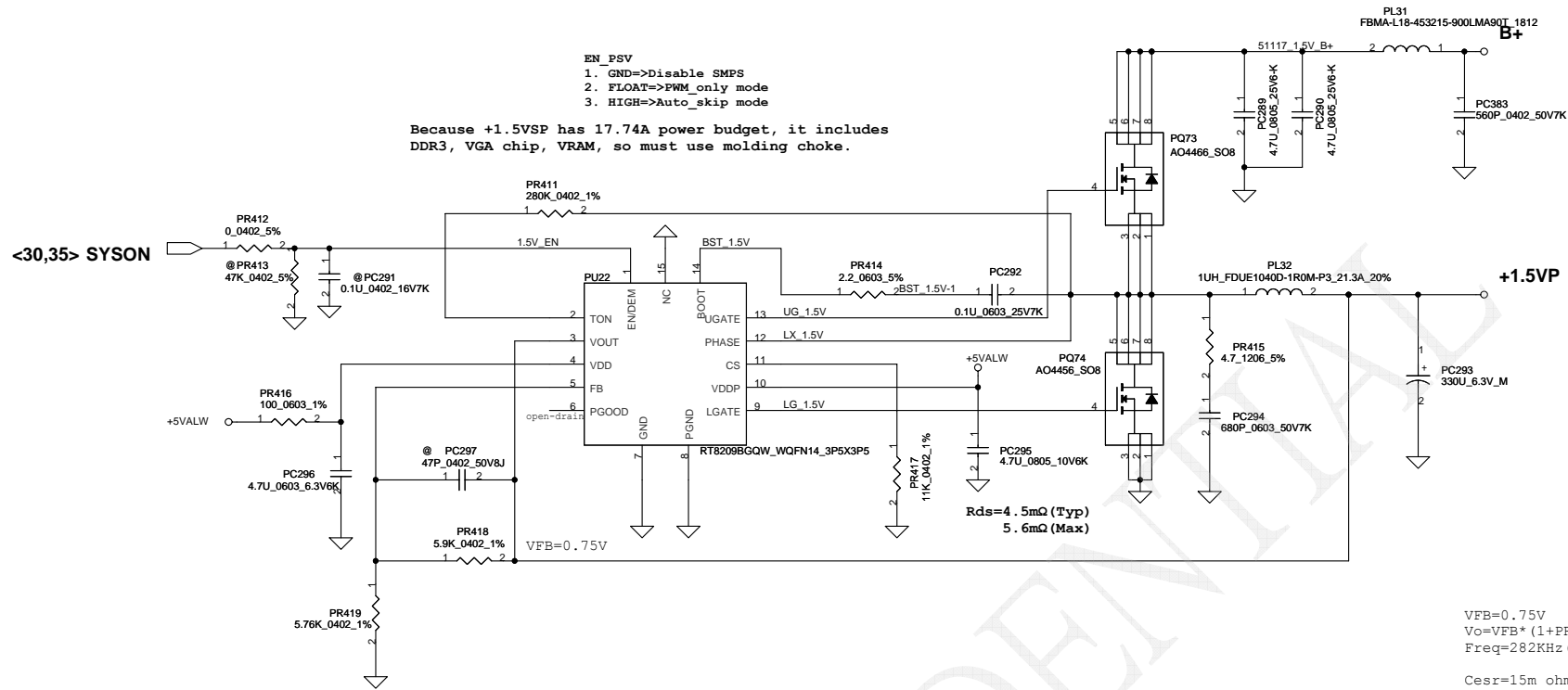
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- EN_PSV
 1. GND=>Disable SMPS
 2. FLOAT=>PWM_only mode
 3. HIGH=>Auto_skip mode

Because +1.5VSP has 17.74A power budget, it includes DDR3, VGA chip, VRAM, so must use molding choke.

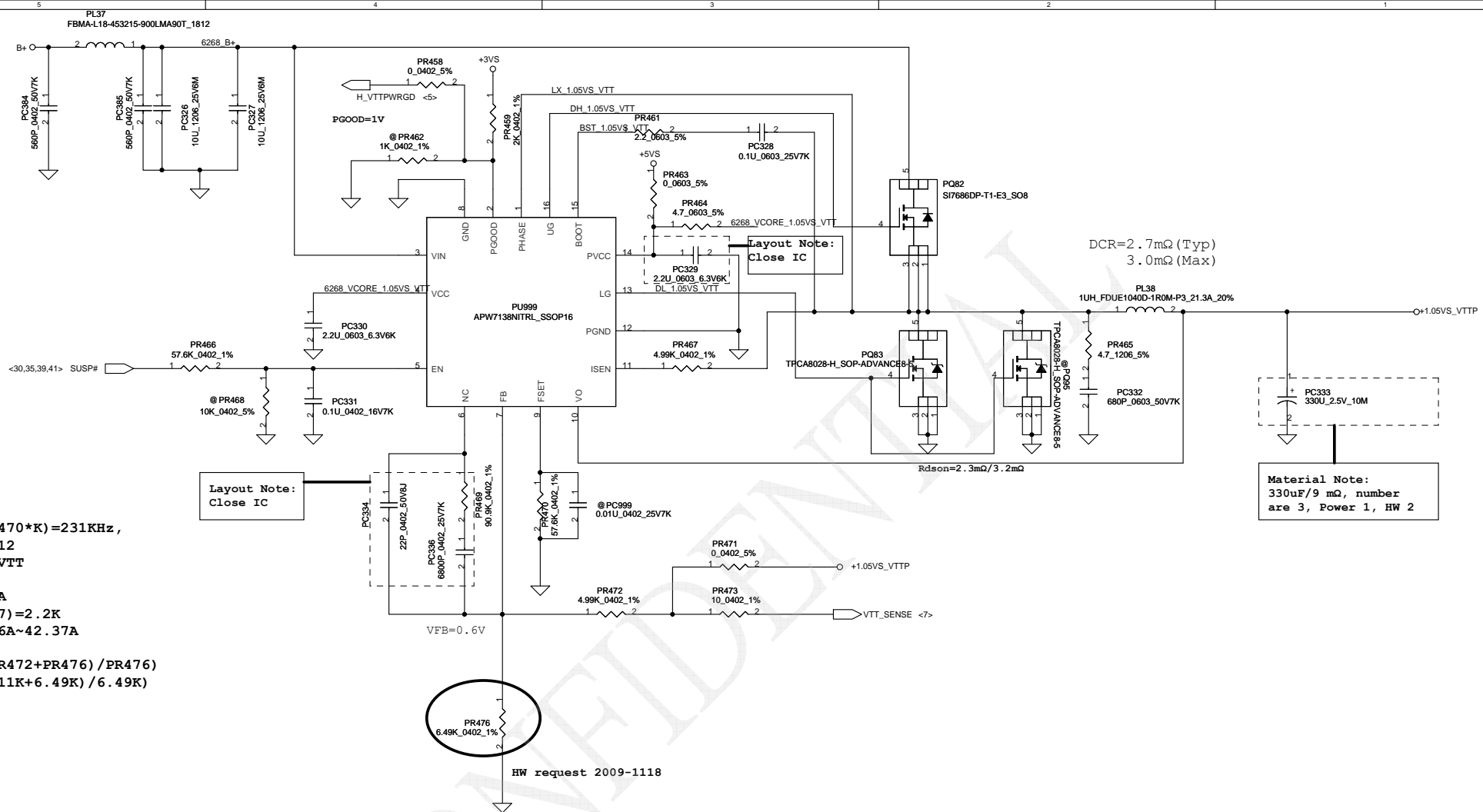


VFB=0.75V
 $V_o = VFB * (1 + PR418 / PR419) = 1.52V$
 Freq=282KHz (min) , 300KHz (typ)

Cesr=15m ohm
 Ipeak=15.82A
 Iocpmin=18.98A
 $\Delta I = ((19 - 1.5) * (1.5 / 19)) / (L * Freq) = 4.899A$
 $1/2 \Delta I = 2.449A$

Iocp=18.09A~29.13A

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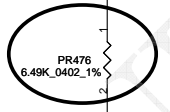
$f_{sw} = 1 / (PR470 * K) = 231 \text{ kHz}$
 $K = 75 * 10^{-12}$
 $+1.05V_{SP_VTT}$
 $I_{peak} = 25 \text{ A}$
 $I_{max} = 17.5 \text{ A}$
 $R_{sen} (PR467) = 2.2 \text{ K}$
 $I_{ocp} = 30.96 \text{ A} \sim 42.37 \text{ A}$

$V_o = V_r * ((PR472 + PR476) / PR476)$
 $= 0.6 * ((5.11 \text{ K} + 6.49 \text{ K}) / 6.49 \text{ K})$
 1.07 V

Layout Note:
Close IC

Layout Note:
Close IC

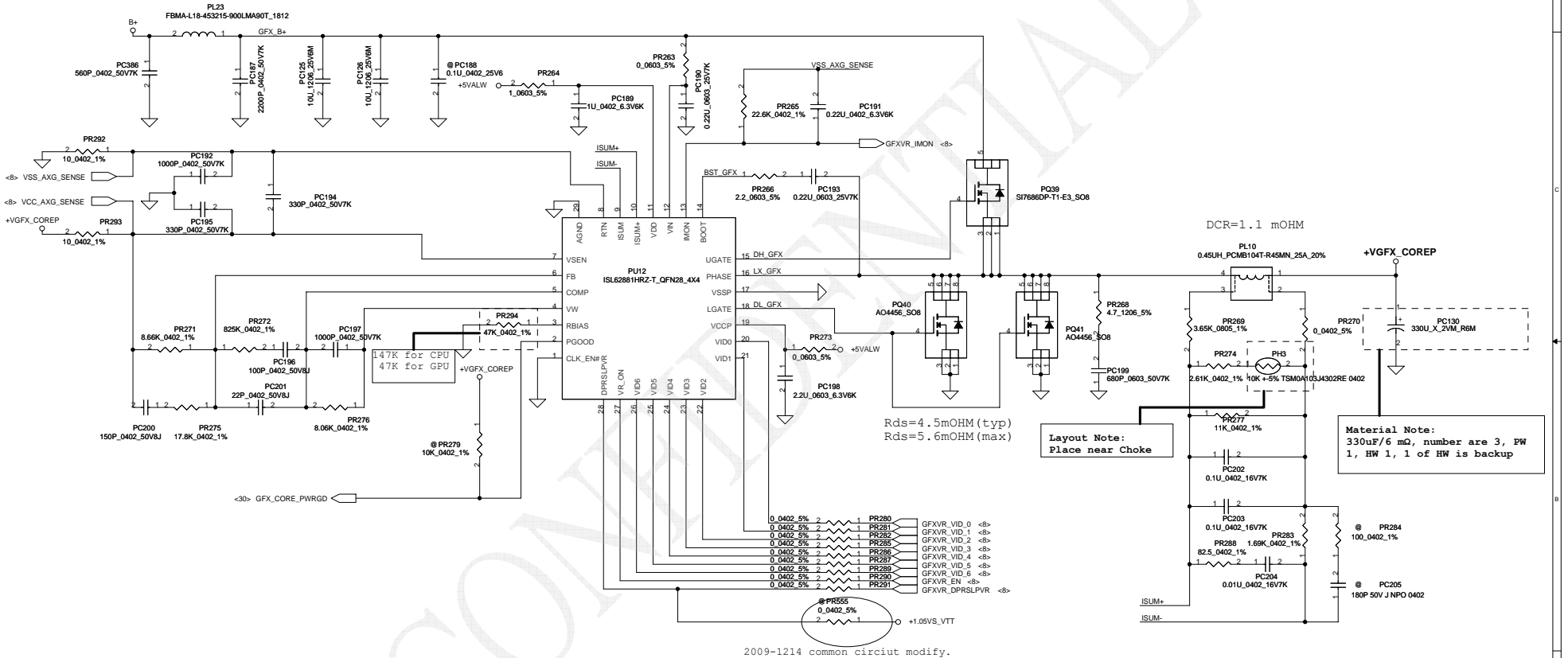
Material Note:
330uF/9 mΩ, number
are 3, Power 1, HW 2



HW request 2009-1118

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Intel Auburndale CPU(Integrate Graphics) Ipeak=22A Imax=15A
 OCP calculation : Assume DCR=1.1m ohm
 $G1=Rn/(Rn+Rsum)=0.617$
 where $Rn=PR277 // (PR274+PH3)=5.875k\ \text{ohm}$
 $Rsum=PR269=3.65k\ \text{ohm}$
 $LL=2 * Rdroop * G1 * DCR / Ri = 6.96m\ \text{V/A}$
 where $Rdroop=PR271=8.66k\ \text{ohm}$, $Ri=PR283=1.69k\ \text{ohm}$
 $Iocp=OCP\ \text{Threshold} * Rdroop / LL = 24.89A$



Layout Note:
Place near Choke

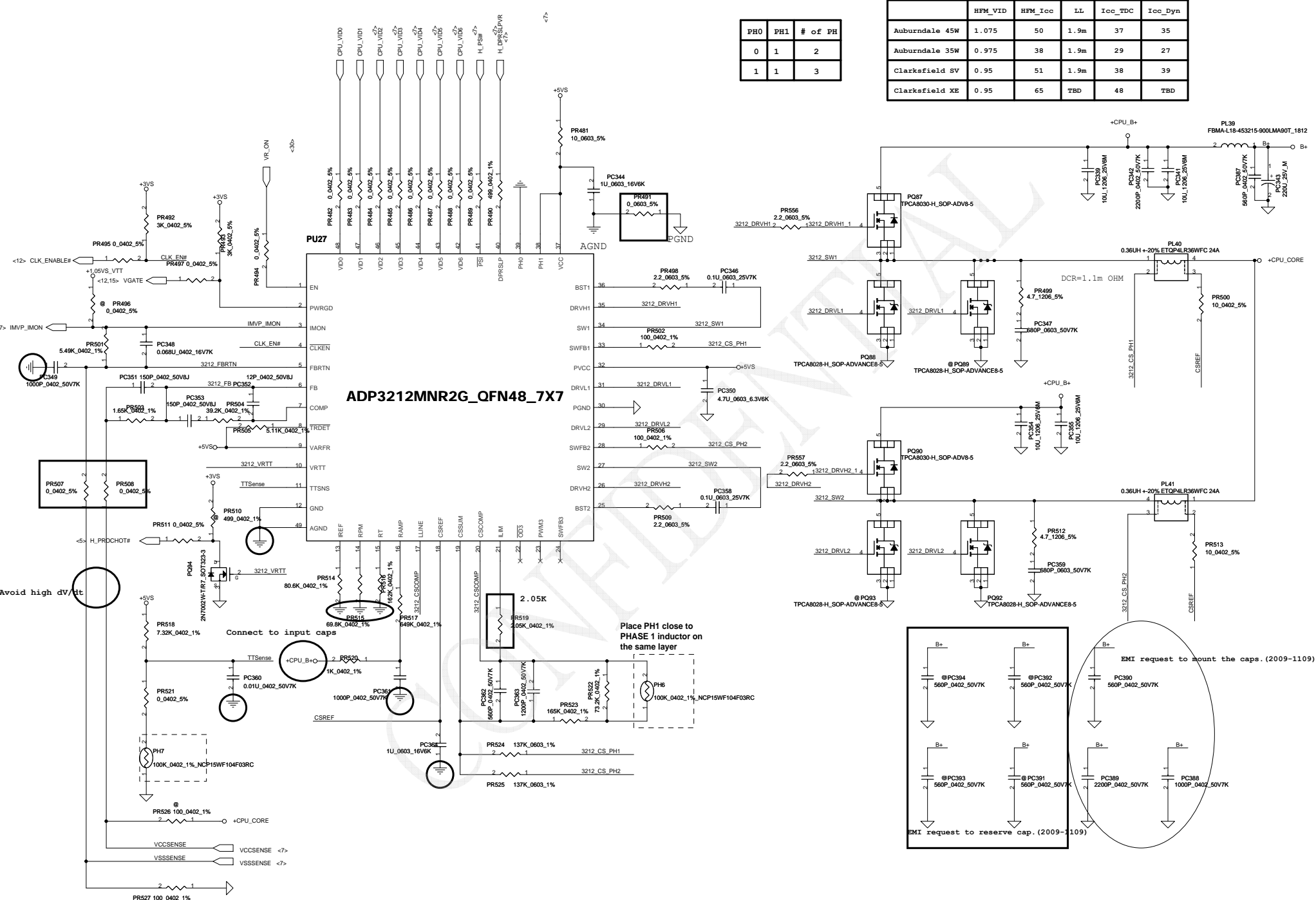
Material Note:
330uF/6 mΩ, number are 3, PW
1, HW 1, 1 of HW is backup

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PH0	PH1	# of PH
0	1	2
1	1	3

	HFM_VID	HFM_Icc	LL	Icc_TDC	Icc_Dyn
Auburndale 45W	1.075	50	1.9m	37	35
Auburndale 35W	0.975	38	1.9m	29	27
Clarksfield SV	0.95	51	1.9m	38	39
Clarksfield XE	0.95	65	TBD	48	TBD

ADP3212MNR2G_QFN48_7X7



Avoid high dV/dt

Connect to input caps

Place PH1 close to PHASE 1 inductor on the same layer

EMI request to mount the caps. (2009-1109)

EMI request to reserve cap. (2009-1109)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Arrandale CPU of UMA SKU only use 1 LS MOS	Arrandale CPU of UMA SKU only use 1 LS MOS	0.1	45	1 pop PQ87,PQ90, un-pop PQ86. 2 Delete PQ89, PQ93 SB00000GL00(S TR TPCA8028-H 1N SOP ADVANCE 4 PC A false)	2009-1019	to DVT
2	BOM unique.	In order to BOM unique for 1SS355, re-link PD8.	0.1	38	Change PD8 from SC1SS355003 to SC100001K00	2009-1019	to DVT
3	CIS link error.	CIS link error.	0.1	45	Change PR500 from SD028100A00(S RES I/16W 10 +-5% 0402) to SD028100A80(S RES 1/16W 10 +-5% 0402)	2009-1019	to DVT
4	BOM unique.	BOM unique.	0.1	39	Change PC265 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1019	to DVT
5	BOM unique.	BOM unique.	0.1	41	Change PC284 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1019	to DVT
6	BOM unique.	BOM unique.	0.1	45	Change PC350 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1019	to DVT
7	BOM unique.	BOM unique.	0.1	38	Change PC225/PC227 from SE153106K80(S CER CAP 10U 25V K X6S 1206) to SE142106M80 (S CER CAP 10U 25V M X5R 1206)	2009-1019	to DVT
8	BOM unique.	BOM unique.	0.1	45	Change PC339/PC341 from SE153106K80(S CER CAP 10U 25V K X6S 1206) to SE142106M80 (S CER CAP 10U 25V M X5R 1206)	2009-1019	to DVT
9	BOM unique.	BOM unique.	0.1	43	Change PQ83 from SB00000I900(S TR AON6704L 1N DFN) to SB00000GL00(S TR TPCA8028-H 1N SOP)	2009-1019	to DVT
10	VTT Power rail command design.	VTT Power rail command design.	0.1	43	Delete PQ95 SB00000GL00(S TR TPCA8028-H 1N SOP)-X63826B0L1 Delete PQ95 SB00000I900(S TR AON6704L 1N DFN)-OTHERS	2009-1019	to DVT
11	Charger, EMI request.	EMI request to add a bead to replace Jump to PASS EMI test.	0.2	39	Add FL45 SM010018210(S SUPPRE_TAI-TECH HCB4532KF-800T90 1812)	2009-1105	to DVT
12	+VSBP, EMI request.	EMI request to add PC221/PC222 to PASS EMI test	0.2	37	Add PC221 SE000005Z80 S CER CAP .22U 25V K X7R 0603 Add PC222 SE042104K80 S CER CAP .1U 25V K X7R 0603	2009-1105	to DVT
13	+1.8VSP, BOM error.	+1.8VSP EN delete wrong. Must add PR401 and PC274 for SUSP# enable.	0.2	41	Add PR401 SD028220280 S RES I/16W 22K 0402 5% Add PC274 SE026474K80 S CER CAP 0.47U 16V K X7R 0603	2009-1105	to DVT
14	+1.5VP, EMI request.	EMI request add snubber for +1.5VP to PASS EMIU test.	0.2	42	Add PR415 SD001470B80 S RES I/4W 4.7 +-5% 1206 Add PC294 SE025681K80 S CER CAP 680P 50V K X7R 0603	2009-1105	to DVT
15	+1.5VP, EMI request.	EMI request add a small cap to reduce high Freq noise. EMI request change boost R to 2.2 ohm.	0.2	42	Add PC383 SE074561K80 S CER CAP 560P 50V K X7R 0402 Change PR414 from SD013000080 to SD013220B80	2009-1105	to DVT
16	+1.05VS_VTTP EMI request.	EMI request add two small cap to reduce high Freq noise.	0.2	43	Add PC384 SE074561K80 S CER CAP 560P 50V K X7R 0402 Add PC385 SE074561K80 S CER CAP 560P 50V K X7R 0402	2009-1105	to DVT
17	+1.05VS_VTTP EMI request.	EMI request add snubber for +1.05VS_VTTP to PASS EMIU test.	0.2	43	Add PR465 SD001470B80 S RES I/4W 4.7 +-5% 1206 Add PC332 SE024681J80 S CER CAP 680P 50V J NPO 0603	2009-1105	to DVT
18	+1.05VS_VTTP EMI request.	EMI request change boost R to 2.2 ohm.	0.2	43	Change PR461 from SD013000080 to SD013220B80	2009-1105	to DVT
19	+1.05VS_VTTP, HW request.	HW request to increase +1.05VS_VTTP voltage.	0.2	43	Change PR472 from SD034499180 to SD034649180.	2009-1105	to DVT
20	+GFX_COREP, EMI request.	EMI request add a small cap to reduce high Freq noise.	0.2	44	Add PC386 SE074561K80 S CER CAP 560P 50V K X7R 0402	2009-1105	to DVT
21	+GFX_COREP, EMI request.	EMI request add snubber for +1.05VS_VTTP to PASS EMIU test.	0.2	44	Add PR268 SD001470B80 S RES I/4W 4.7 +-5% 1206 Add PC199 SE024681J80 S CER CAP 680P 50V J NPO 0603	2009-1105	to DVT
22	+GFX_COREP, EMI request.	EMI request change boost R to 2.2 ohm.	0.2	44	Change PR266 from SD013000080 to SD013220B80	2009-1105	to DVT

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
24	+CPU_COREP, EMI request.	EMI request add a small cap to reduce high Freq noise.	0.2	45	Add PC387 SE074561K80 S CER CAP 560P 50V K X7R 0402	2009-1105	to DVT
25	+CPU_COREP, EMI request.	EMI request change boost R to 2.2 ohm.	0.2	45	Change PR498/PR509 from SD013000080 to SD013220B80	2009-1105	to DVT
26	+CPU_COREP, EMI request.	EMI request add snubber for +CPU_COREP to PASS EMIU test.	0.2	45	Add PR499/PR512 SD001470B80 S RES 174W 4.7 +-5% I206 Add PC347/PC359 SE024681J80 S CER CAP 680P 50V J NPO 0603	2009-1105	to DVT
27	+CPU_COREP, Transient Loadline issue.	LA5892 transient and loadline must change some value to meet intel spec.	0.2	45	Change PL40/PL41 from SH000005680 to SH0000012036EM00.	2009-1105	to DVT
28	+CPU_COREP, Transient Loadline issue.	LA5892 transient and loadline must change some value to meet intel spec.	0.2	45	Change PR524/PR525 from SD013120380 to SD013137380.	2009-1105	to DVT
29	+CPU_COREP, Transient Loadline issue.	LA5892 transient and loadline must change some value to meet intel spec.	0.2	45	Change PC362 from SE074391K80 S CER CAP 390P 50V K X7R 0402 to SE074561K80 S CER CAP 560P 50V K X7R 0402	2009-1105	to DVT
30	+CPU_COREP, Transient Loadline issue.	LA5892 transient and loadline must change some value to meet intel spec.	0.2	45	Change PR501 from SD034536180 S RES 5.36K 0402 1% to SD034549180 S RES 1/16W 5.49K 0402 1%	2009-1105	to DVT
31	+CPU_COREP, EMI request.	+CPU_COREP, EMI request.	0.3	45	Add PC388 SE074102K80 S CER CAP 1000P 50V K X7R 0402	2009-1113	to DVT
32	+CPU_COREP, EMI request.	+CPU_COREP, EMI request.	0.3	45	Add PC389 SE074222K80 S CER CAP 2200P 50V K X7R 0402 Add PC390 SE074561K80 S CER CAP 560P 50V K X7R 0402	2009-1113	to DVT
33	+CPU_COREP, cost issue.	Beucase SF000000G80 will cost uo, change to SF22004M210.'	0.3	45	Change PC343 from SF000000G80 to SF22004M210.	2009-1113	to DVT
34	+CPU_COREP, IMON issue.	Because Intel update IMON RC time constant, update PC348 to 0.068u to meet spec.	0.3	45	Change PC348 from SE076103K80 S CER CAP .01U 16V K X7R 0402 to SE000003J80 S CER CAP 0.068U 16V K X7R 0402	2009-1113	to DVT
35	+3V/+5V cost issue.	Because Nippon cost up thier OS-CON cap, so we change Nippon cap to Sanyo cap by sourcer request.	0.4	38	Change PC233/PC237 from SF22001M300 S ELE CAP 220U 6.3V M F60 (6.3X5.7) PXC to SF22001M200 S ELE CAP 220U 6.3V M B C6 SVPC ESR15	2009-1118	to DVT
36	+1.05VS_VTTP issue.	HW request to increase +1.05VS_VTTP voltage.	0.4	43	Change PR472 from SD034649180 to SD034511180.	2009-1118	to DVT
37	+1.05VS_VTTP issue.	HW request to increase +1.05VS_VTTP voltage.	0.4	43	Chnage PR476 from SD034665180 to SD034649180.	2009-1118	to DVT
38	+0.75VSP power sequence issue.	HW request to adjust power sequence.	0.4	47	change PR409 from SD028000080 S RES 0 0402 5% to SD028200280 S RES 1/16W 20K 0402 5%.	2009-1118	to DVT
39	+1.05VS_VTTP issue.	+1.05VS_VTTP choke unique to +1.5VP.	0.4	43	Change PL38 from SH000008V80 S COIL 1UH +-20% PCMB103E-1R0MS 20A to SH000009U00 S COIL 1UH +-20% FDUE1040D-1R0M=P3 21.3A	2009-1118	to DVT
40	+1.05VS_VTTP 2nd source issue.	In order to phase in 2nd source, change ISL6268 to APW7138.	0.5	43	Change PU26 from SA00001HT80 S IC ISL6268CAZ-T SSOP 16P to PU999 SA000020600 S IC APW7138NITRL SSOP 16P	2009-1208	to PVT
41	+1.05VS_VTTP 2nd source issue.	APW7138 needn't pop PC335.	0.5	43	Delete PC335 SE075103K80 S CER CAP .01U 25V K X7R 0402 and change location to PC999.	2009-1208	to PVT
42	HDD LED flash issue.	HDD LED will flash when plug in adapter, because +3VS rise a little. HW request add PC224 to solve it.	0.5	37	Add PC224 SE000000K80 S CER CAP 1U 6.3V X5R 0402	2009-1208	to PVT
43	HDD LED flash issue.	If add PC224, must change PR330 from 0 to 1k to avoid SPOK pin fail. that is add a current limit R on SPOK pin.	0.5	37	Chnage PR330 from SD028000080 to SD028100180.	2009-1208	to PVT
44	BOM error.	+1.8VSP choke use wrong material. Unique MP2121 to other project.	0.5	41	Change FL30 from SH000006I80 S COIL 2.2UH +-20% PCMC063T -2R2MN 8A to SH000009Q00 S COIL 2.2UH 20% MSCDRI-74A-2R2M-E 6.5A Add PR554 SD028000080 0 0402 5%	2009-1208	to PVT
45	+1.05VS_VTTP issue.	HW request to adjust +1.05VS_VTTP Vout.	0.5	43	Change PR472 from SD034511180 to SD034499180.	2009-1208	to PVT
46	+VGF_X_COREP issue	ISL62881 common circiut update.	0.5	44	Delete PR291 SD028000080. Add PR555 SD028000080.	2009-1208	to PVT

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24	Sequense issue.	Modify sequense by HW request.	0.6	37	Chnage PR330 from SD028100180 S RES 1/16W 1K +-5% 0402 to SD028000080 S RES 1/16W 0 +-5% 0402.	2010-0112	to Pre-MP
25	Sequense issue.	Modify sequense by HW request.	0.6	37	Delete PC224 SE000000K80 S CER CAP 1U 6.3V K X5R 0402	2010-0112	to Pre-MP
26	EMI issue.	Because EMI has power BB on 250MHz, add HS gate R to solve.	0.6	45	Add PR556/PR557 SD013220B80 S RES 1/10W 2.2 +-5% 0603	2010-0112	to Pre-MP
27	BOM loss update in DVT.	BOM loss update in DVT, change 1.8V choke.	0.6	41	Change PL30 from SH000006180 S COIL 2.2UH +-20% PCMC063T-2R2MN 8A to SH000009Q00 S COIL 2.2UH 20% MSCDRI-74A-2R2M-E 6.5A	2010-0112	to Pre-MP
28	Common circiut update.	GFX_COREP common circiut update.	0.6	44	Add PR291 SD028000080 0 0402 5% Delete PR555 SD028000080 0 0402 5%	2010-0112	to Pre-MP
29	Changer choke issue.	Because Cyntec has quality issue and can't use in MFG, in order to prevent shortage issue, change to Maglayer.	0.6	39	Chnage PL29 from SH000005Z80 S COIL 10UH +-20% PCMB104T-100MS 6A to SH000009R00 S COIL 10UH +-20% MMD-10DZ-100M-X1 6A	2010-0112	to Pre-MP
30							
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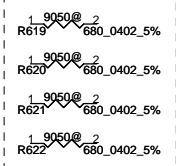
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Item	Phase	PAGE	DATE	Modifycatio list	Purpose
1			09 / 30	Q9 / Q15 / Q65 / Q14 / Q36 / Q19 / Q31 / Q56 / Q57 Change to SB00000AR10 Q4/Q5/Q6/Q7/Q13/Q24/Q25/Q59/Q61/Q62/Q63/Q20 Change to SB570020120	
2	DVT		11 / 03	Modify WWAN Mini catd PIN define. X1 / X2 Change to SJ132P7KW10. Add PCH_SUSCLK net for remove EC crystal. Remove C147. Add F2 for RF team. 11 / 05 Add C670 / C671 / C672 / C673 For INTEL Change C217 to 22U and add C221 22U for CRT issue. 11 / 09 Add P80DATA PD 100kohm(R51) for EC common design. 11 / 10 Add C40 / C41 / C42 / C43 / C44 for EMI. Add ACIN#(Q16) for ACIN LED(NEW60) Add C45 / C46 / C47 / C48 for LAN Common mode noise Remove net BT_LED#. 11 / 11 Add R14 for MINI1_LED Function. 11 / 16 Add D13/D14/D16/D23/D24/D25/D26/D30 for ESD Add R836/C60 R338/C555 for RF. L21 Change to SM010012010 L5 Change to SM01000AX00 Change R619/R621 to 680ohm Change R620/R622 to 3.9kohm Y1 Change to SJ100009R00 11 / 16 R841 Change to 8.2k ohm 11 / 17 Update Power SCH Change T1 to SP050006B00 11 / 18 Change PCH P/N to SA00003N7B0 Change R167 to 470 ohm. 11 / 19 Update Power SCH	
3	PVT		12 / 07 12 / 09	C259 / C279 / C692 / C693 Change to SE107475K80 0603 type Reserved R15 (net LOCAL_DIM) / R16 (net COLOR_ENG_EN) for LVDS function. Reserved R307 for +LCDVDD. EC Pin36 for WLAN_LED# (output), Pin 17 for MINI1_LED# (input) EC Pin91 for 3G_LED#(output) & Pin85 for WWAN_LED# (input) 12 / 10 Update Power SCH 12 / 11 Update Power SCH Add R96 PD 100K for LVDS Panel issue. Add C674 / C675 / C676 For EMI. Del SW3 Power on SW 12 / 14 Update Power SCH 12 / 16 UB change to SA00000U500 12 / 17 R619 / R621 change to 2.2K SD028220180 for LED Q13 / R477 Change to unpop R171 Change to pop,R172 change to unpop for Board ID. Add R777 / R778 For HDMI Issue.Only pop R778. R751 Change to 2.2K.	
4	PRE MP		01 / 06 01 / 11	ADD PU R951 / R953 UNPOP D23 for MIC noise issue. UNPOP R827 / R828, ADD L7 SM070001600 for USB. Update Power SCH Change Q9, Q65, Q15, Q14, Q36, Q19, Q31, Q56, Q57 to SB00000DH00 Change LED1 / LED3 to SC591NB5A30 Del L7, Add R827 / R828. Del D26 / D25 Update Power SCH 01 / 21 03 / 01 Modify Power SCH NAME	
	MP		05 / 11 06 / 09	Reserve D13 / D24 / D30 @ (ESD) Add NEW7X0@ / PEW51@ BOM Structure fo ID	

For NEW50 / NEW90 LED

For PEW51 project ID



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