ZZZ

PCB

Part Number = DAZ0FQ00100

ZZZ

64M512@

X76244BOL01

Part Number = X76244BOL01

ZZZ

64M1G@

X76244BOL03

Part Number = X76244BOL03

ZZZ

128M1G@

X76244BOL05

Part Number = X76244BOL05

ZZZ

128M2G@

X76244BOL06

Part Number = X76244BOL06

Compal Confidential

PEW76 Schematics Document

AMD Danube

Champlain Processor with RS880M/SB820/Madison VGA

2010-06-07

LA5911P REV: 1.0

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Model Name : NEW75/85/95

Danube

VRAM 1GB 64M16 x 8 page 19, 20

DDR3

AMD S1G4 Processor
uPGA-638 Package
Champlain page 4,5,6,7

Memory BUS(DDR3)
Dual Channel
1.5V DDRIII 800~1333MHz

204pin DDRIII-SO-DIMM X2
BANK 0, 1, 2, 3 page 8,9

ATI M97
Madisan/Park
uFCBGA-962
Page 14,15,16,17,18,21,22

PCI-Express x 16
Gen2

Hyper Transport Link
16 x 16

ATI RS880M
uFCBGA-528
page 10,11,12,13

Thermal Sensor
ADM1032
page 6

Clock Generator
ICS9LPRS488
page 23

LVDS page 24

CRT page 26

HDMI Conn. page 25

A link Express2
Gen1

ATI SB820M
uFCBGA-605
page 27,28,29,30,31

page 36,37	page 27	page 37	page 36	page 36	page 36
USB conn X 3	CMOS Camera	Bluetooth Conn <Option>	Mini card (WL)X1	3G/GPS WWAN <Option>	Card Reader
USB port 0,1,2	USB port 5	USB port 12	USB port 8	USB port 9	USB port 6

3.3V 48MHz
USB
3.3V 24.576MHz/48Mhz
HD Audio

S-ATA Gen2

MINI Card 1
WLAN
page 36
GPP1

LAN(GbE)
Broadcom
BCM57780
page 34
GPP0

RJ45 page 35

LPC BUS

SATA HDD Conn. page 32
port 0

CDROM Conn. page 32
port 1

HDA Codec
ALC272X
page 42

Audio AMP page 43

Phone Jack x2 page 43

ENE KB926
page 38

Touch Pad page 39

Int.KBD page 39

EC I/O Buffer page 38

BIOS page 39

LED page 40

Fan Control page 44

RTC CKT. page 26

Extend Card/B
1. USB X2
2. Cardreader JM385

LID SW / MEDIA/B page 39

Power On/Off CKT. page 41

DC/DC Interface CKT. page 45

Power Circuit
page 46,47,48,49,50,51
52,53,54

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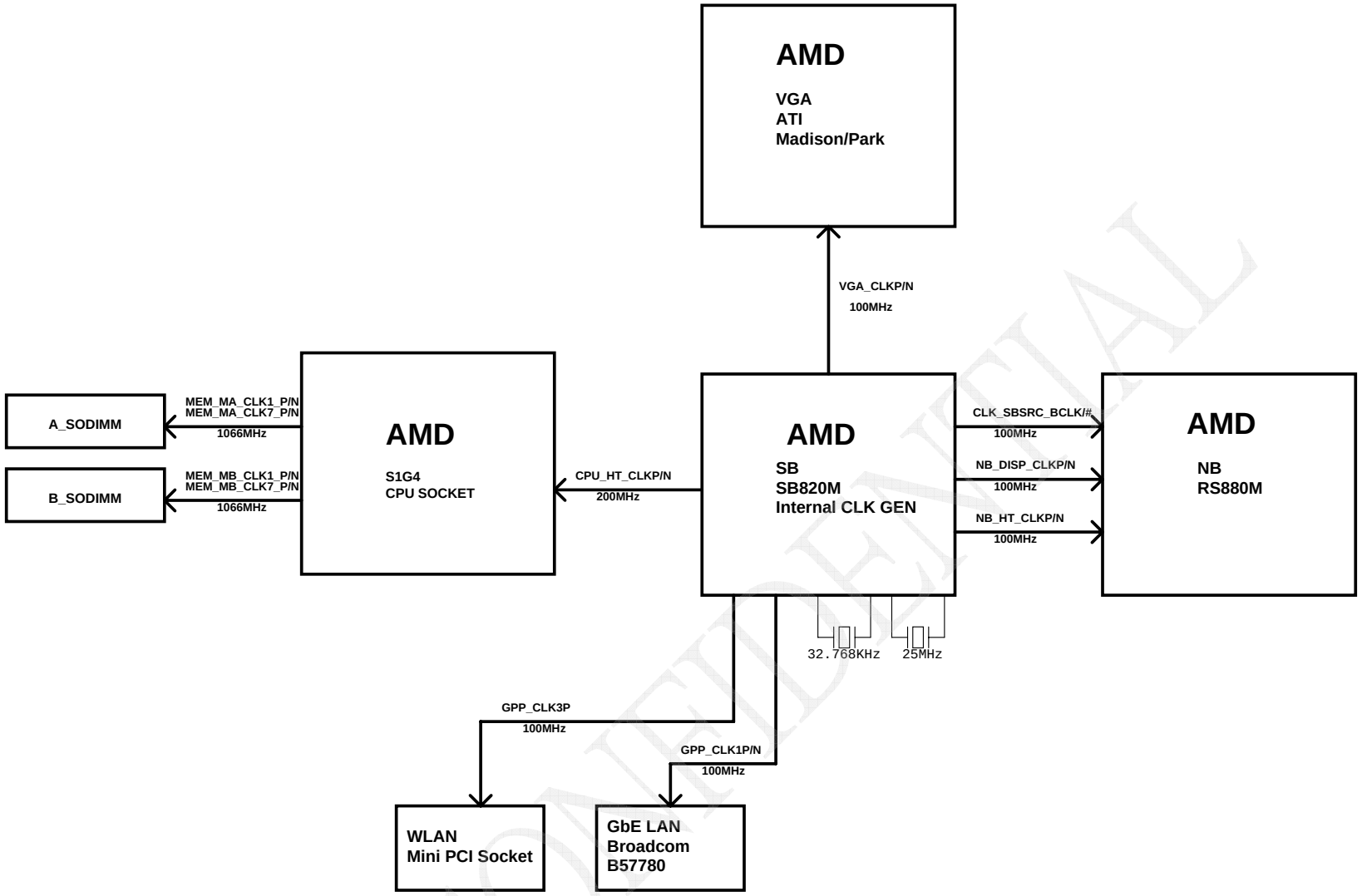

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE_0	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+CPU_CORE_1	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die Northbridge of CPU(0.8-1.1V)	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.1VS	1.1V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+1.2V_HT	1.2V switched power rail	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+1.5VS	1.5V power rail for PCIE Card	ON	OFF	OFF
+1.8V	1.8V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001 011X b	16H

EC SM Bus2 address

Device	Address	HEX
ADI ADM1032 (CPU)	1001 100X b	98H
GMT G781-1 (GPU)	1001 101X b	9AH
SB-Temp Sensor		98H

SB820 SM Bus 0 address

Device	Address	HEX
Clock Generator (SILEGO SLG8SP626)	1101 001Xb	D2
DDR DIMM1	1001 000Xb	90
DDR DIMM2	1001 010Xb	94
Mini card		

SB820 SM Bus 1 address

Device	Address

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	
1	*No USB Patch*
2	*Capilano w/ USB patch*
3	
4	
5	
6	
7	*Add USB patch*

BTO Option Table

BTO Item	BOM Structure

Project ID Table

--For SSID define
--For TSI thermal math

Board ID	PCB Revision
0	*NEW75/85/95*
1	*PEW76/86/96*
2	*PEW56*
3	
4	
5	
6	
7	

BOM Config

EXT CLKGEN

PowerXpress SKU(Madison): 3G@/BT@/UMA@/ VGA@/SG@/EXT@/EXTPW@/VB@/MAD@
PowerXpress SKU(Park): 3G@/BT@/UMA@/ VGA@/SG@/EXT@/EXTPW@/VB@/PARK@
DIS ONLY:(Park) 3G@/BT@/DISO@/ VGA@/EXT@/EXTPW@/PARK@
UMA only SKU: 3G@/BT@/UMA@/ UMAO@/EXT@/VB@

INT CLKGEN

PowerXpress SKU(Madison):3G@/BT@/UMA@/VGA@/SG@/INT@/VB@/MAD@
PowerXpress SKU(Park): 3G@/BT@/UMA@/VGA@/SG@/INT@/VB@/PARK@
DIS ONLY(PARK): 3G@/BT@/DISO@/VGA@/INT@/PARK@
UMA only SKU: 3G@/BT@/UMA@/UMAO@/INT@/VB@

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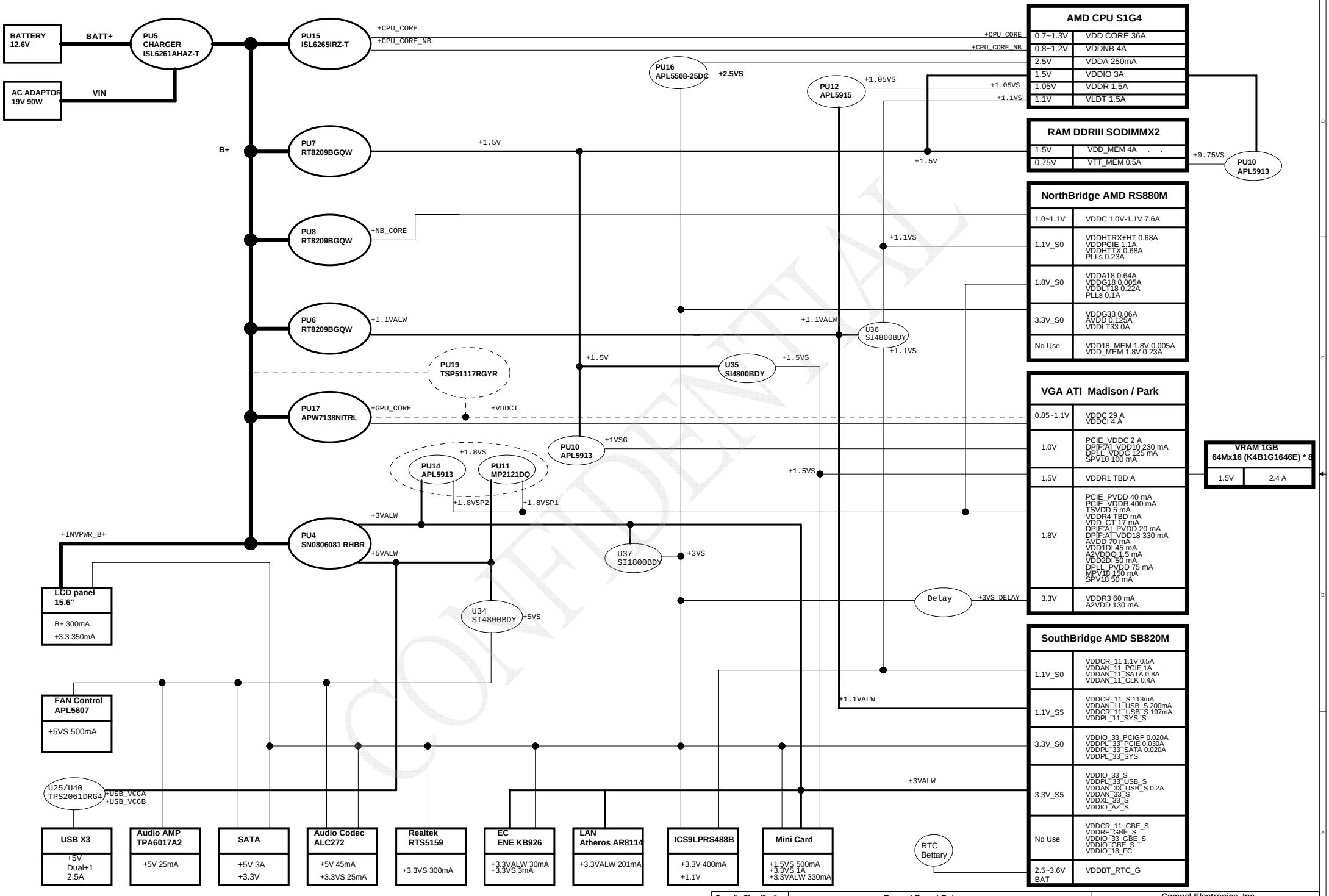
BATTERY 12.6V
BATT+
PU5 CHARGER ISL6261AHAZ-T
AC ADAPTOR 19V 90W
VIN
B+
PU15 ISL6265IRZ-T
+CPU_CORE
+CPU_CORE_NB
PU16 APL5508-25DC
+2.5VS
PU12 APL5915
+1.05VS
+1.1VS
PU7 RT8209BGQW
+1.5V
PU8 RT8209BGQW
+NB_CORE
PU6 RT8209BGQW
+1.1VALW
PU19 TSP51117RGYR
U36 SI4800BDY
U35 SI4800BDY
PU17 APW7138NITRL
+GPU_CORE
+VDDCI
PU10 APL5913
+1VSG
PU14 APL5913
PU11 MP2121DQ
+1.8VS
+1.8VSP2
+1.8VSP1
+3VALW
+INVPWR_B+
PU4 SN0806081 RHBR
+5VALW
U37 SI1800BDY
+3VS
U34 SI4800BDY
+5VS
Delay
+3VS_DELAY
LCD panel 15.6"
B+ 300mA
+3.3 350mA
FAN Control APL5607
+5VS 500mA
U25/U40 TPS2061DRG4
+USB_VCCA
+USB_VCCB
USB X3
+5V
Dual+1
2.5A
Audio AMP TPA6017A2
+5V 25mA
SATA
+5V 3A
+3.3V
Audio Codec ALC272
+5V 45mA
+3.3VS 25mA
Realtek RTS5159
+3.3VS 300mA
EC ENE KB926
+3.3VALW 30mA
+3.3VS 3mA
LAN Atheros AR8114
+3.3VALW 201mA
ICS9LPRS488B
+3.3V 400mA
+1.1V
Mini Card
+1.5VS 500mA
+3.3VS 1A
+3.3VALW 330mA
RTC Bettary
AMD CPU S1G4
0.7~1.3V VDD CORE 36A
0.8~1.2V VDDNB 4A
2.5V VDDA 250mA
1.5V VDDIO 3A
1.05V VDDR 1.5A
1.1V VLDT 1.5A
RAM DDRIII SODIMMX2
1.5V VDD_MEM 4A
0.75V VTT_MEM 0.5A
+0.75VS
PU10 APL5913
NorthBridge AMD RS880M
1.0~1.1V VDDC 1.0V-1.1V 7.6A
1.1V_S0 VDDHTRX+HT 0.68A VDDPCIE 1.1A VDDHTTX 0.68A PLLs 0.23A
1.8V_S0 VDDA18 0.64A VDDG18 0.005A VDDLT18 0.22A PLLs 0.1A
3.3V_S0 VDDG33 0.06A AVDD 0.125A VDDLT33 0A
No Use VDD18_MEM 1.8V 0.005A VDD_MEM 1.8V 0.23A
VGA ATI Madison / Park
0.85~1.1V VDDC 29 A VDDCI 4 A
1.0V PCIE_VDDC 2 A DPF:A]_VDD10 230 mA DPLL_VDDC 125 mA SPV10 100 mA
1.5V VDDR1 TBD A
1.8V PCIE_PVDD 40 mA PCIE_VDDR 400 mA TSVDD 5 mA VDDR4 TBD mA VDD_CT 17 mA DPF:A]_PVDD 20 mA DPF:A]_VDD18 330 mA AVDD 70 mA VDD1DI 45 mA A2VDDQ 1.5 mA VDD2DI 50 mA DPLL_PVDD 75 mA MPV18 150 mA SPV18 50 mA
3.3V VDDR3 60 mA A2VDD 130 mA
VRAM 1GB 64Mx16 (K4B1G1646E) * 8
1.5V 2.4 A
SouthBridge AMD SB820M
1.1V_S0 VDDCR_11 1.1V 0.5A VDDAN_11_PCIE 1A VDDAN_11_SATA 0.8A VDDAN_11_CLK 0.4A
1.1V_S5 VDDCR_11_S 113mA VDDAN_11_USB_S 200mA VDDCR_11_USB_S 197mA VDDPL_11_SYS_S
3.3V_S0 VDDIO_33_PCIGP 0.020A VDDPL_33_PCIE 0.030A VDDPL_33_SATA 0.020A VDDPL_33_SYS
3.3V_S5 VDDIO_33_S VDDPL_33_USB_S VDDAN_33_USB_S 0.2A VDDAN_33_S VDDXL_33_S VDDIO_AZ_S
No Use VDDCR_11_GBE_S VDDRF_GBE_S VDDIO_33_GBE_S VDDIO_GBE_S VDDIO_18_FC
2.5~3.6V BAT VDDBT_RTC_G
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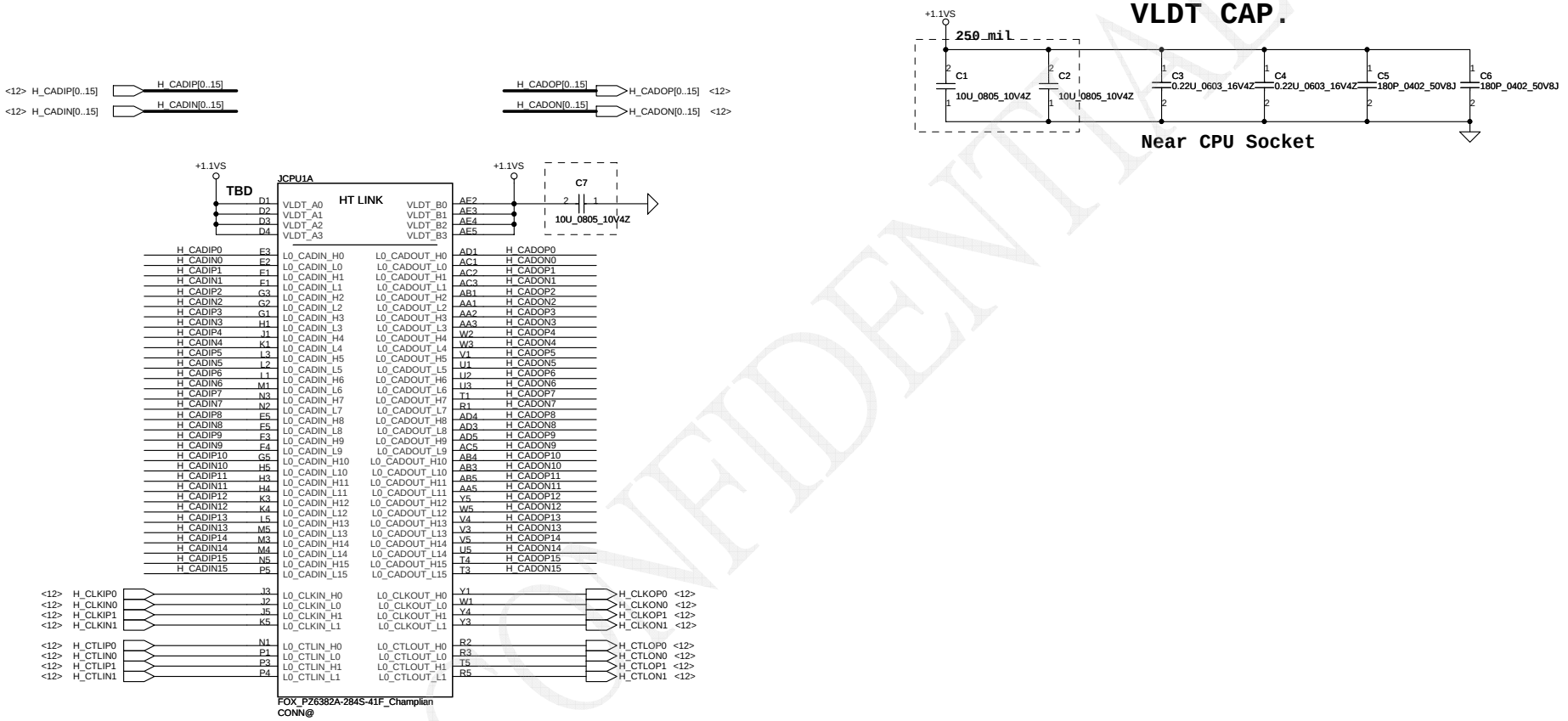

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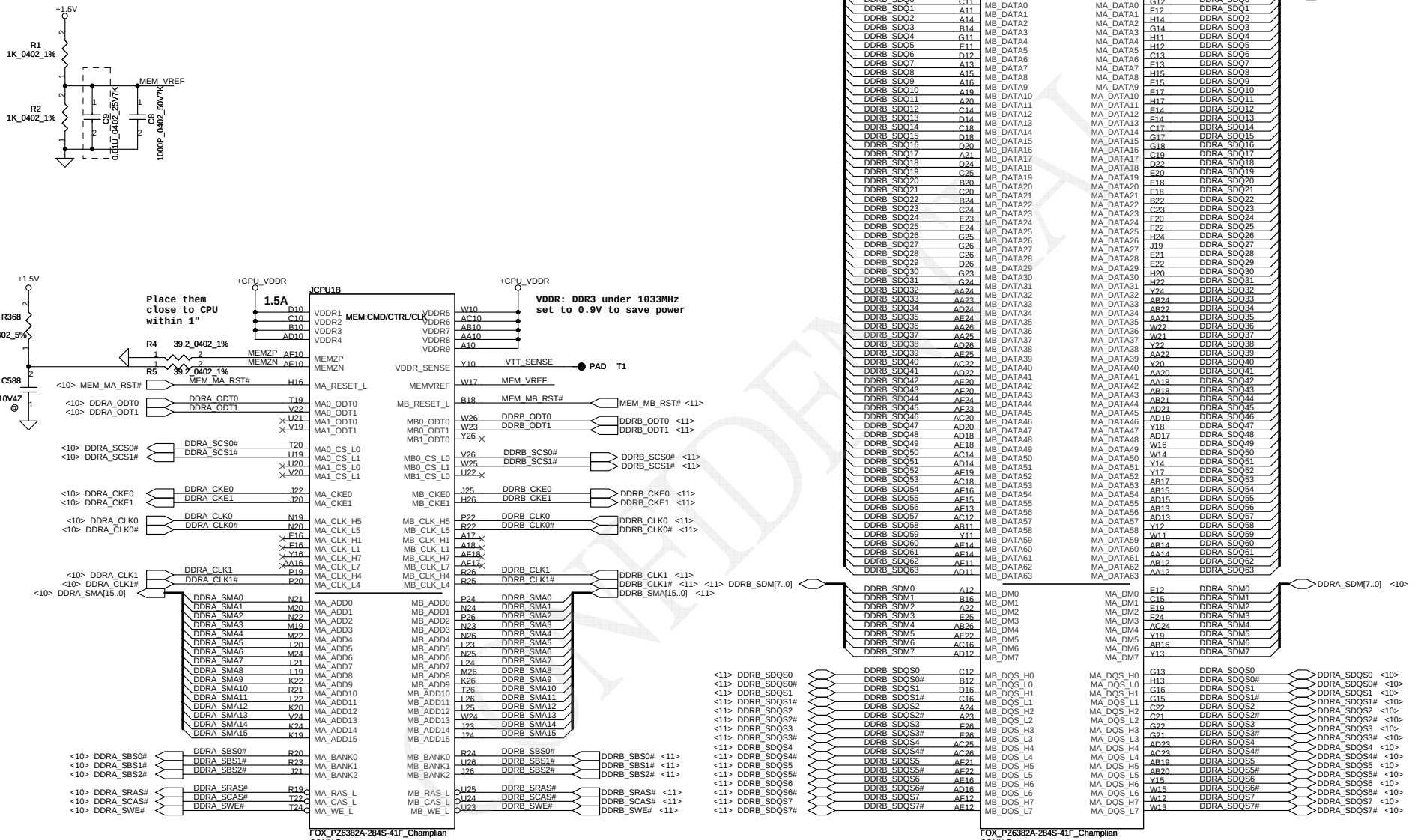
Processor DDR3 Memory Interface



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Champlain: C1E
C1E: LDT_REQ# no connect
CLMC: LDT_REQ# connect to NB

LDT_RES# / MEMHOT#
no support in S1g4

VDDA=0.25A

JCPU1D

FOX_PZ6382A-284S-41F_Champlian
CONN@

PROCHOT:
Input: For HTC Function
Output: Over Temperature Condition

For SCAN connect use

Address 1001 100X b

CPU internal thermal sensor

FDV301N, the Vgs is:
min = 0.65V
Typ = 0.85V
Max = 1.5V

2.09V for Gate

CONN@ SAMTEC_ASP-68200-07

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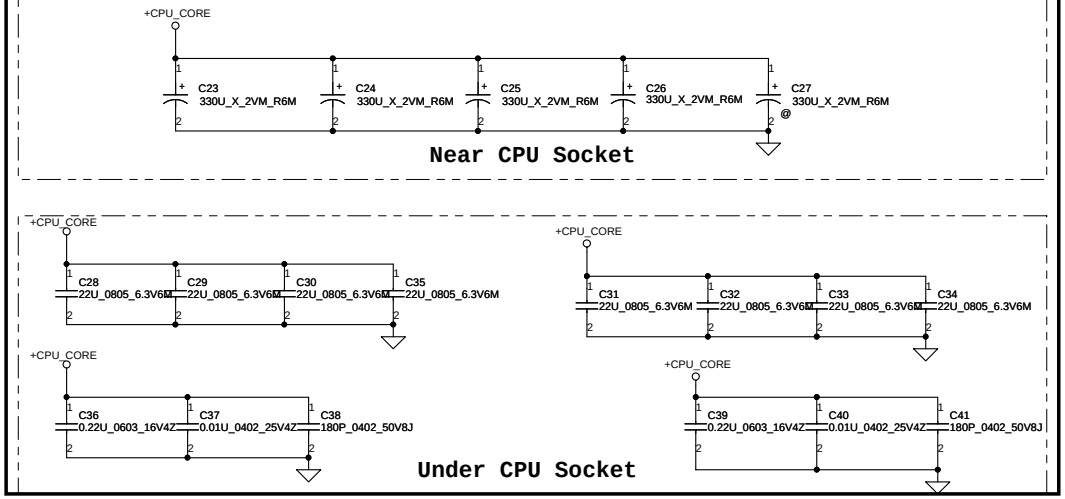
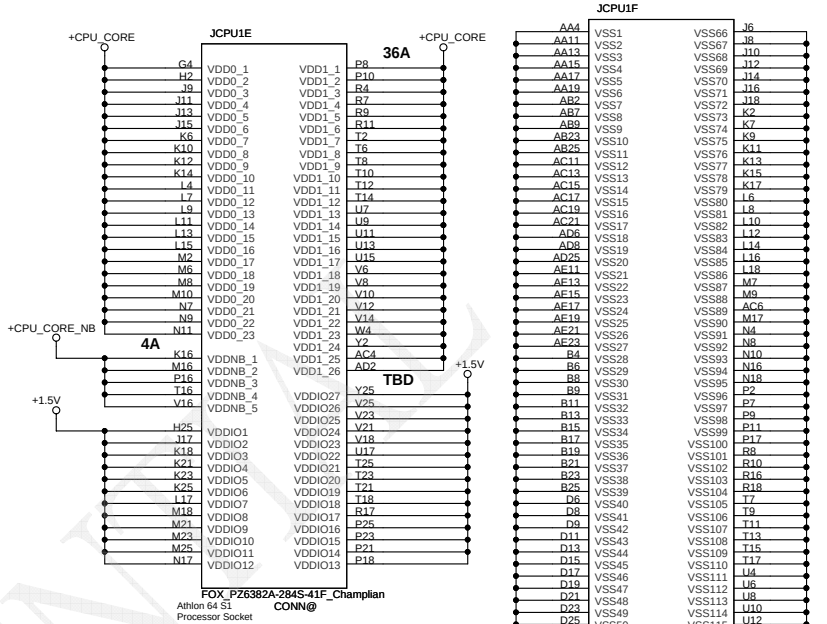
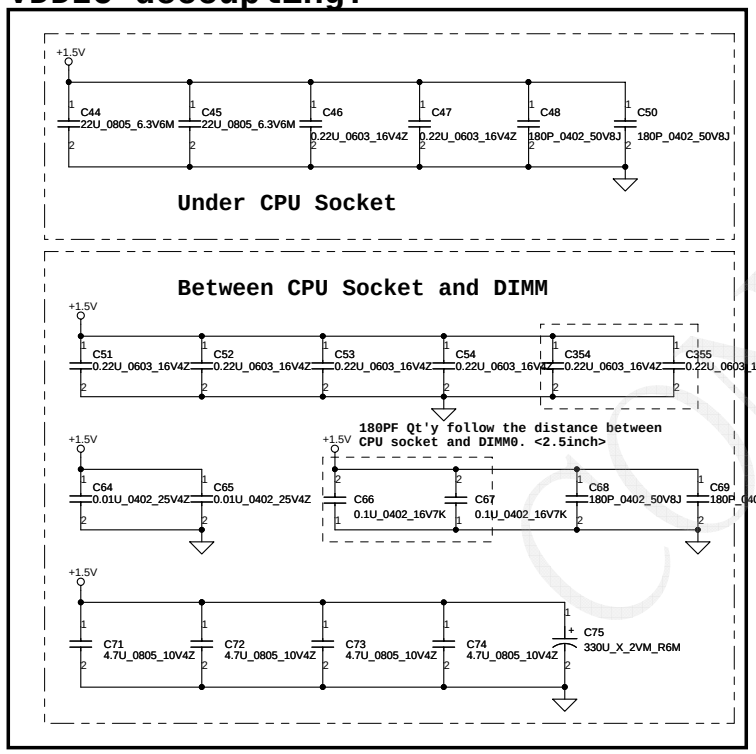
VDD(+CPU_CORE) decoupling.

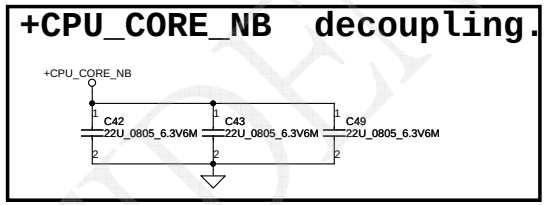




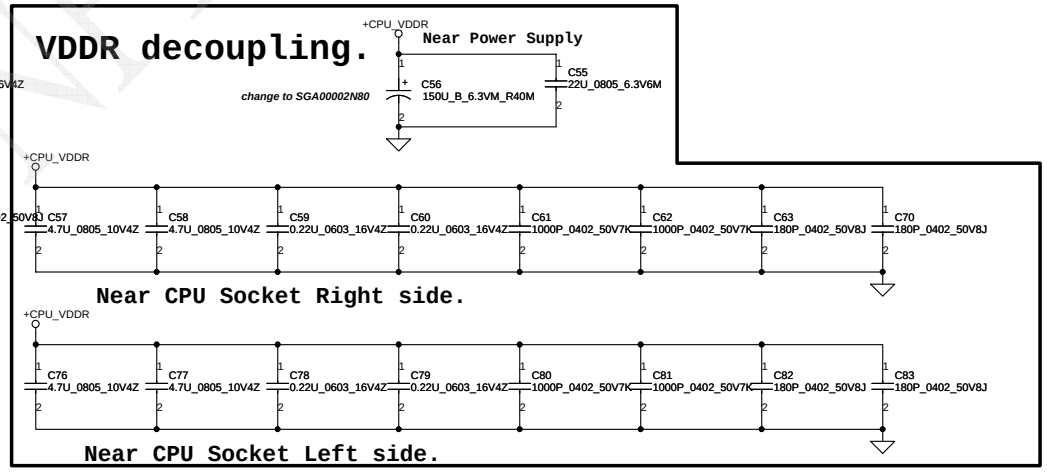
VDDIO decoupling.



+CPU_CORE_NB decoupling.



VDDR decoupling.



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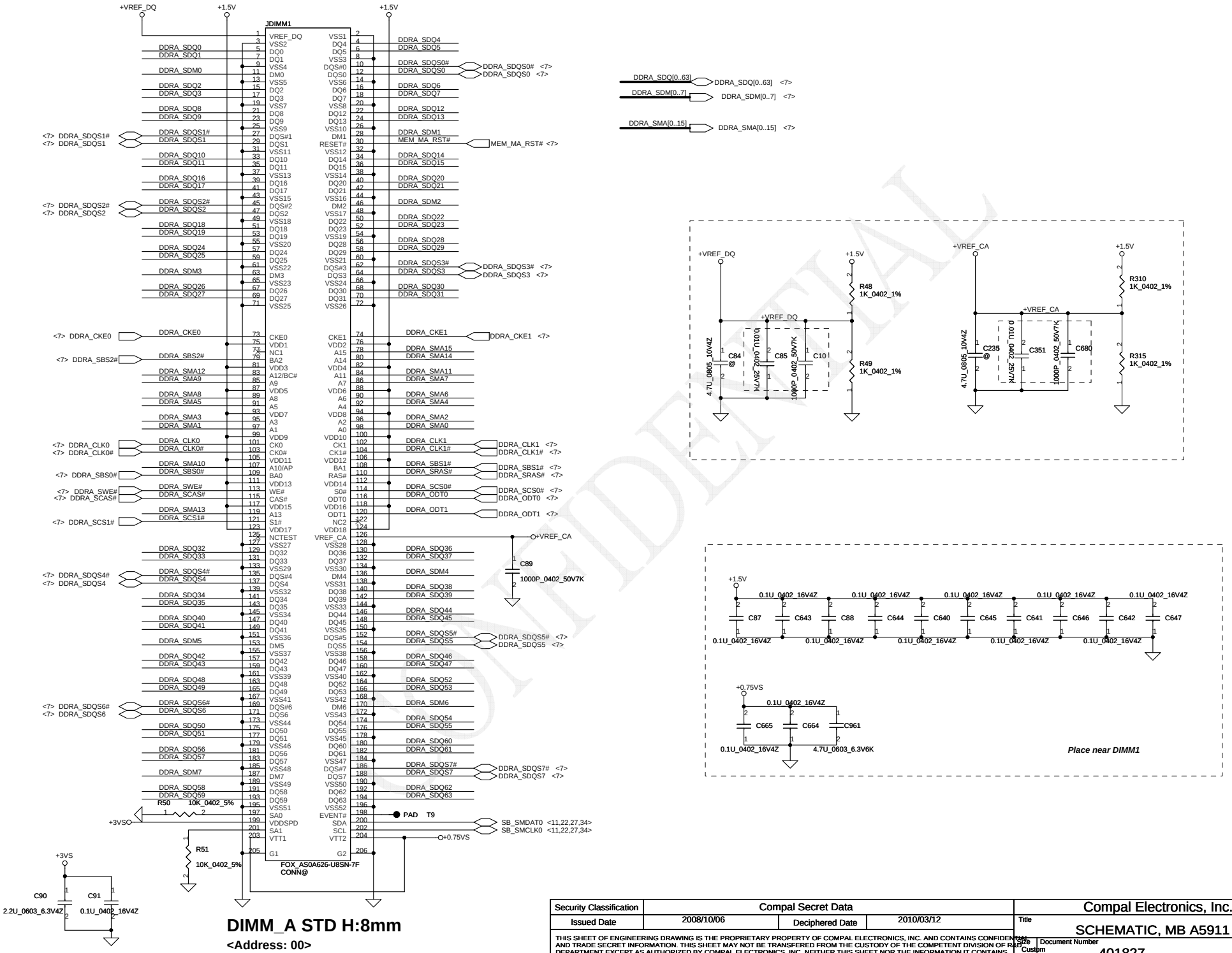

DIMM_A STD H:8mm

<Address: 00>

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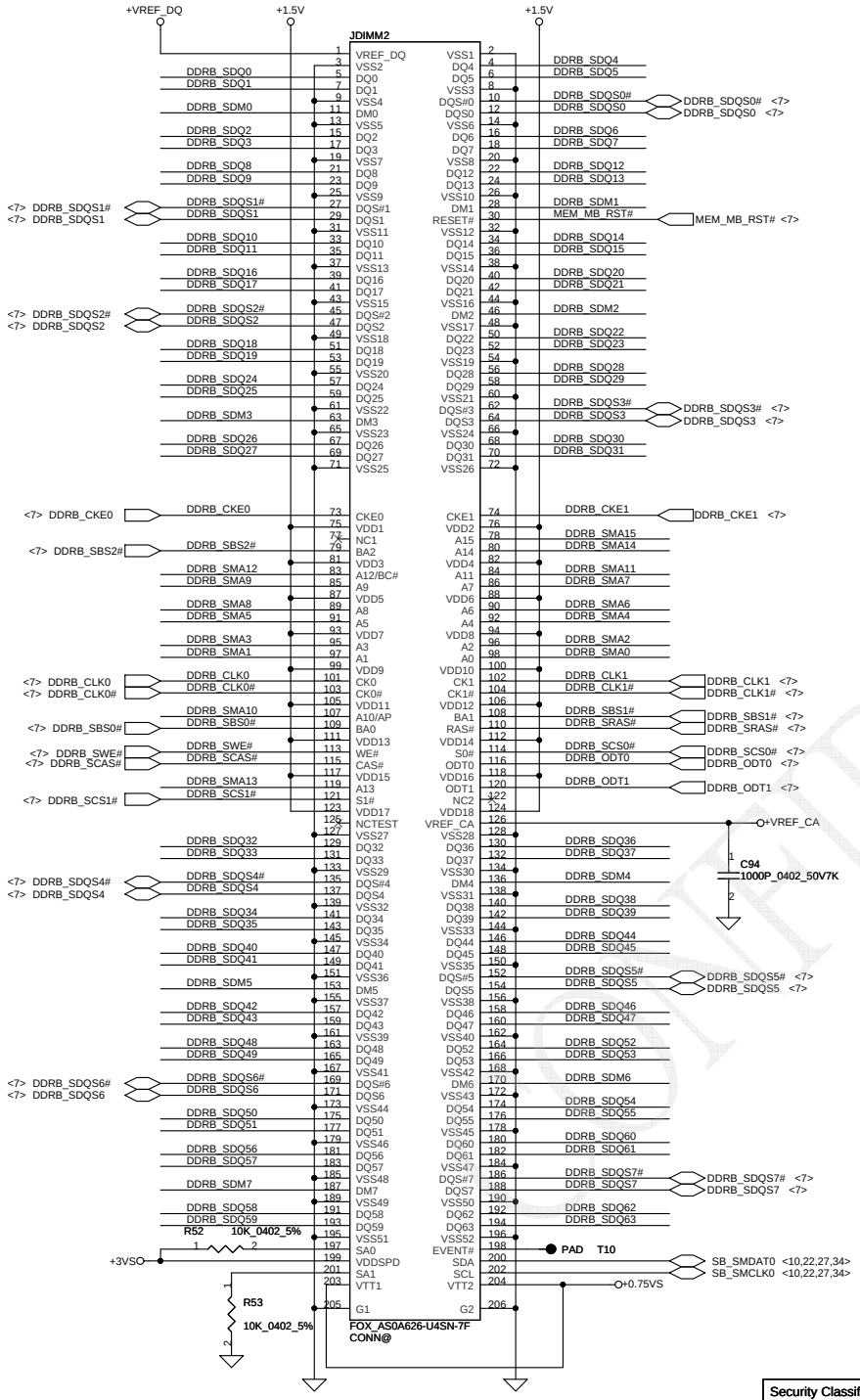
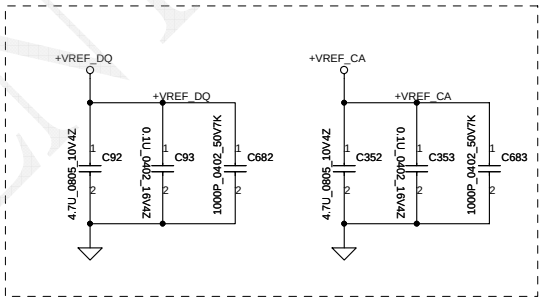
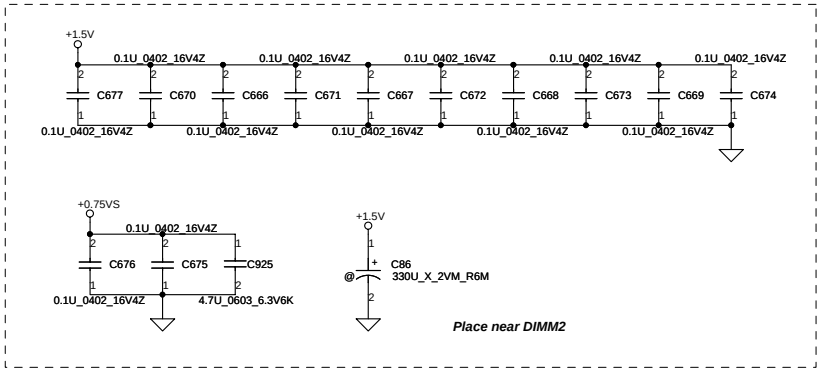


DDRB_SDQ[0..63] DDRB_SDQ[0..63] <7>

DDRB_SDM[0..7] DDRB_SDM[0..7] <7>

DDRB_SMA[0..15] DDRB_SMA[0..15] <7>





DIMM_B STD H:4mm

<Address: 01>

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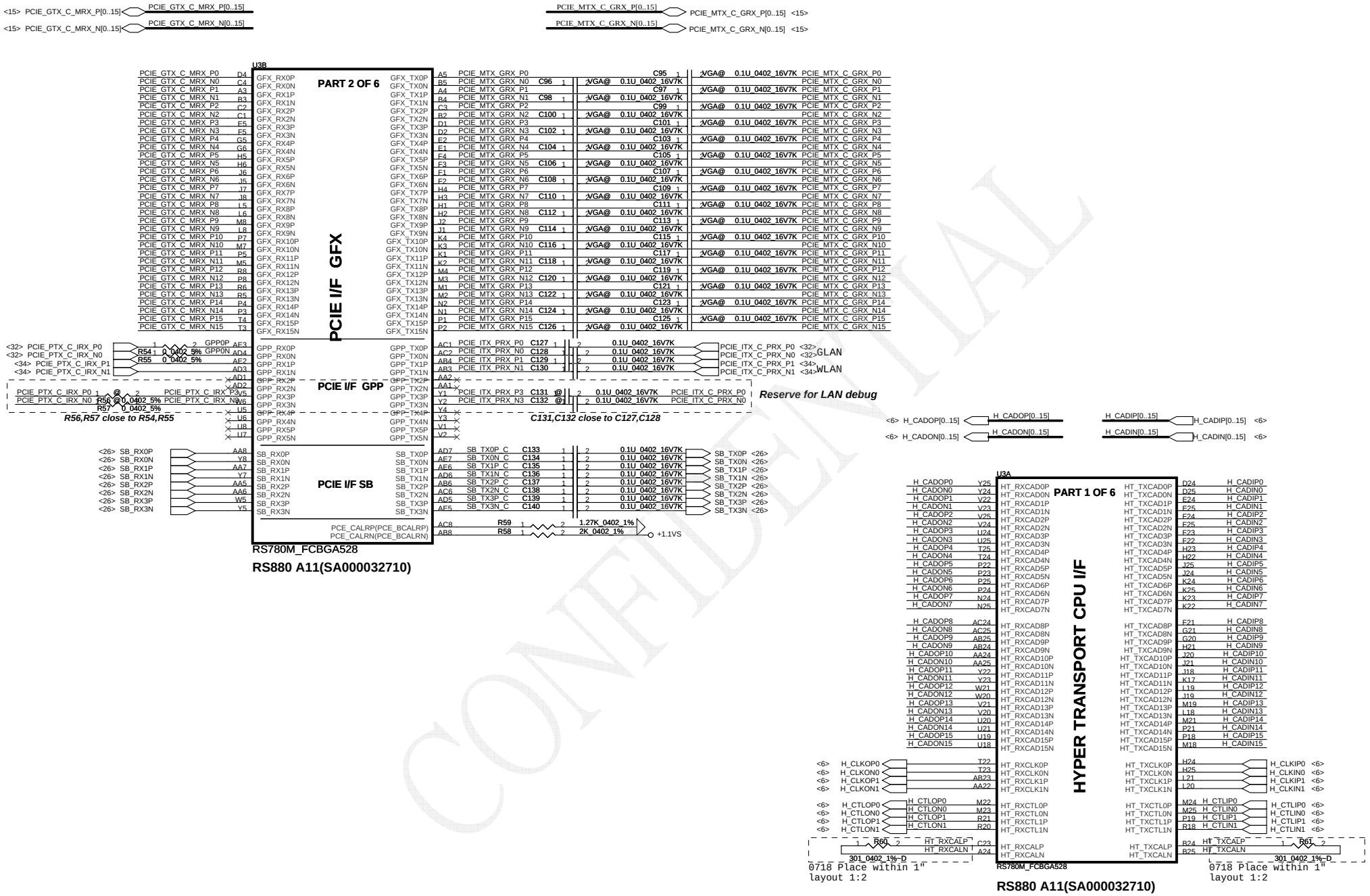

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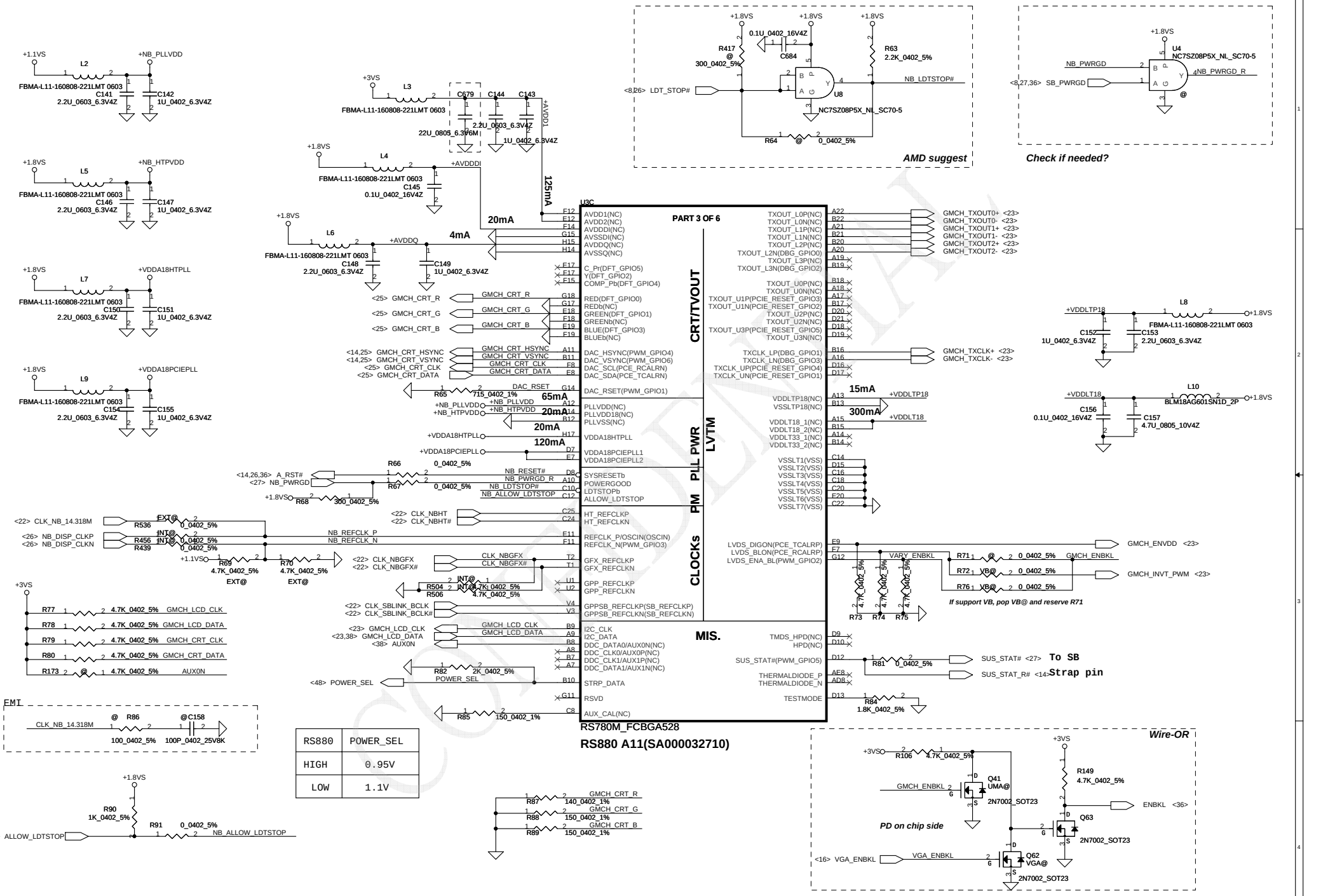

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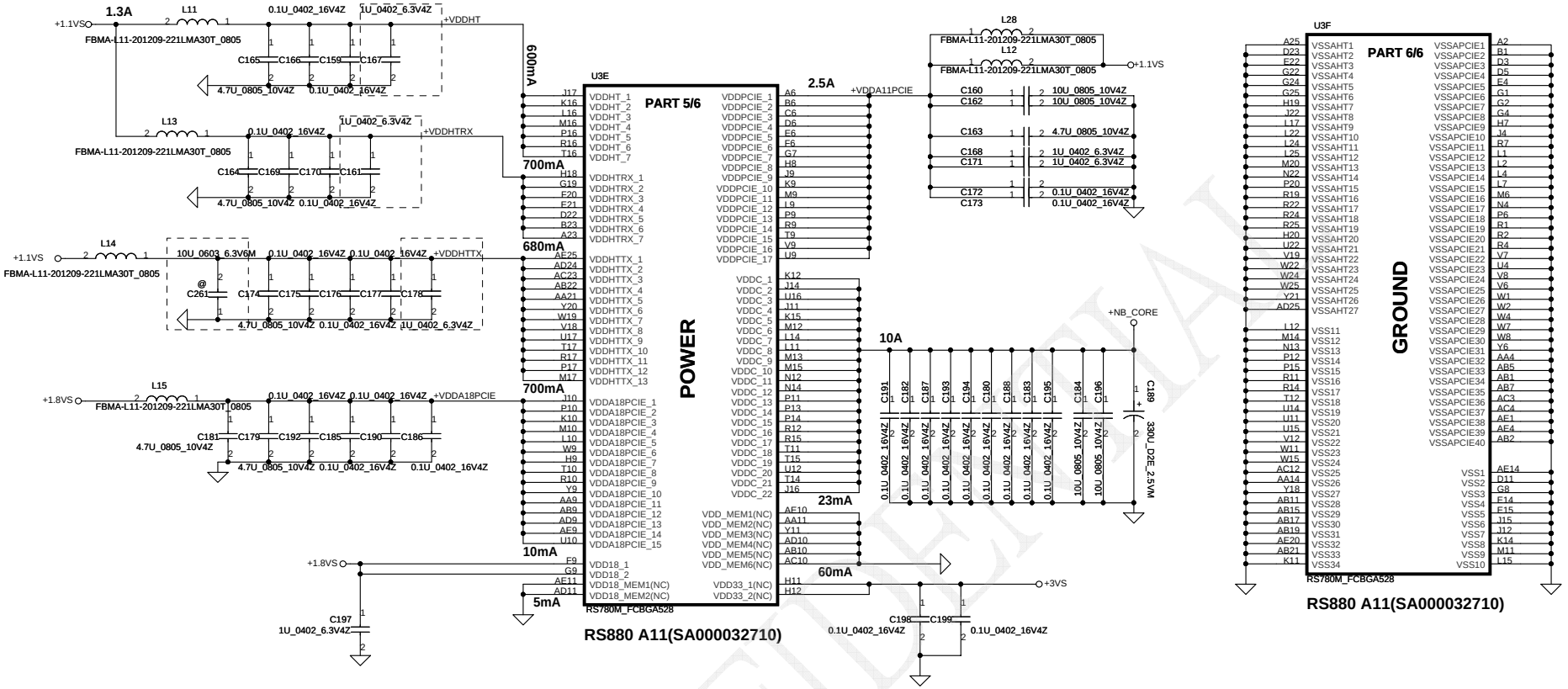


Side port and Strap setting

Debug Mode

<13,25> GMCH_CRT_VSYNC — R92 3K_0402_5% — +3VS; R93 @ 3K_0402_5%

Load EEPROM Strap

D1 @ CH751H-40PT_SOD323-2

<13> SUS_STAT_R# — A_RST# <13,26,36>; R264 @ 3K_0402_5%

Enable Side Port Memory

<13,25> GMCH_CRT_HSYNC — R94 3K_0402_5% — +3VS; R95 @ 3K_0402_5%

DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEb

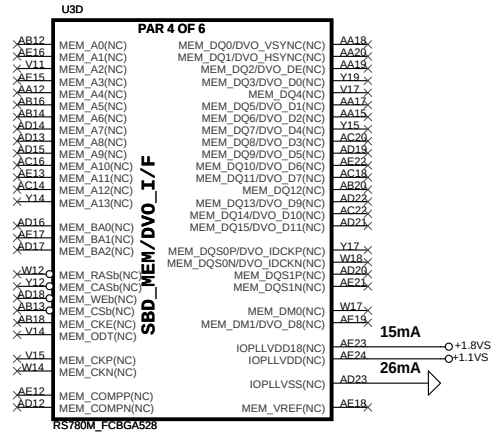
```
Enables the Test Debug Bus using GPIO. (VSYNC)
1 : Disable
0 : Enable
```

DFT_GPIO1: LOAD_EEPROM_STRAPS

```
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
default values if not connected
```

Enable Side Port Memory

```
RS880: HSYNC#
0:   Enable        Register Readback of strap:
1 :  Disable       NB_CLKCFG:CLK_TOP_SPARE_D[1]
```



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Issued Date	2008/10/06	Deciphered Date 2010/03/12	Title: SCHEMATIC, MB A5911
Size: Custom	Document Number: 401827		Rev: D
Date: Tuesday, September 14, 2010	Sheet 14 of 55		

<12> PCIE_GTX_C_MRX_P[0..15] → PCIE_GTX_C_MRX_P[0..15]
<12> PCIE_GTX_C_MRX_N[0..15] → PCIE_GTX_C_MRX_N[0..15]
PCIE_MTX_C_GRX_P[0..15] → PCIE_MTX_C_GRX_P[0..15] <12>
PCIE_MTX_C_GRX_N[0..15] → PCIE_MTX_C_GRX_N[0..15] <12>

GFX PCIE LANE REVERSAL

U5A

PCIE_MTX_C_GRX_P15	AA38	PCIE_RX0P	PCIE_TX0P	Y33	PCIE_GTX_MRX_P15	C200	0.1U_0402_16V7K	PCIE_GTX_C_MRX_P15	
PCIE_MTX_C_GRX_N15	Y37	PCIE_RX0N	PCIE_TX0N	Y32	PCIE_GTX_MRX_N15	C201	0.1U_0402_16V7K	PCIE_GTX_C_MRX_N15	VGA@
PCIE_MTX_C_GRX_P14	Y35	PCIE_RX1P	PCIE_TX1P	W33	PCIE_GTX_MRX_P14	C202	0.1U_0402_16V7K	PCIE_GTX_C_MRX_P14	
PCIE_MTX_C_GRX_N14	W36	PCIE_RX1N	PCIE_TX1N	W32	PCIE_GTX_MRX_N14	C203	0.1U_0402_16V7K	PCIE_GTX_C_MRX_N14	VGA@
PCIE_MTX_C_GRX_P13	W38	PCIE_RX2P	PCIE_TX2P	U33	PCIE_GTX_MRX_P13	C204	0.1U_0402_16V7K	PCIE_GTX_C_MRX_P13	
PCIE_MTX_C_GRX_N13	V37	PCIE_RX2N	PCIE_TX2N	U32	PCIE_GTX_MRX_N13	C205	0.1U_0402_16V7K	PCIE_GTX_C_MRX_N13	VGA@
PCIE_MTX_C_GRX_P12	V35	PCIE_RX3P	PCIE_TX3P	U30	PCIE_GTX_MRX_P12	C206	0.1U_0402_16V7K	PCIE_GTX_C_MRX_P12	
PCIE_MTX_C_GRX_N12	U36	PCIE_RX3N	PCIE_TX3N	U29	PCIE_GTX_MRX_N12	C207	0.1U_0402_16V7K	PCIE_GTX_C_MRX_N12	VGA@
PCIE_MTX_C_GRX_P11	U38	PCIE_RX4P	PCIE_TX4P	T33	PCIE_GTX_MRX_P11	C208	0.1U_0402_16V7K	PCIE_GTX_C_MRX_P11	
PCIE_MTX_C_GRX_N11	T37	PCIE_RX4N	PCIE_TX4N	T32	PCIE_GTX_MRX_N11	C209	0.1U_0402_16V7K	PCIE_GTX_C_MRX_N11	VGA@
PCIE_MTX_C_GRX_P10	T35	PCIE_RX5P	PCIE_TX5P	T30	PCIE_GTX_MRX_P10	C210	0.1U_0402_16V7K	PCIE_GTX_C_MRX_P10	
PCIE_MTX_C_GRX_N10	R36	PCIE_RX5N	PCIE_TX5N	T29	PCIE_GTX_MRX_N10	C211	0.1U_0402_16V7K	PCIE_GTX_C_MRX_N10	VGA@
PCIE_MTX_C_GRX_P9	R38	PCIE_RX6P	PCIE_TX6P	P33	PCIE_GTX_MRX_P9	C212	0.1U_0402_16V7K	PCIE_GTX_C_MRX_P9	
PCIE_MTX_C_GRX_N9	P37	PCIE_RX6N	PCIE_TX6N	P32	PCIE_GTX_MRX_N9	C213	0.1U_0402_16V7K	PCIE_GTX_C_MRX_N9	VGA@
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PCIE_MTX_C_GRX_N8	N36	PCIE_RX7N	PCIE_TX7N	P29	PCIE_GTX_MRX_N8	C215	0.1U_0402_16V7K	PCIE_GTX_C_MRX_N8	VGA@
PCIE_MTX_C_GRX_P7	N38	PCIE_RX8P	PCIE_TX8P	N33	PCIE_GTX_MRX_P7	C216	0.1U_0402_16V7K	PCIE_GTX_C_MRX_P7	
PCIE_MTX_C_GRX_N7	M37	PCIE_RX8N	PCIE_TX8N	N32	PCIE_GTX_MRX_N7	C217	0.1U_0402_16V7K	PCIE_GTX_C_MRX_N7	VGA@
PCIE_MTX_C_GRX_P6	M35	PCIE_RX9P	PCIE_TX9P	N30	PCIE_GTX_MRX_P6	C218	0.1U_0402_16V7K	PCIE_GTX_C_MRX_P6	
PCIE_MTX_C_GRX_N6	L36	PCIE_RX9N	PCIE_TX9N	N29	PCIE_GTX_MRX_N6	C219	0.1U_0402_16V7K	PCIE_GTX_C_MRX_N6	VGA@
PCIE_MTX_C_GRX_P5	L38	PCIE_RX10P	PCIE_TX10P	L33	PCIE_GTX_MRX_P5	C220	0.1U_0402_16V7K	PCIE_GTX_C_MRX_P5	
PCIE_MTX_C_GRX_N5	K37	PCIE_RX10N	PCIE_TX10N	L32	PCIE_GTX_MRX_N5	C221	0.1U_0402_16V7K	PCIE_GTX_C_MRX_N5	VGA@
PCIE_MTX_C_GRX_P4	K35	PCIE_RX11P	PCIE_TX11P	L30	PCIE_GTX_MRX_P4	C222	0.1U_0402_16V7K	PCIE_GTX_C_MRX_P4	
PCIE_MTX_C_GRX_N4	J36	PCIE_RX11N	PCIE_TX11N	L29	PCIE_GTX_MRX_N4	C223	0.1U_0402_16V7K	PCIE_GTX_C_MRX_N4	VGA@
PCIE_MTX_C_GRX_P3	J38	PCIE_RX12P	PCIE_TX12P	K33	PCIE_GTX_MRX_P3	C224	0.1U_0402_16V7K	PCIE_GTX_C_MRX_P3	
PCIE_MTX_C_GRX_N3	H37	PCIE_RX12N	PCIE_TX12N	K32	PCIE_GTX_MRX_N3	C225	0.1U_0402_16V7K	PCIE_GTX_C_MRX_N3	VGA@
PCIE_MTX_C_GRX_P2	H35	PCIE_RX13P	PCIE_TX13P	J33	PCIE_GTX_MRX_P2	C226	0.1U_0402_16V7K	PCIE_GTX_C_MRX_P2	
PCIE_MTX_C_GRX_N2	G36	PCIE_RX13N	PCIE_TX13N	J32	PCIE_GTX_MRX_N2	C227	0.1U_0402_16V7K	PCIE_GTX_C_MRX_N2	VGA@
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PCIE_MTX_C_GRX_N1	F37	PCIE_RX14N	PCIE_TX14N	K29	PCIE_GTX_MRX_N1	C229	0.1U_0402_16V7K	PCIE_GTX_C_MRX_N1	VGA@
PCIE_MTX_C_GRX_P0	F35	PCIE_RX15P	PCIE_TX15P	H33	PCIE_GTX_MRX_P0	C230	0.1U_0402_16V7K	PCIE_GTX_C_MRX_P0	
PCIE_MTX_C_GRX_N0	E37	PCIE_RX15N	PCIE_TX15N	H32	PCIE_GTX_MRX_N0	C231	0.1U_0402_16V7K	PCIE_GTX_C_MRX_N0	VGA@

PCI EXPRESS INTERFACE

CLOCK

<22> CLK_PEG_VGA → AB35 PCIE_REFCLKP
<22> CLK_PEG_VGA# → AA36 PCIE_REFCLKN

For M96, AH16 is NC
For Mahatten need PD

AJ21 NC#1
AK21 NC#2
AH16 NC_PWRGOOD
R99 2 1 VGA@ 10K_0402_5%

VGA_RST# → AA30 PERSTB

CALIBRATION

PCIE_CALRP Y30 R98 1 VGA@ 2 1.27K_0402_1%
PCIE_CALRN Y29 R100 1 VGA@ 2 2K_0402_1% +1.0VSG

216-0729002 A12 M96_BGA962
MAD@
MAD A12 (SA00003M300)

add for VB support.

U5G

LVDS CONTROL

VARY_BL AK27 → R96 10K_0402_5% → VGA_PNL_PWM <23>
DIGON AJ27 → R97 10K_0402_5% → VGA_ENVDD <23>

TXCLK_UP_DPF3P	AK35		
TXCLK_UN_DPF3N	AL36		
TXOUT_U0P_DPF2P	AJ38		
TXOUT_U0N_DPF2N	AK37		
TXOUT_U1P_DPF1P	AH35		
TXOUT_U1N_DPF1N	AJ36		
TXOUT_U2P_DPF0P	AG38		
TXOUT_U2N_DPF0N	AH37		
TXOUT_U3P	AE35		
TXOUT_U3N	AG36		

LVTMDP

TXCLK_LP_DPE3P	AP34	VGA_TXCLK+	VGA_TXCLK+ <23>
TXCLK_LN_DPE3N	AR34	VGA_TXCLK-	VGA_TXCLK- <23>
TXOUT_L0P_DPE2P	AW37	VGA_TXOUT0+	VGA_TXOUT0+ <23>
TXOUT_L0N_DPE2N	AU35	VGA_TXOUT0-	VGA_TXOUT0- <23>
TXOUT_L1P_DPE1P	AR37	VGA_TXOUT1+	VGA_TXOUT1+ <23>
TXOUT_L1N_DPE1N	AU39	VGA_TXOUT1-	VGA_TXOUT1- <23>
TXOUT_L2P_DPE0P	AP35	VGA_TXOUT2+	VGA_TXOUT2+ <23>
TXOUT_L2N_DPE0N	AR35	VGA_TXOUT2-	VGA_TXOUT2- <23>
TXOUT_L3P	AN36		
TXOUT_L3N	AP37		

216-0729002 A12 M96_BGA962
MAD@

U5 PARK@
PARK XT-M2 A11
PARK A11 (SA00003MC10)

+3VSG
R491 10K_0402_5% VGA@
<26,32,34> PLT_RST# → D45 RB751V_SOD323 VGA@ → VGA_RST#
<26> PE_GPIO0 → D44 RB751V_SOD323 SG@
R492 2.2K_0402_5% @ → +3VSG
Pop for PX verify

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Strap Name		Pin Straps description <all internal PD>	Setting
VIP_DEVICE_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver 0: Driver would ignore the value sampled on VHAD_0 during reset 1: VHAD_0 to determine whether or not a VIP slave device	0
VGA_DIS	GPIO9	VGA Disable determines 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Defailt setting for desktop)	1
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13,12,11 (config 2,1,0) : memory apertures a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. 128 MB 000 b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. 256 MB 001 * 64 MB 010	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0: Diable, 1: Enable	0
AUD[1] AUD(0)	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	11
BIF_GEN2_EN	GPIO2	0= Advertises the PCI-E device as 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	0
RESERVED	H2SYNC GPIO8 GPIO21	Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected	

External VGA Thermal Sensor

U6 VGA@ ADM1032ARMZ-2REEL_MSOP8

Address 1001 101X b

Q5B VGA@ DMN66D0LDW-7_SOT363-6

Q5A VGA@ DMN66D0LDW-7_SOT363-6

Location / VRAM	VRAM_ID3 <vendor1>	VRAM_ID2 <pcs> 64MX16	VRAM_ID1 <vendor2>	VRAM_ID0 <size>
Samsung	O	1 <4 pcs>	O	O
Hynix	1	1 <4 pcs>	O	O
AMD	1	1 <4 pcs>	1	O
Hynix(128MbX16)	1	1 <4 pcs>	O	1

Park (XT)

Location / VRAM	VRAM_ID3 <vandor>	VRAM_ID2 <size> 64MX16	VRAM_ID1	VRAM_ID0
Samsung	O	O <8 pcs>	O	O
Hynix	1	O <8 pcs>	O	O
AMD	1	O <8 pcs>	1	O
Hynix(128MbX16)	1	O <8 pcs>	O	1

Madsion (Pro)

For VGA boot unstable issue

FLASH ROM

A 1-Mbit serial EEPROM is required on GDDR5 designs DDR3 can be removed

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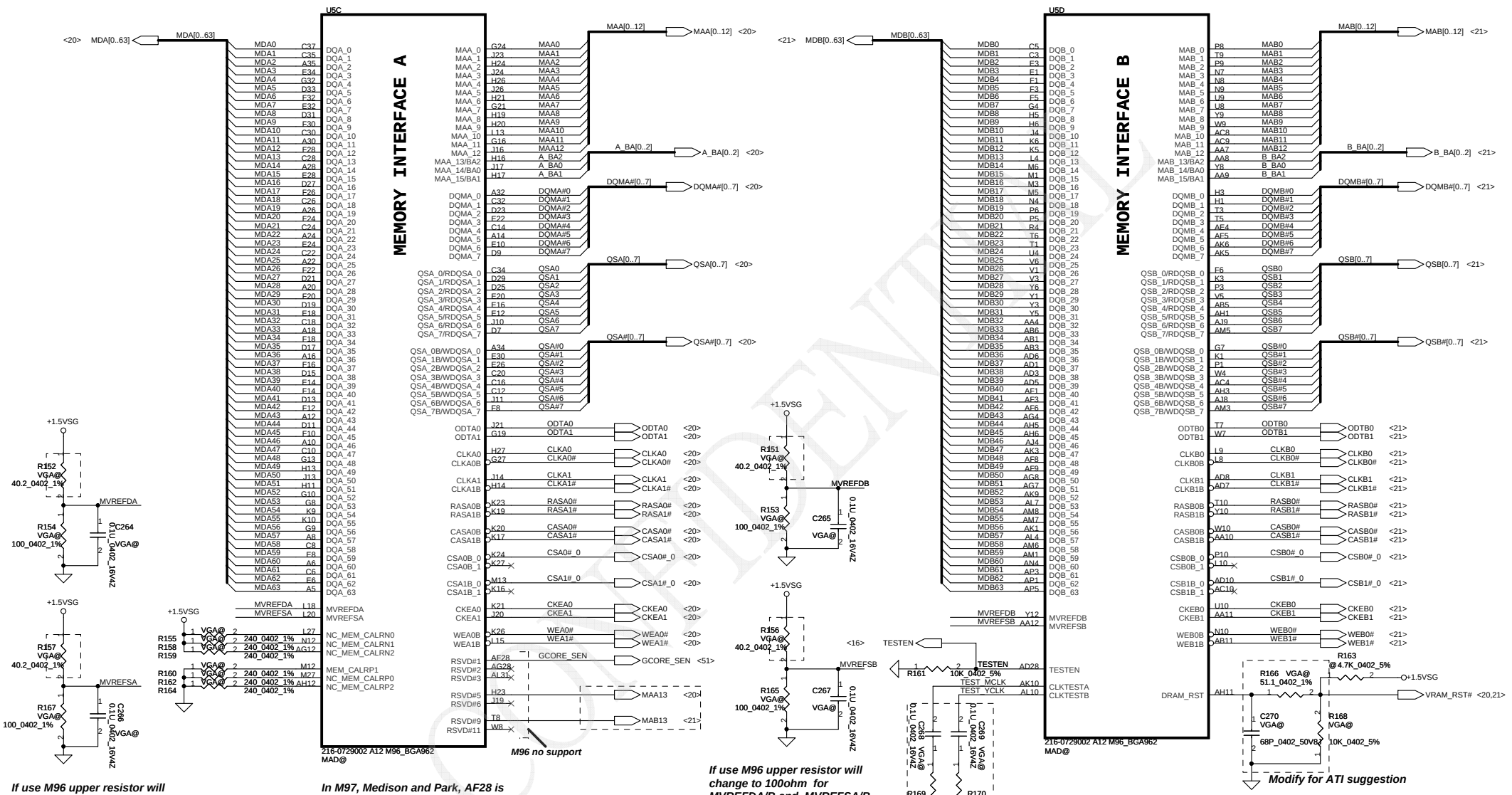
Park only support single channel memory (channel B only)



	M96	Broadway
R168	4.7k Ohm SD028470180	10K Ohm SD028100280
R166	0 Ohm SD028000080	680 Ohm SD028680080
R163	4.7k Ohm SD028470180	DNI
C270	1000 pF SE074102K80	68 pF SE071680J80

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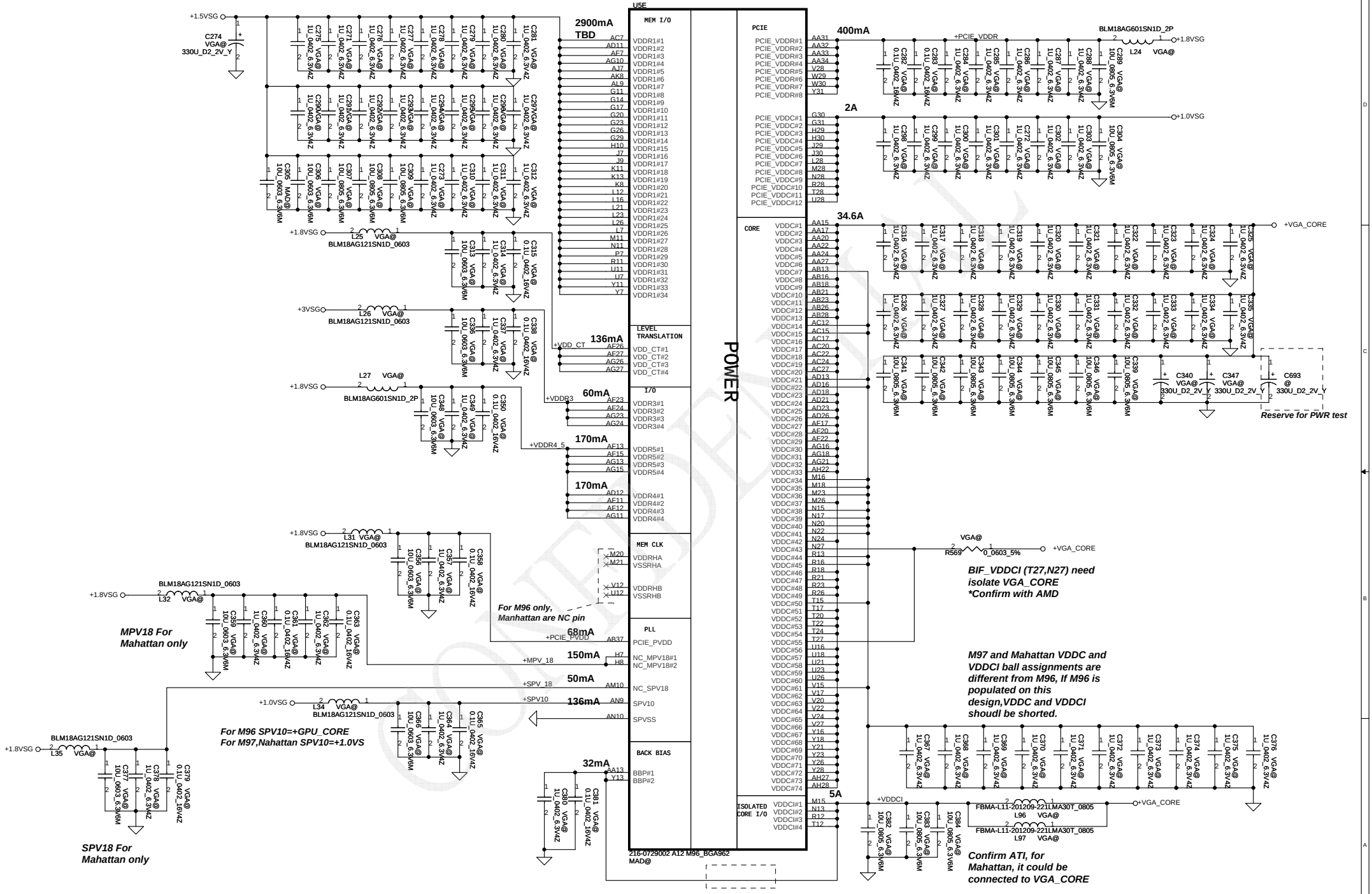

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Title: SCHEMATIC, MB A5911			
Size: Custom	Document Number: 401827		Rev: D
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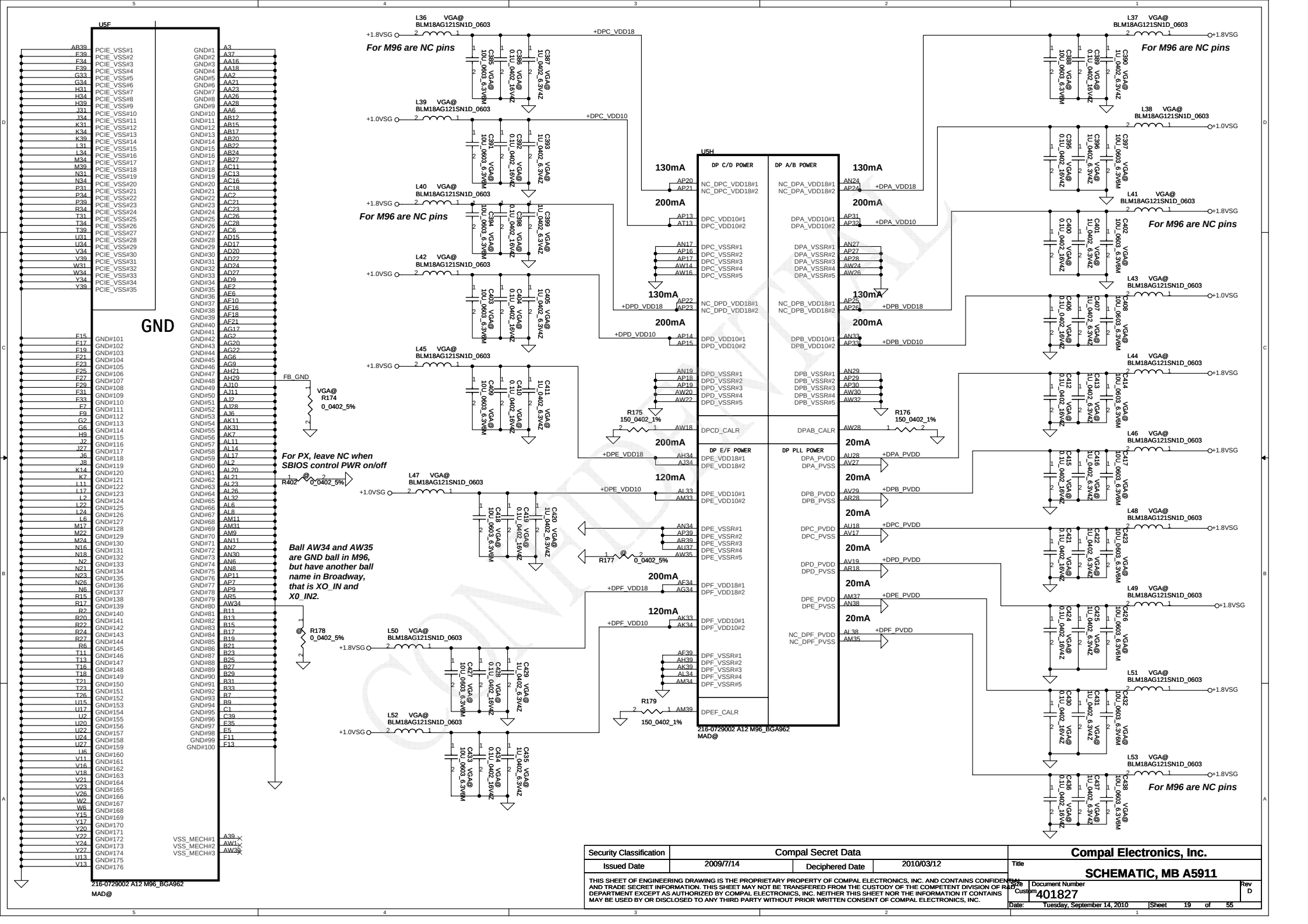

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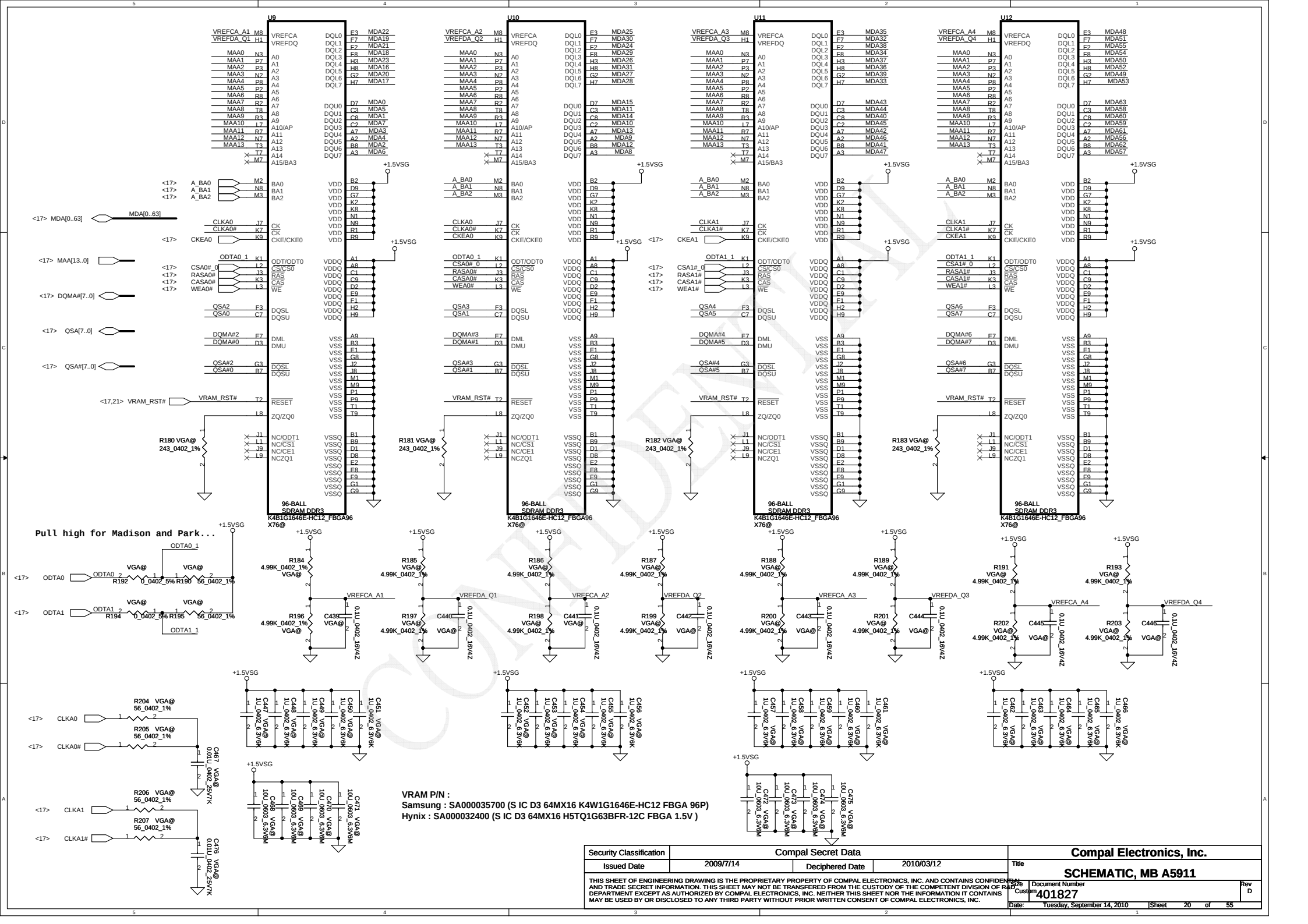

VRAM P/N :
Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)
Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)

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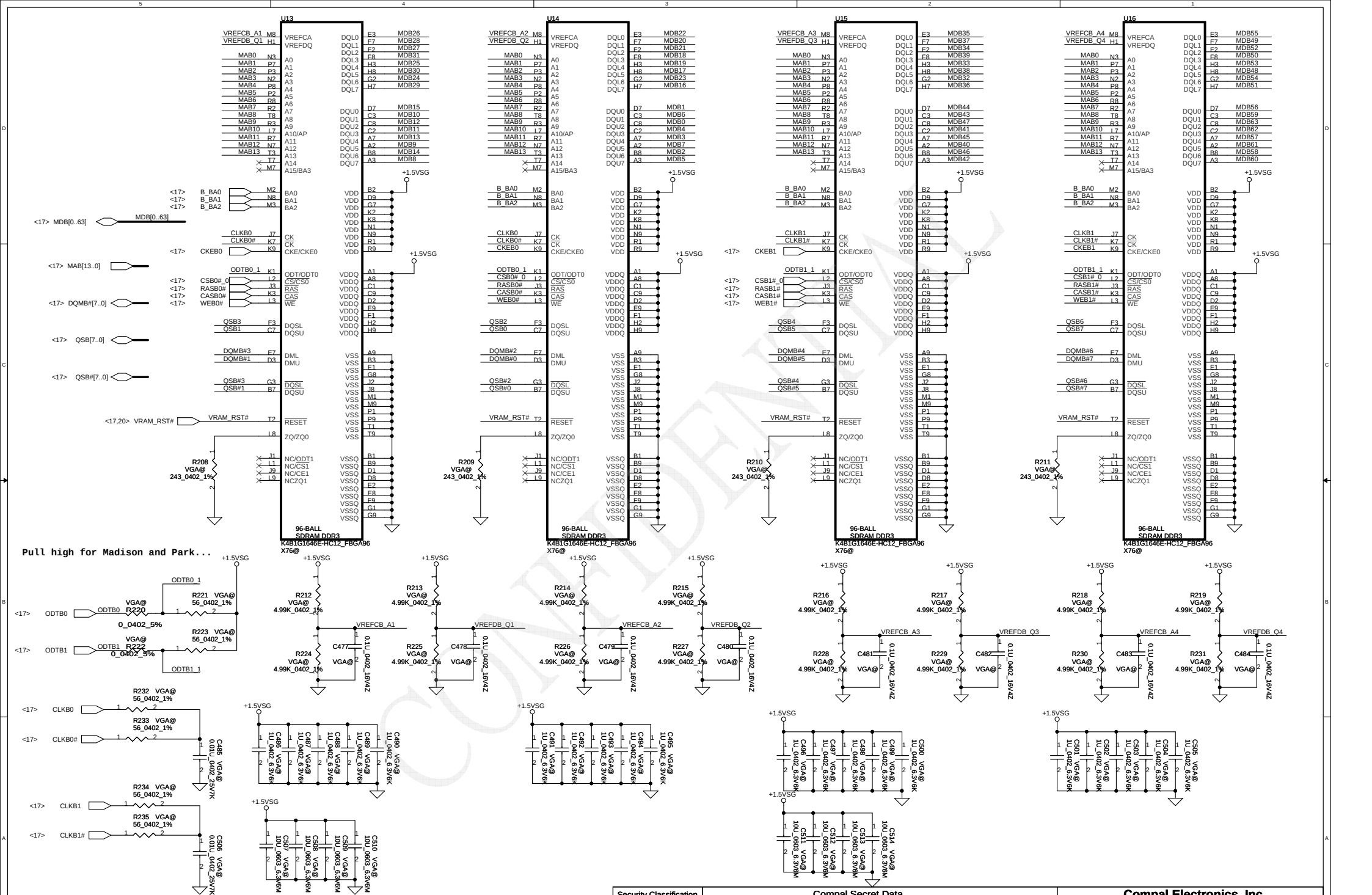

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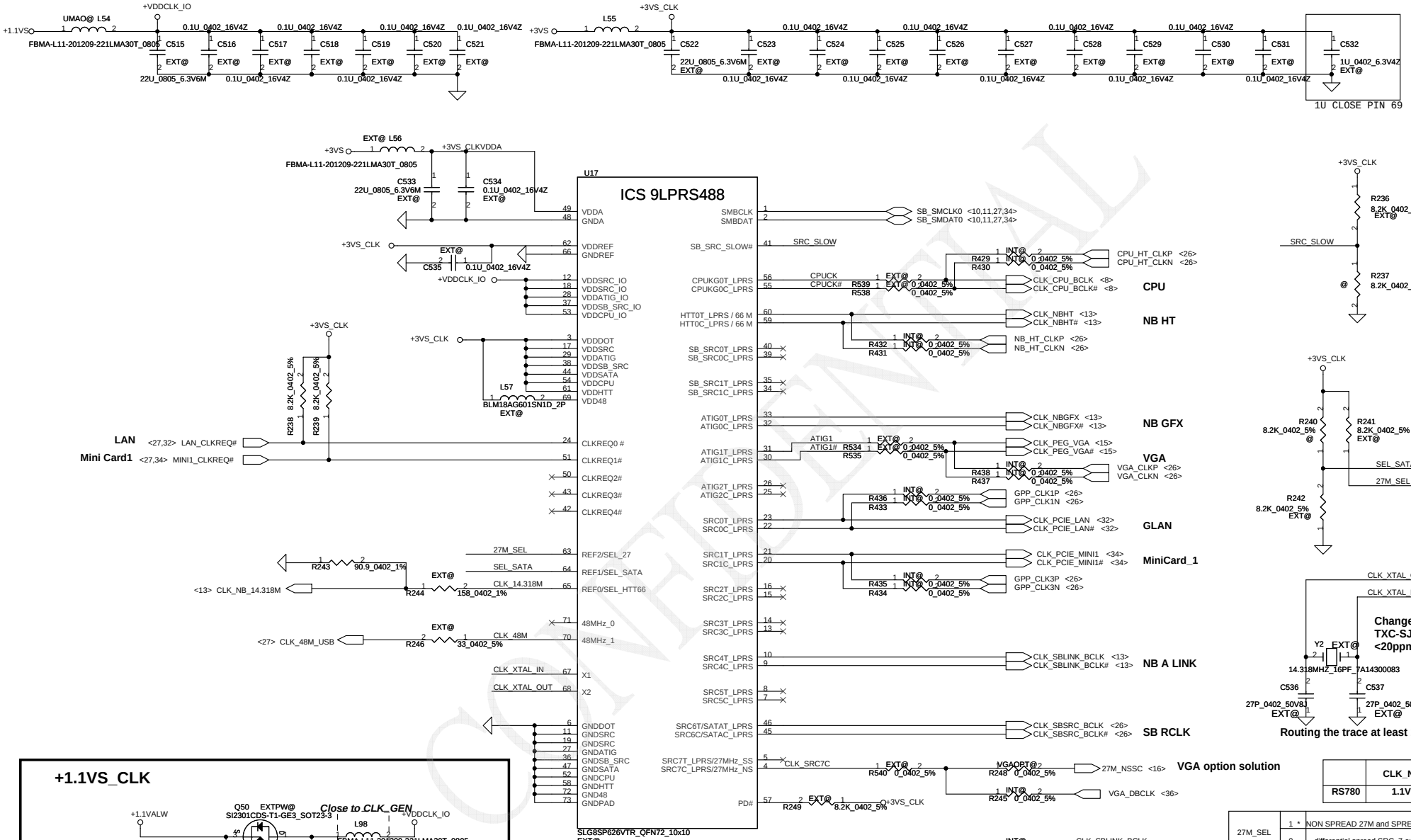
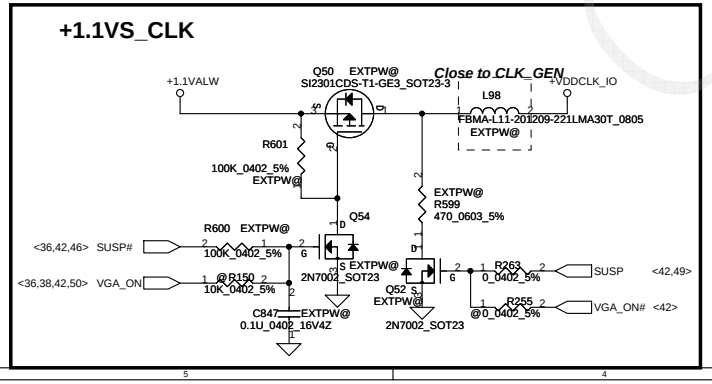


+1.1VS_CLK



1st (SILEGO) : SA00001Z310 S IC SLG8SP626VTR QFN 72P CLK GEN

2nd (ICS) : SA000023H10 S IC ICS9LPRS488CKLFT MLF 72P CLK GEN

	CLK_NB_14.318M
RS780	1.1V 158R/90.0R

27M_SEL	1 *	NON SPREAD 27M and SPREAD 27M output
	0	differential spread SRC_7 output
SEL_HTT66	1	single-ended 66MHz HTT output
	0 *	differential 100MHz HTT output
SEL_SATA	1 *	NON SPREAD 100M SATA SRC6 output
	0	SPREAD 100M SATA SRC6 output

* default

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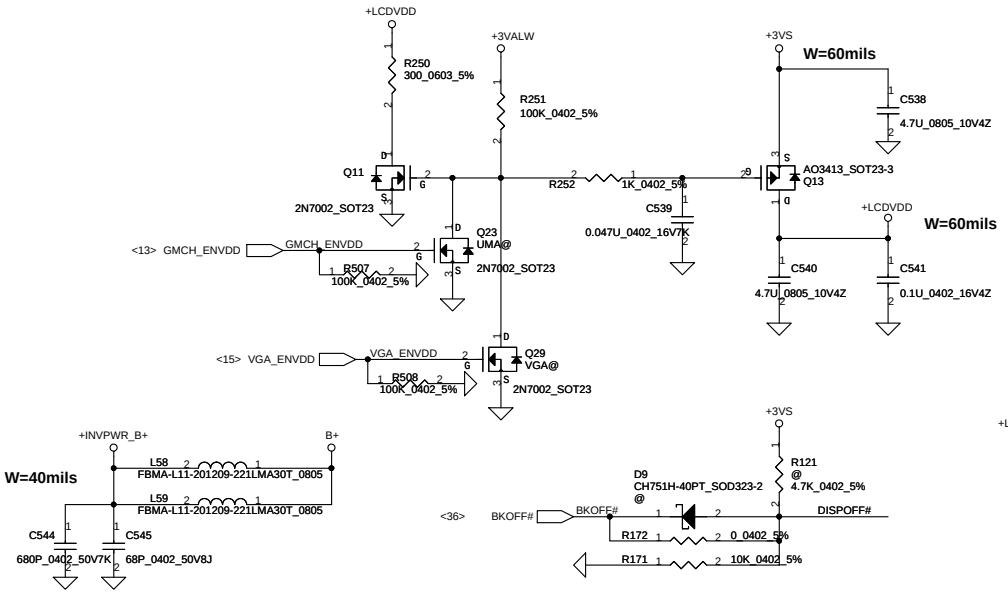
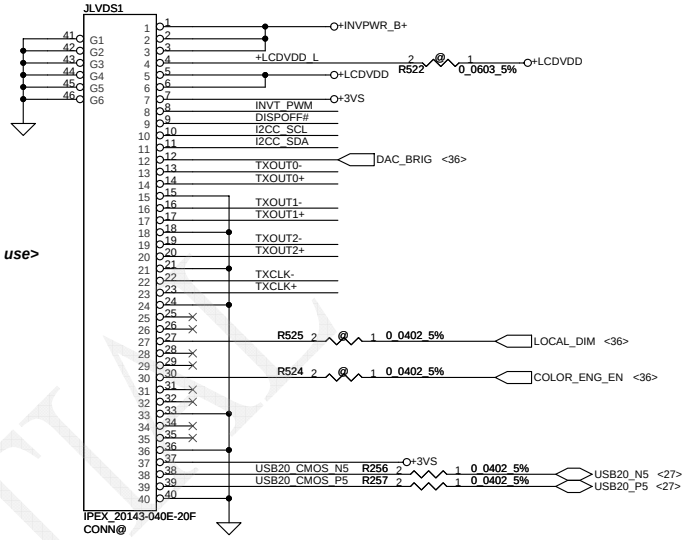
LCD POWER CIRCUIT



LCD/LED PANEL Conn.



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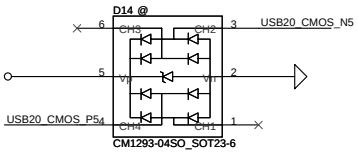
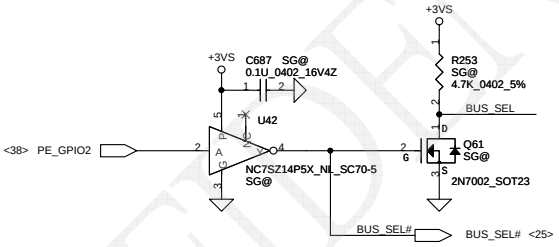
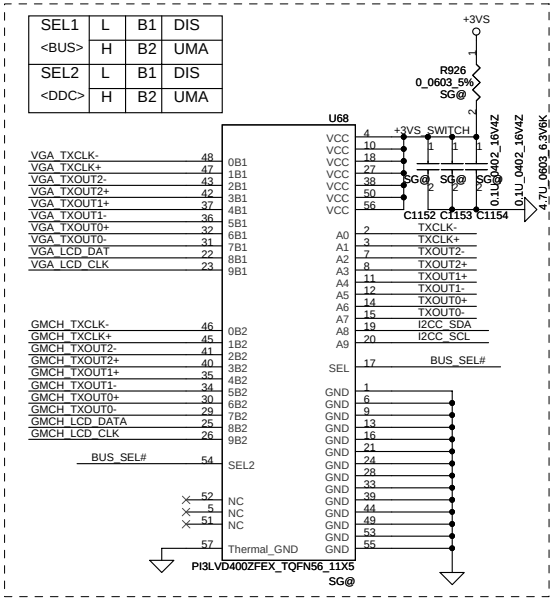
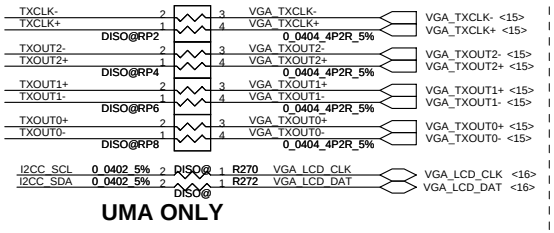




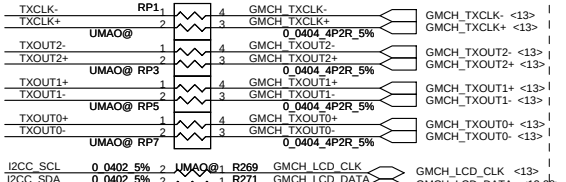
SEL1	L	B1	DIS
<BUS>	H	B2	UMA
SEL2	L	B1	DIS
<DDC>	H	B2	UMA

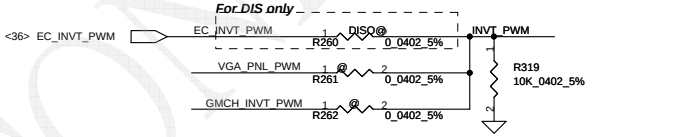


VGA ONLY

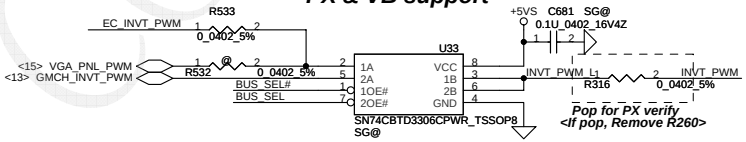


UMA ONLY





PX & VB support



1OE#	L	B1	DIS
	H	Z	
2OE#	L	B1	UMA
	H	Z	

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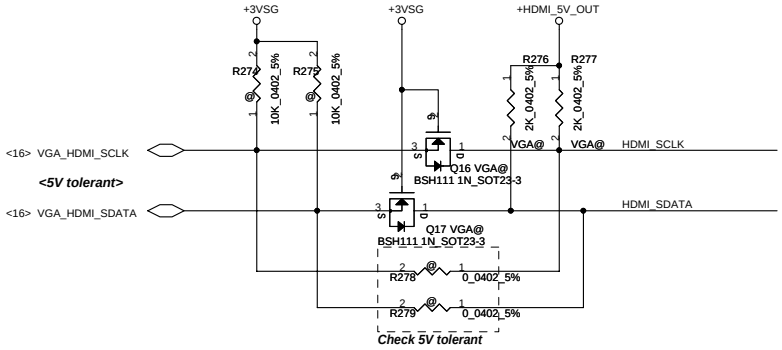
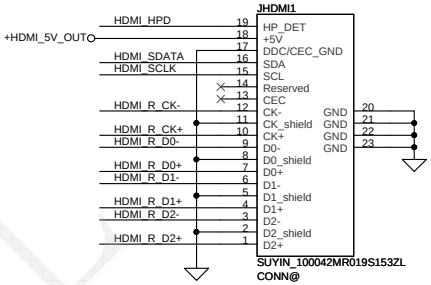
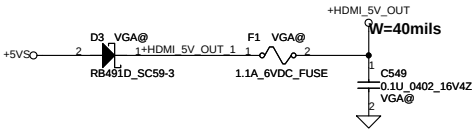
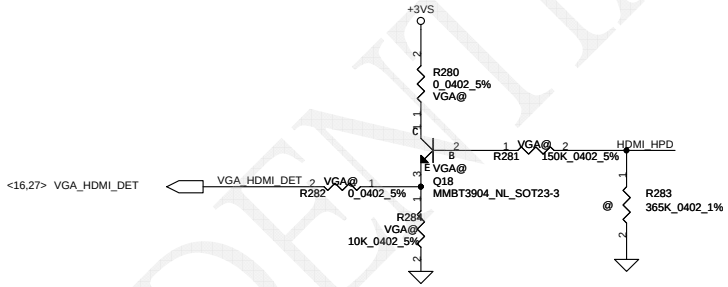
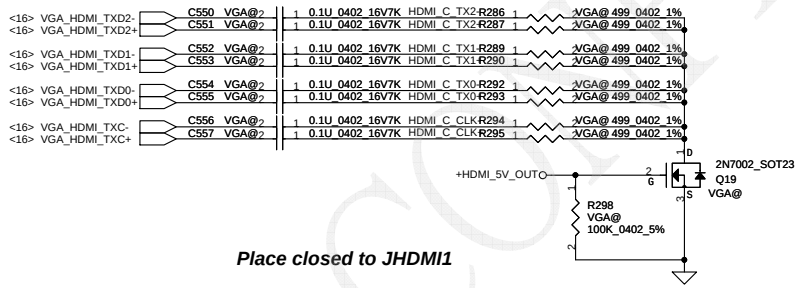




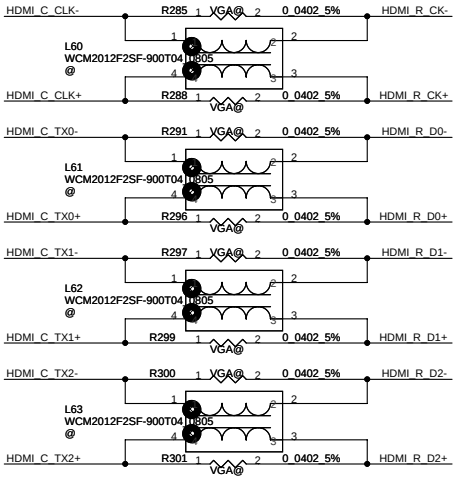
Place closed to JHDMI1







Place closed to JHDMI1



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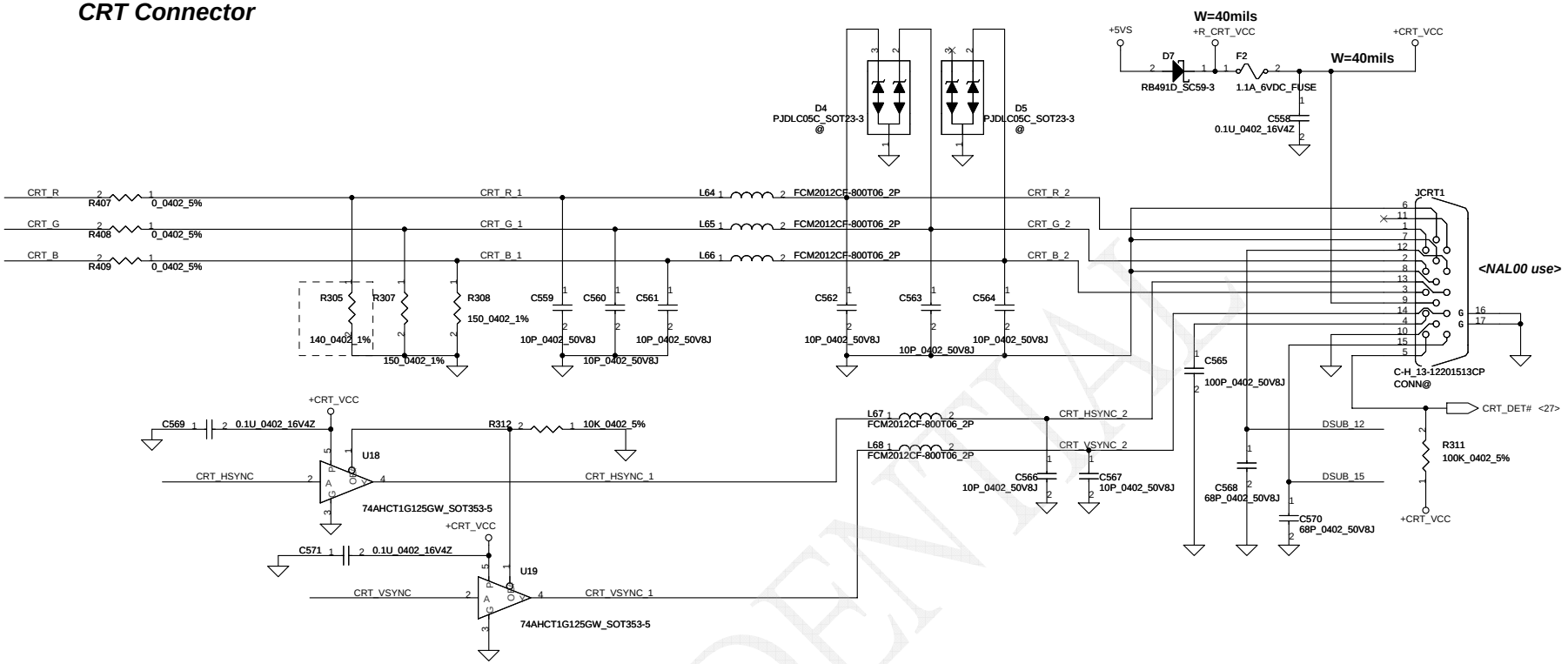
CRT Connector

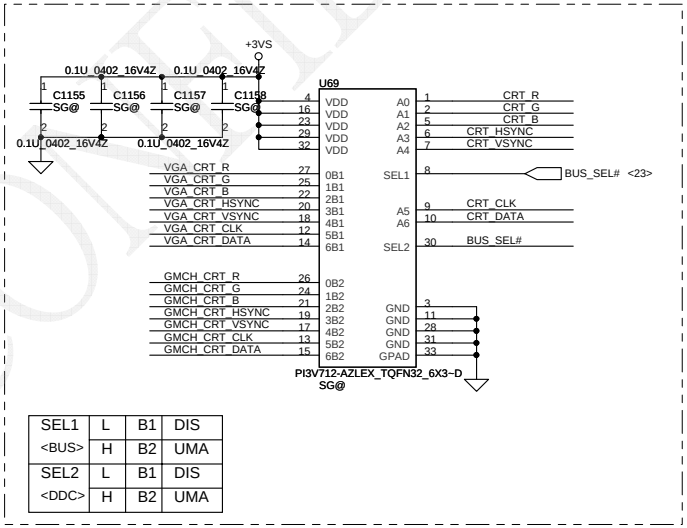


For UMA Only

<13> GMCH_CRT_R	GMCH_CRT_R	R266	UMA@	0_0402_5%	CRT_R
<13> GMCH_CRT_G	GMCH_CRT_G	R83	UMA@	0_0402_5%	CRT_G
<13> GMCH_CRT_B	GMCH_CRT_B	R268	UMA@	0_0402_5%	CRT_B
<13,14> GMCH_CRT_HSYNC	GMCH_CRT_HSYNC	R273	UMA@	0_0402_5%	CRT_HSYNC
<13,14> GMCH_CRT_VSYNC	GMCH_CRT_VSYNC	R267	UMA@	0_0402_5%	CRT_VSYNC
<13> GMCH_CRT_DATA	GMCH_CRT_DATA	R410	UMA@	0_0402_5%	CRT_DATA
<13> GMCH_CRT_CLK	GMCH_CRT_CLK	R406	UMA@	0_0402_5%	CRT_CLK

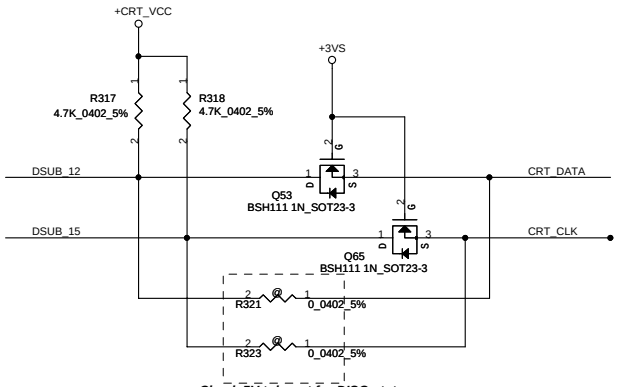
For VGA Only

<16> VGA_CRT_R	VGA_CRT_R	R306	DISO@	0_0402_5%	CRT_R
<16> VGA_CRT_G	VGA_CRT_G	R302	DISO@	0_0402_5%	CRT_G
<16> VGA_CRT_B	VGA_CRT_B	R304	DISO@	0_0402_5%	CRT_B
<16> VGA_CRT_HSYNC	VGA_CRT_HSYNC	R303	DISO@	0_0402_5%	CRT_HSYNC
<16> VGA_CRT_VSYNC	VGA_CRT_VSYNC	R309	DISO@	0_0402_5%	CRT_VSYNC
<16> VGA_CRT_DATA	VGA_CRT_DATA	R411	DISO@	0_0402_5%	CRT_DATA
<16> VGA_CRT_CLK	VGA_CRT_CLK	R412	DISO@	0_0402_5%	CRT_CLK



SEL1	L	B1	DIS
<BUS>	H	B2	UMA
SEL2	L	B1	DIS
<DDC>	H	B2	UMA

Close to Conn side



Check 5V tolerant for DISO state

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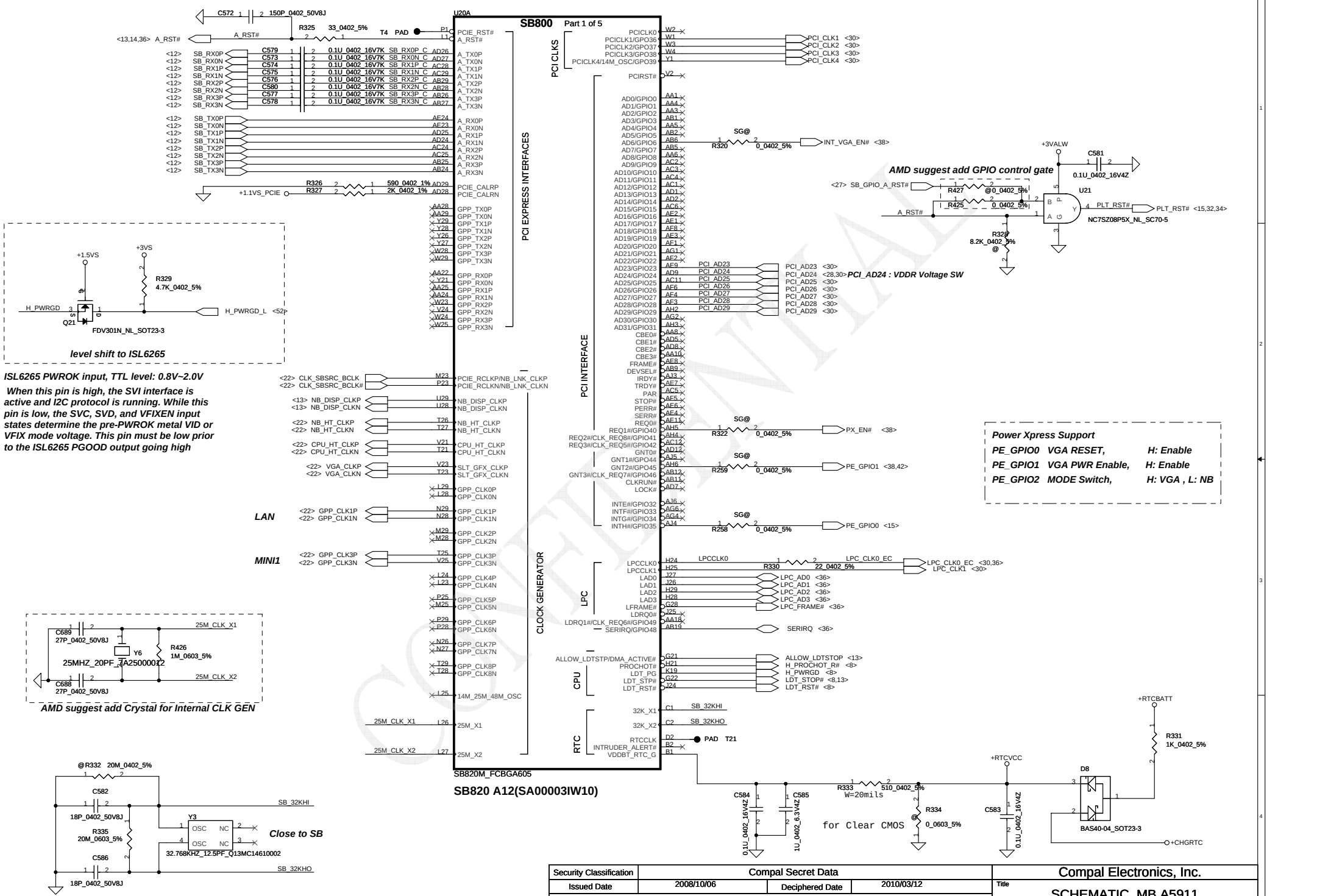

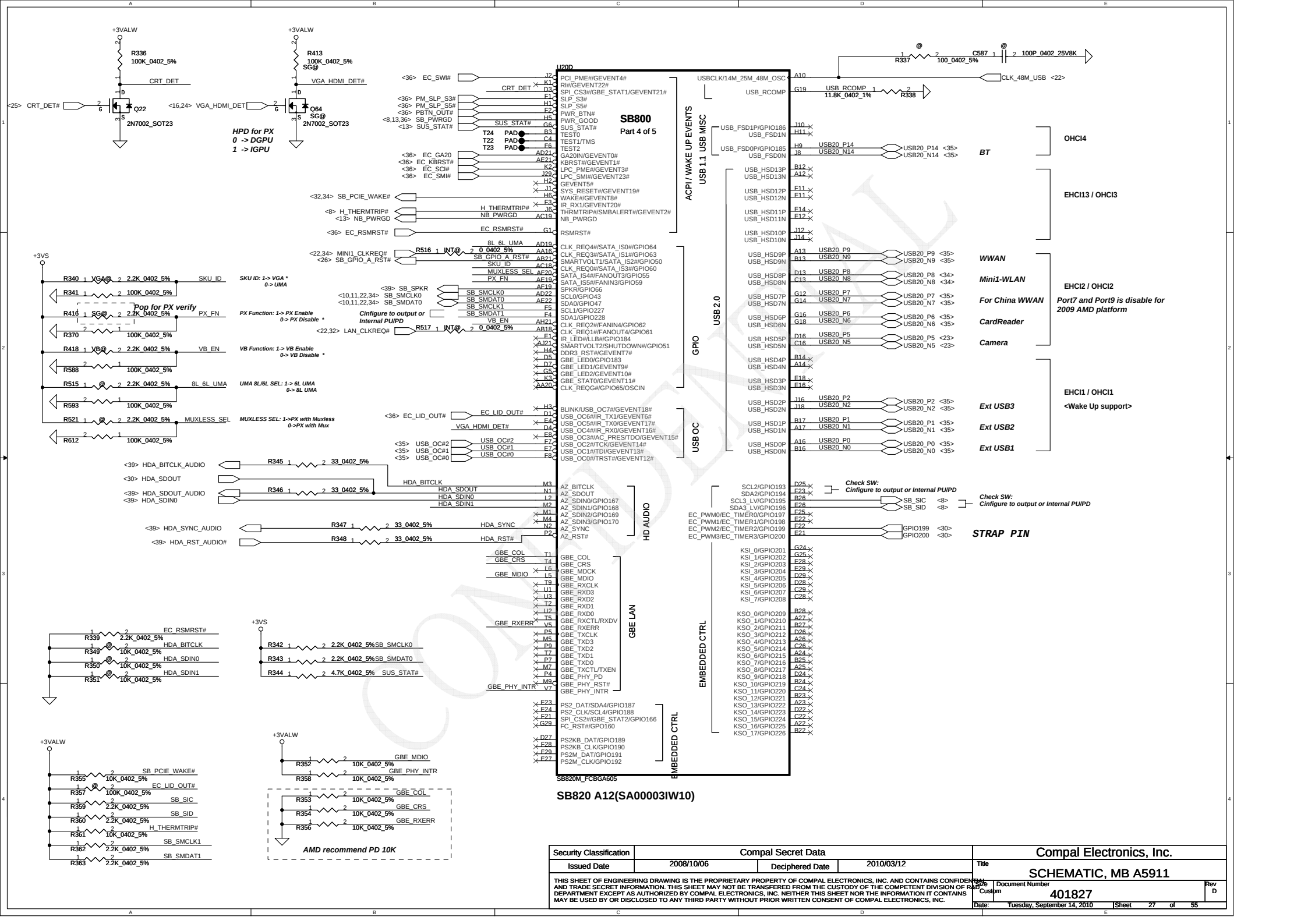

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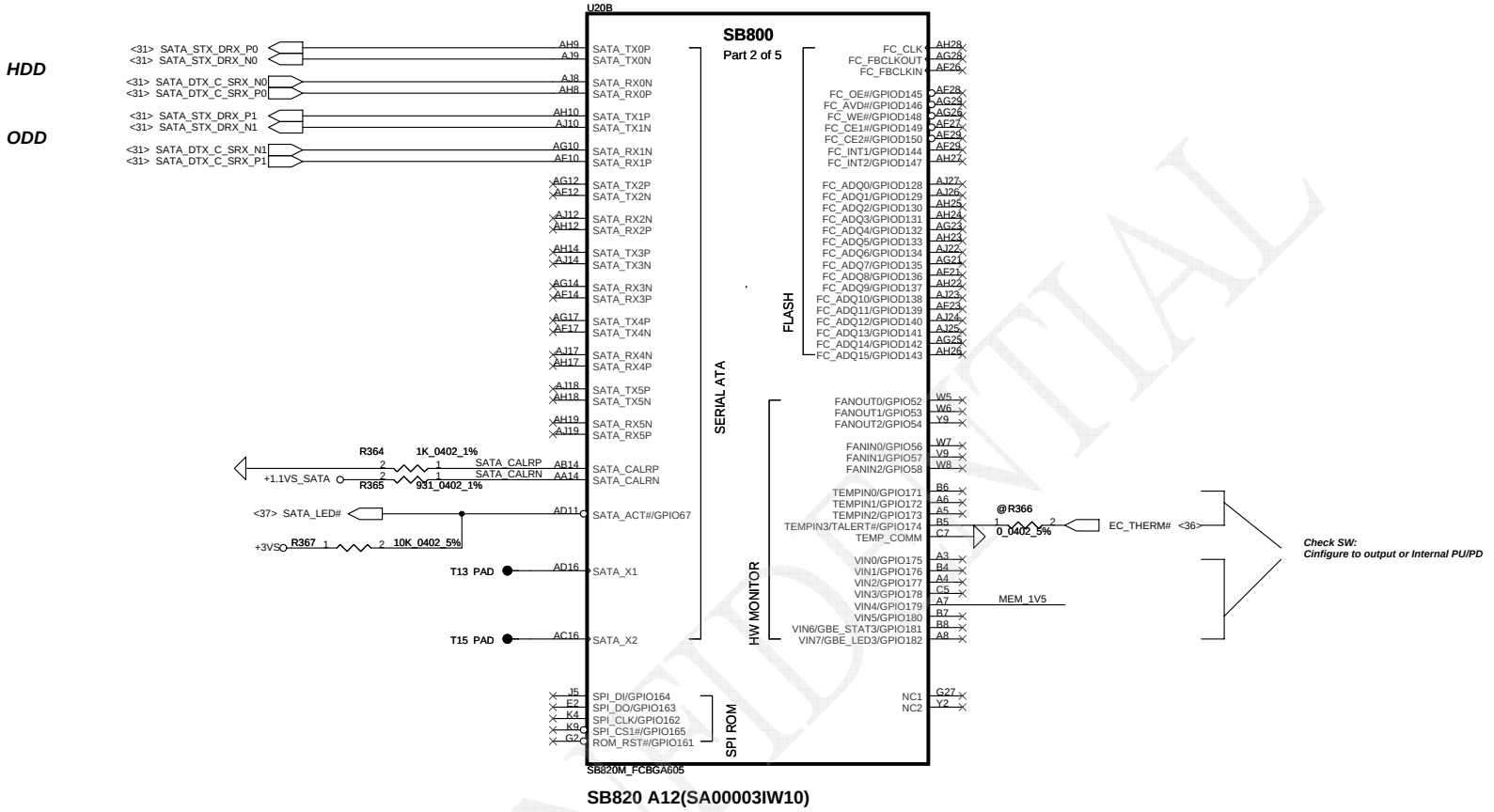
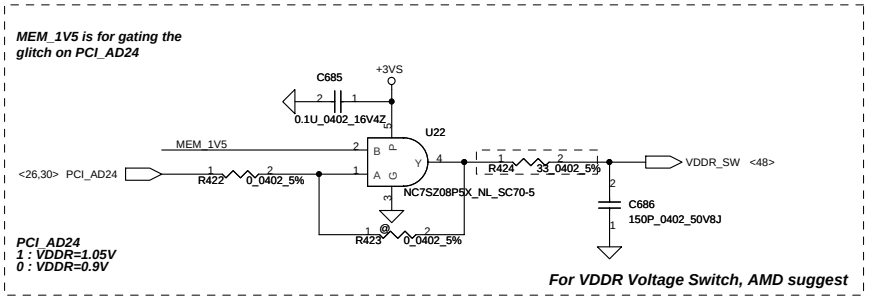


SB820 A12(SA00003IW10)



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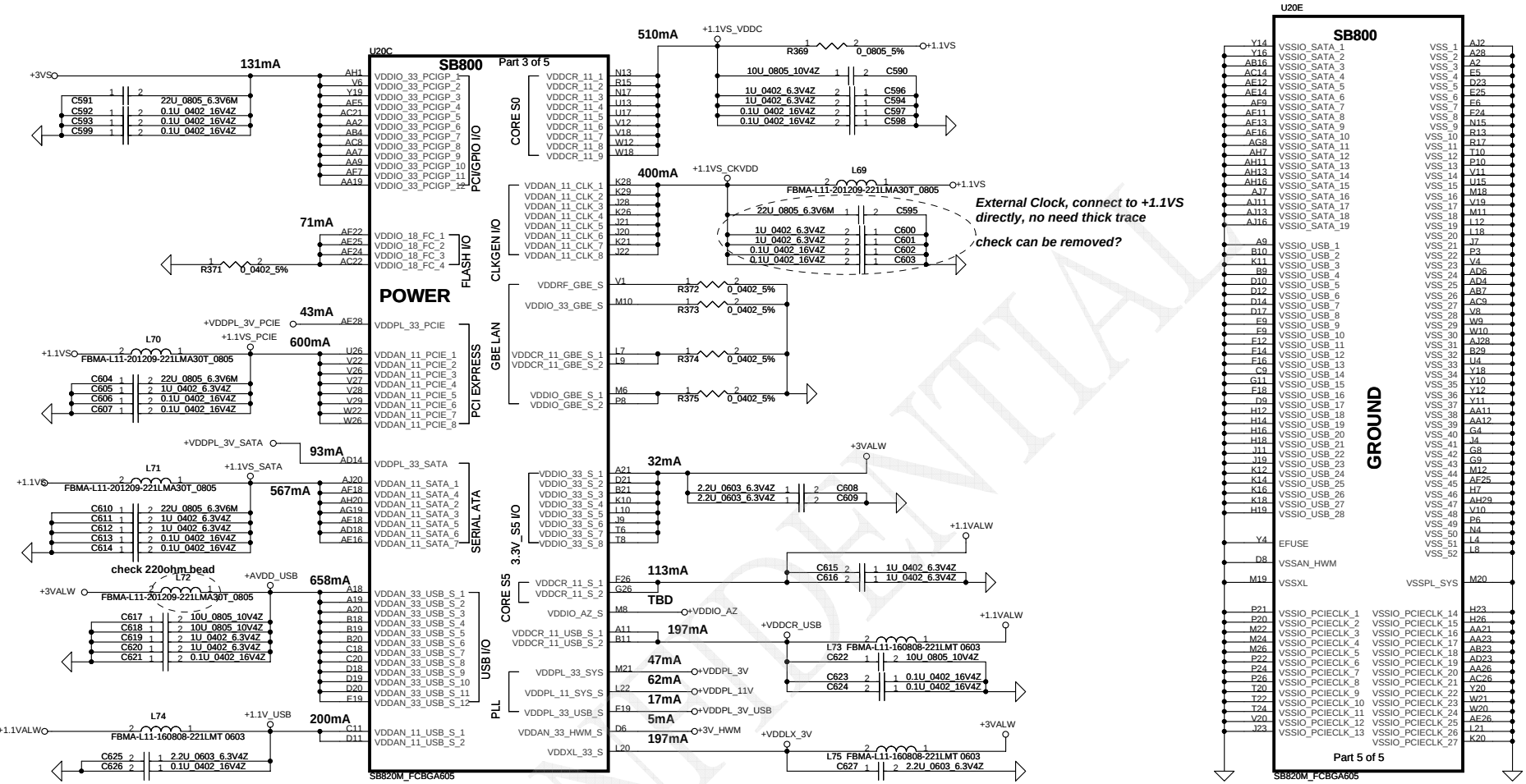

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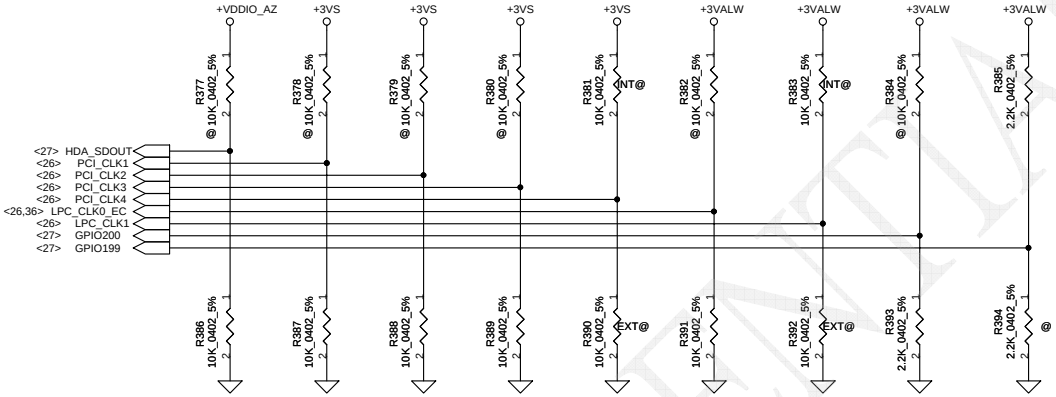
REQUIRED STRAPS

Check Internal PU/PD

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LCP_CLK1	GPIO200 GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE GEN2	WATCHDOG TIMER ENABLE	USE DEBUG STRAP	CPU/HT CLK SEL Enable	EC ENABLE	CLOCKGEN ENABLE	H,H = Reserved H,L = SPI ROM **L,H = LPC ROM (Default L,NC)** L,L = FWH ROM
PULL LOW	Performance MODE DEFAULT	FORCE PCIE GEN1 DEFAULT	WATCHDOG TIMER DISABLE DEFAULT	IGNORE DEBUG STRAP DEFAULT	CPU/HT CLK SEL Disable DEFAULT	EC DISABLE DEFAULT	CLOCKGEN DISABLE DEFAULT	



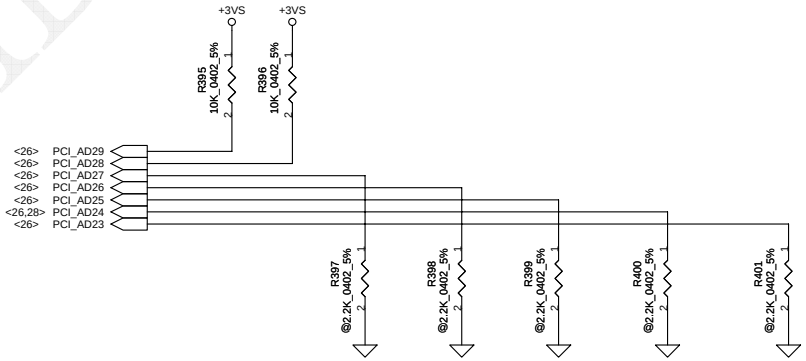
DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

		PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH		USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW		BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

Check AD29,AD28 strap function

check default



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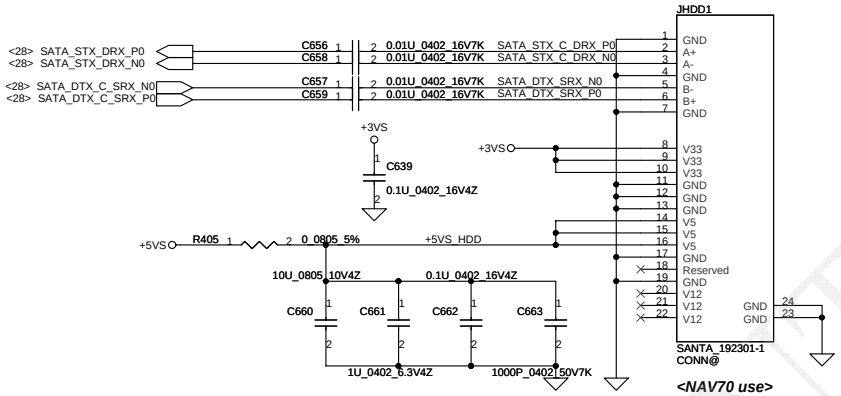
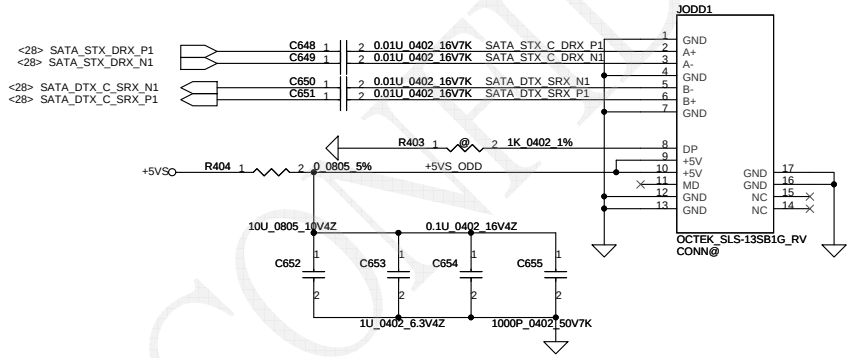
SATA HDD Conn.



SATA ODD Conn.



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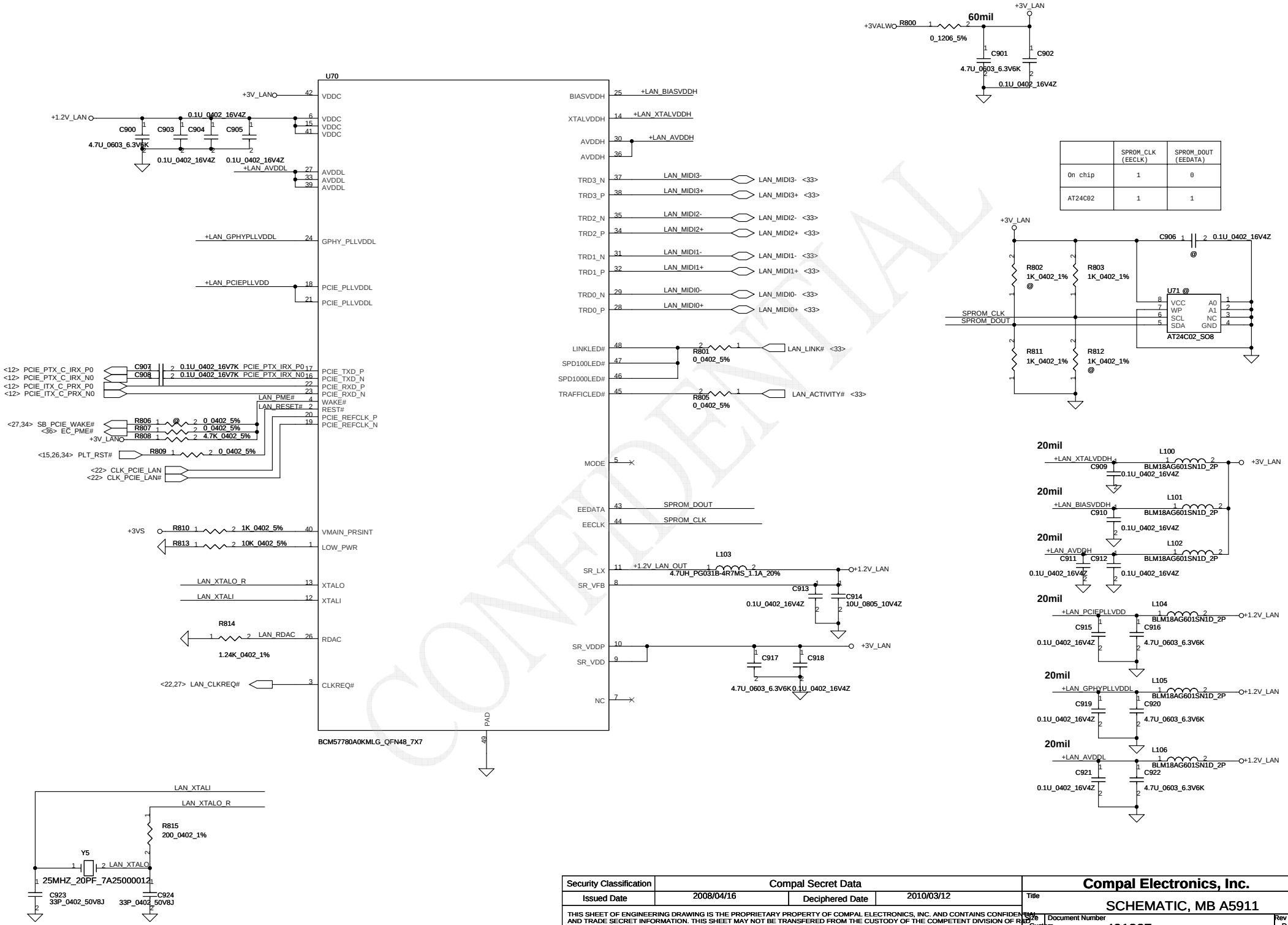

	SPROM_CLK (EECLK)	SPROM_DOUT (EEDATA)
On chip	1	0
AT24C02	1	1

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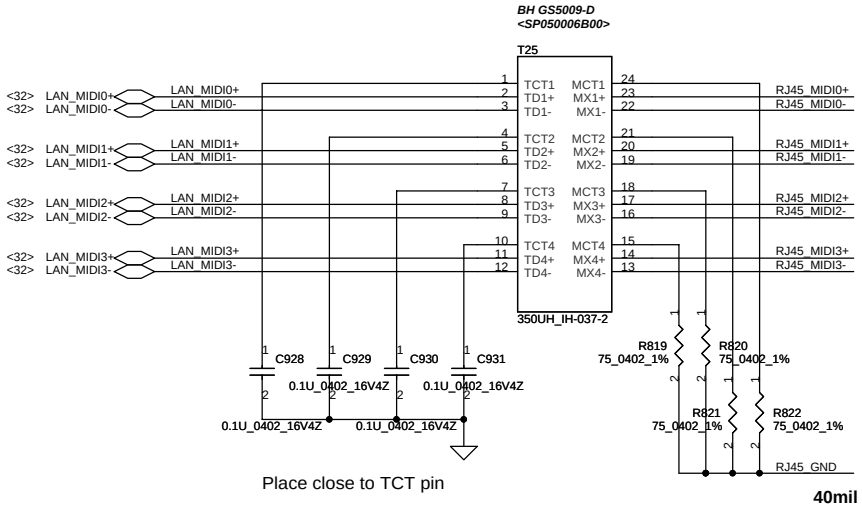
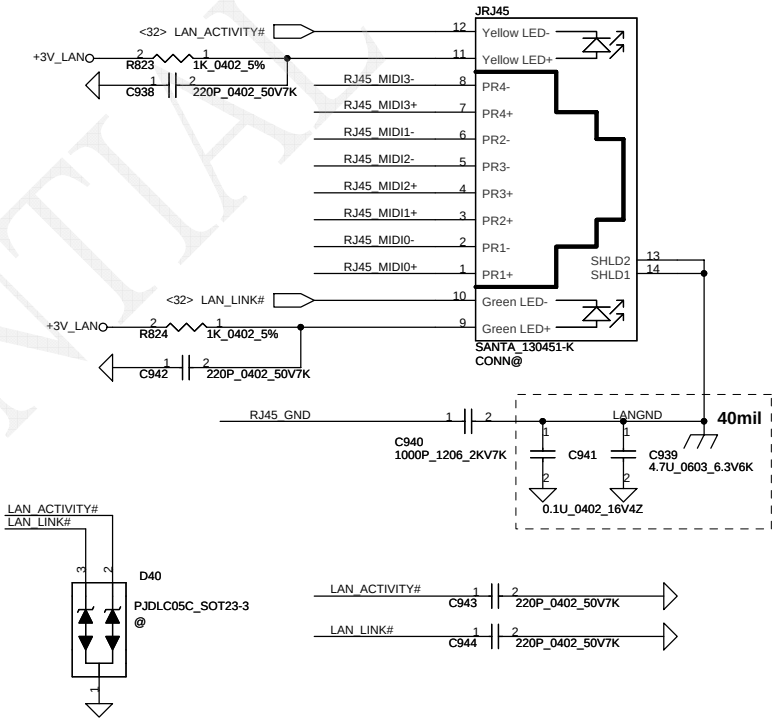


LAN Connector



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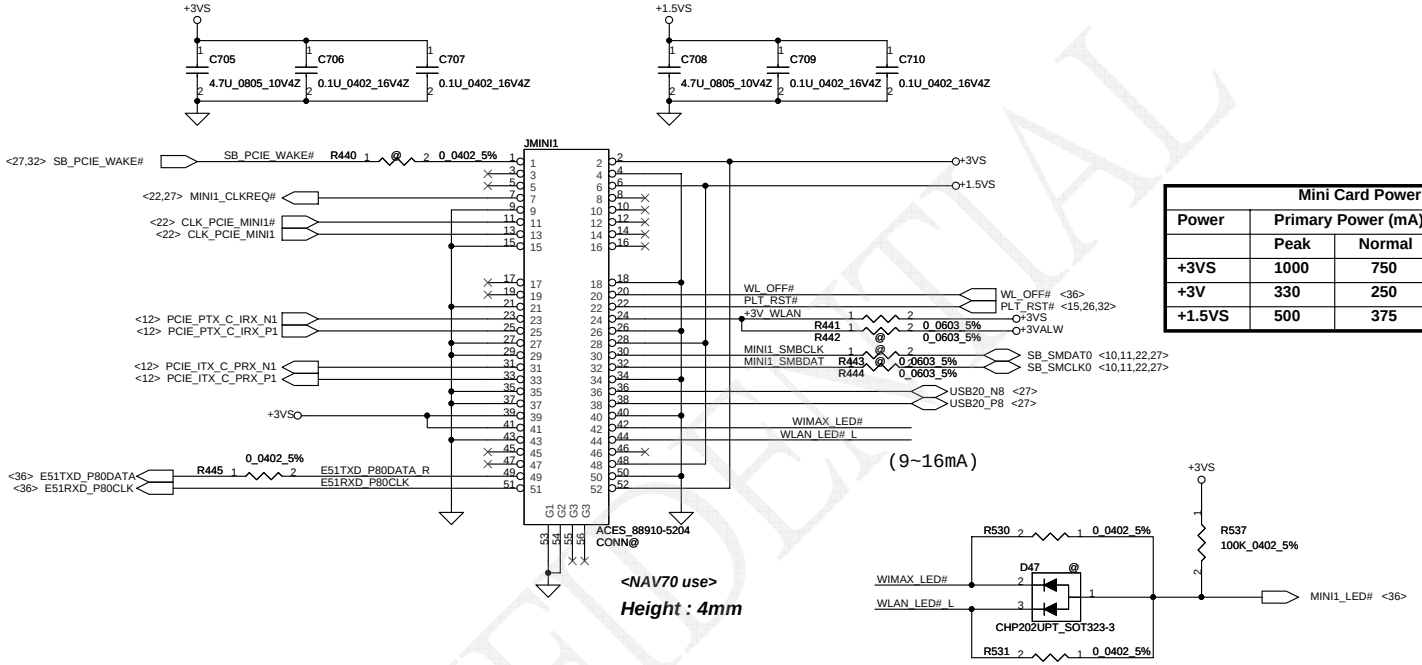
Mini-Express Card for WLAN



Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

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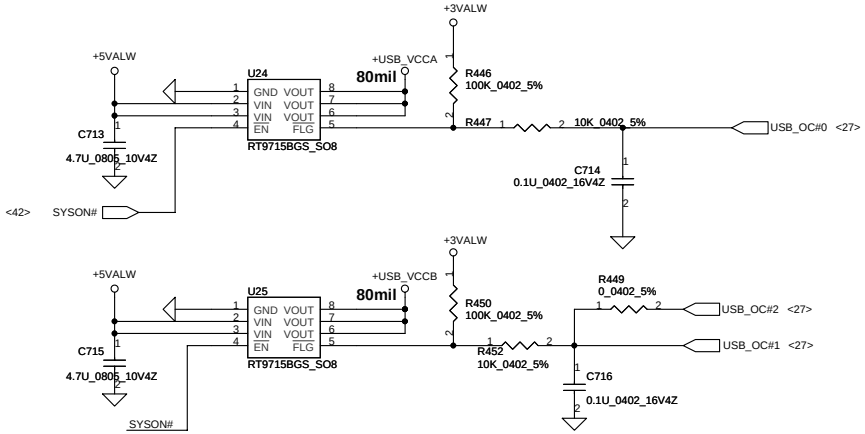
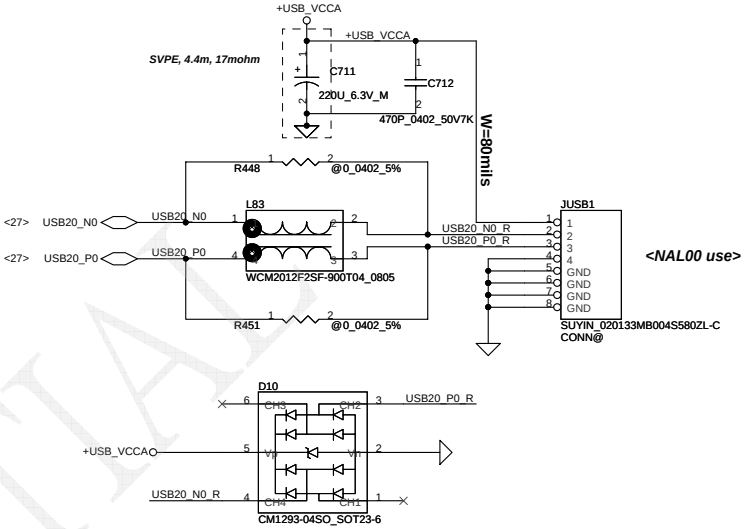
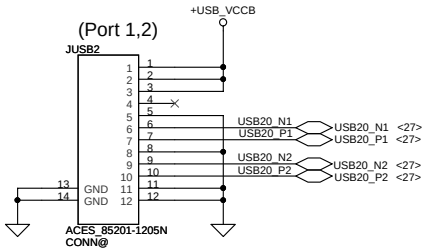




To USB/B Connector



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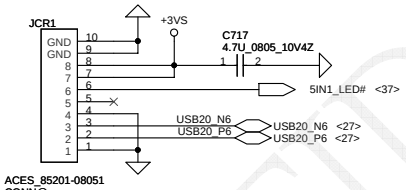
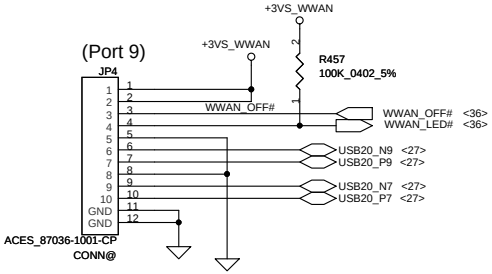
To CardReader/B Connector



<NEW70 use>

To 3G Module Connect



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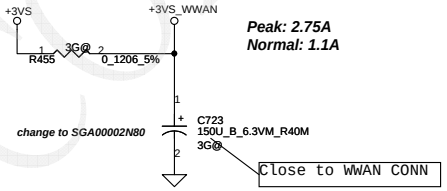
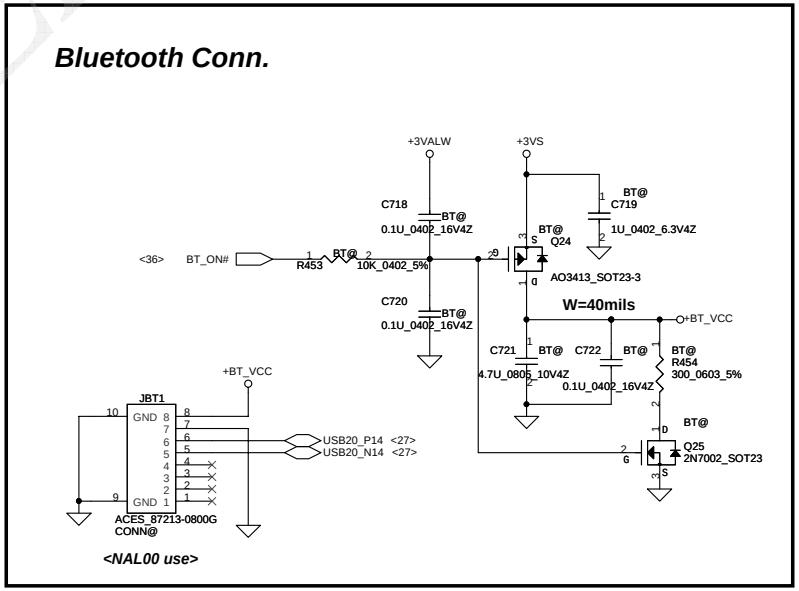


Bluetooth Conn.



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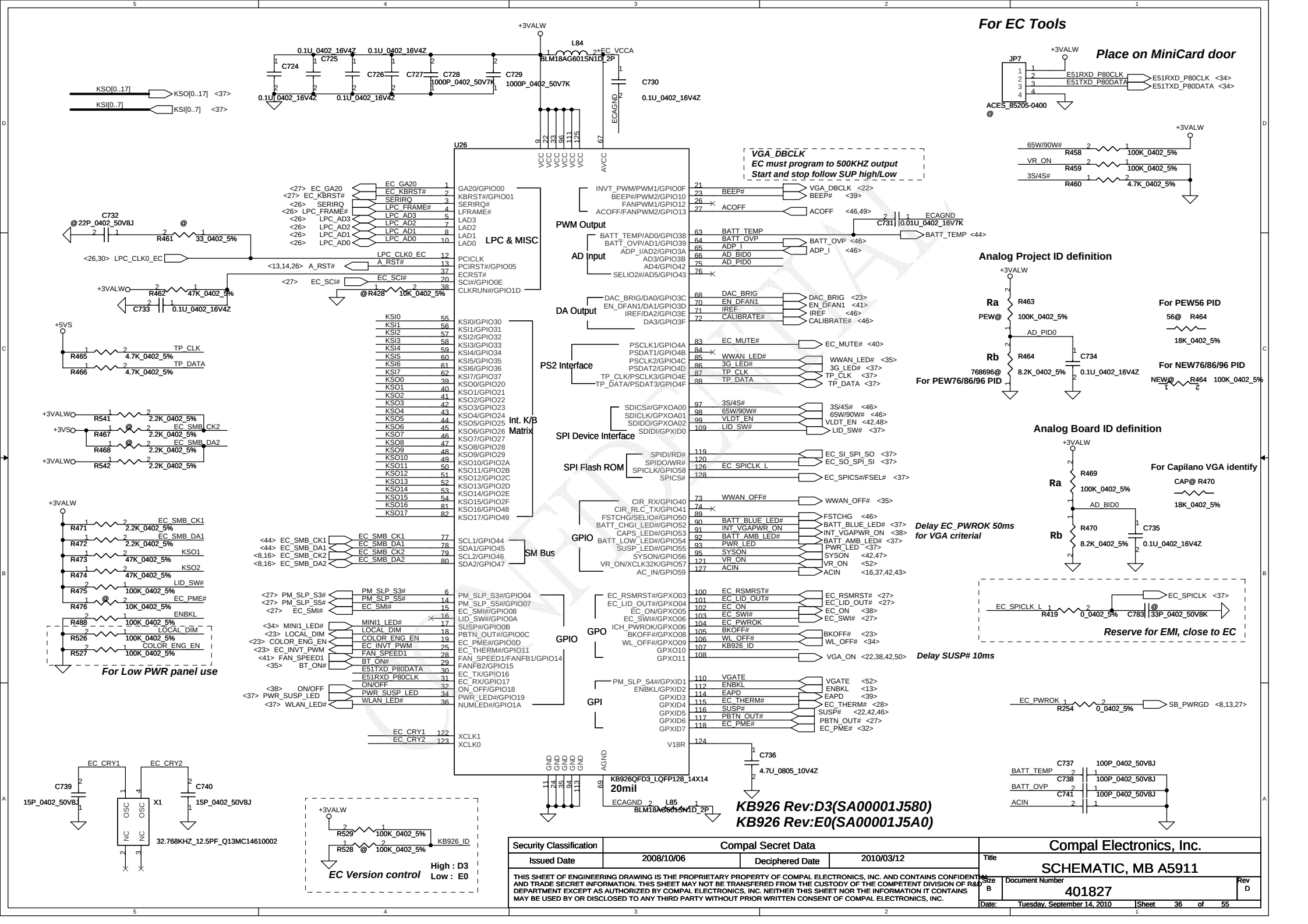
For EC Tools
Place on MiniCard door
JP7
ACES_85205-0400
E51RXD_P80CLK
E51TXD_P80DATA
U26
KB926QFD3_LQFP128_14X14
20mil
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
SPI Device Interface
SPI Flash ROM
Int. K/B Matrix
SM Bus
GPIO
GPO
GPI
VGA_DBCLK
EC must program to 500KHZ output
Start and stop follow SUP high/Low
Analog Project ID definition
For PEW56 PID
For NEW76/86/96 PID
For PEW76/86/96 PID
Analog Board ID definition
For Capilano VGA identify
Delay EC_PWROK 50ms for VGA criterial
Delay SUSP# 10ms
Reserve for EMI, close to EC
For Low PWR panel use
EC Version control
High : D3
Low : E0
KB926 Rev:D3(SA00001J580)
KB926 Rev:E0(SA00001J5A0)
32.768KHZ_12.5PF_Q13MC14610002
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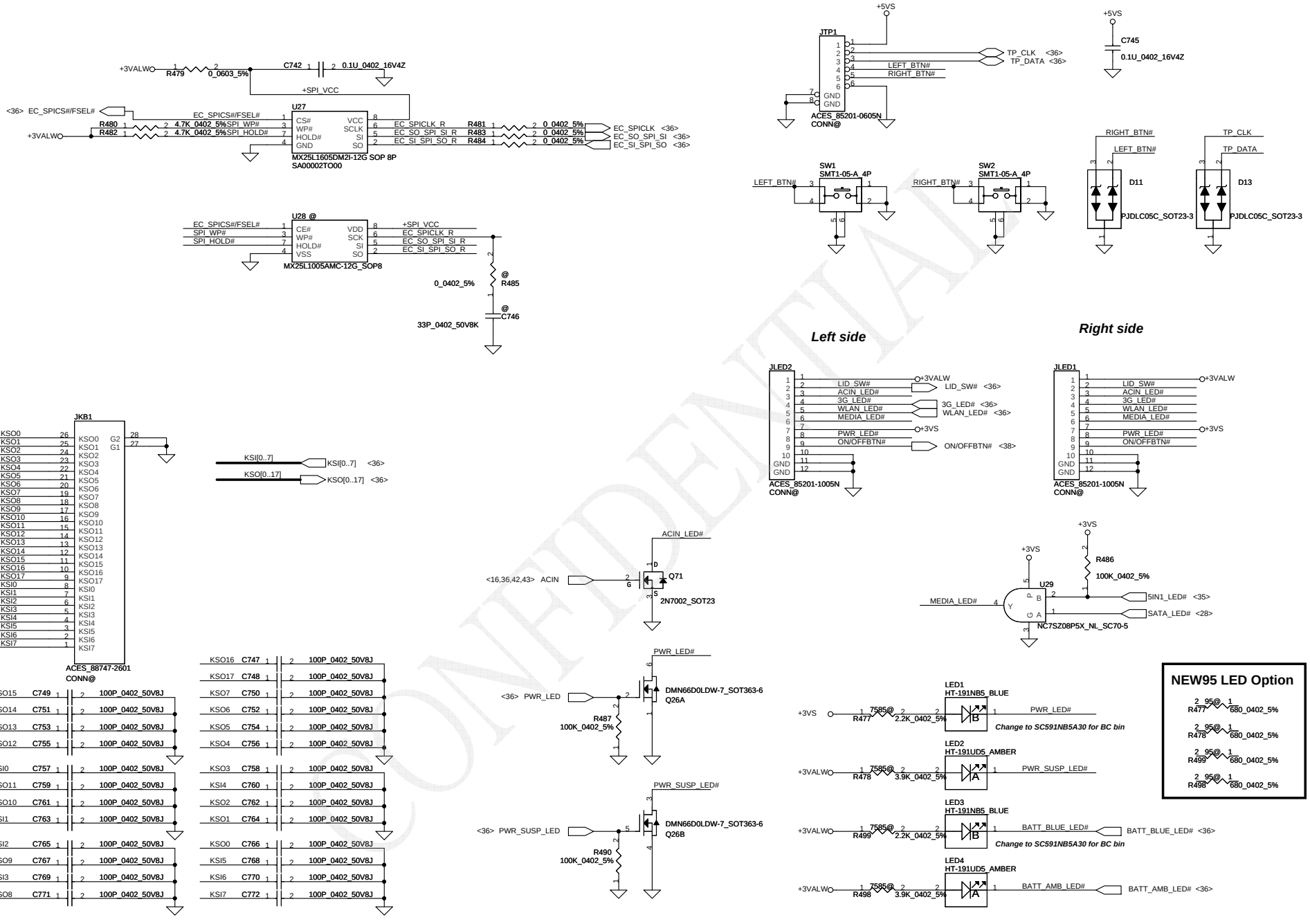

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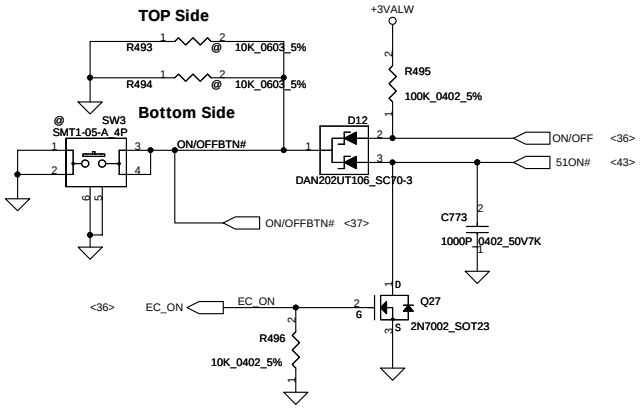
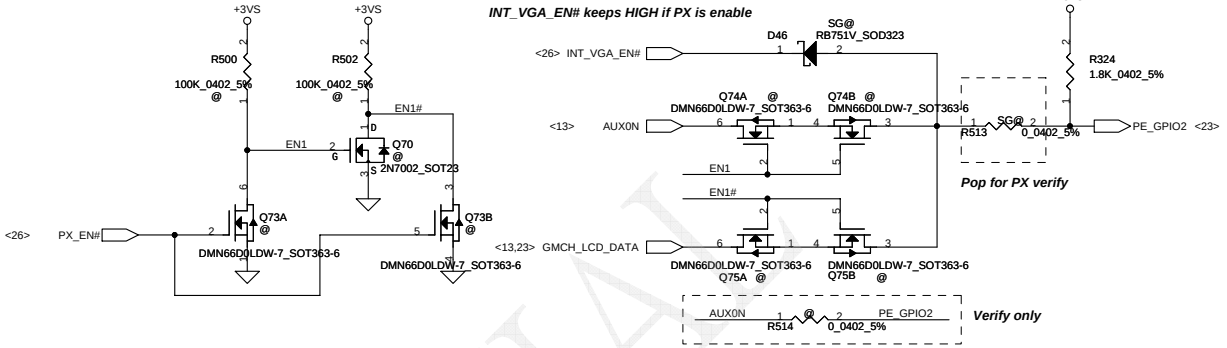
ON/OFF switch **Power Button**

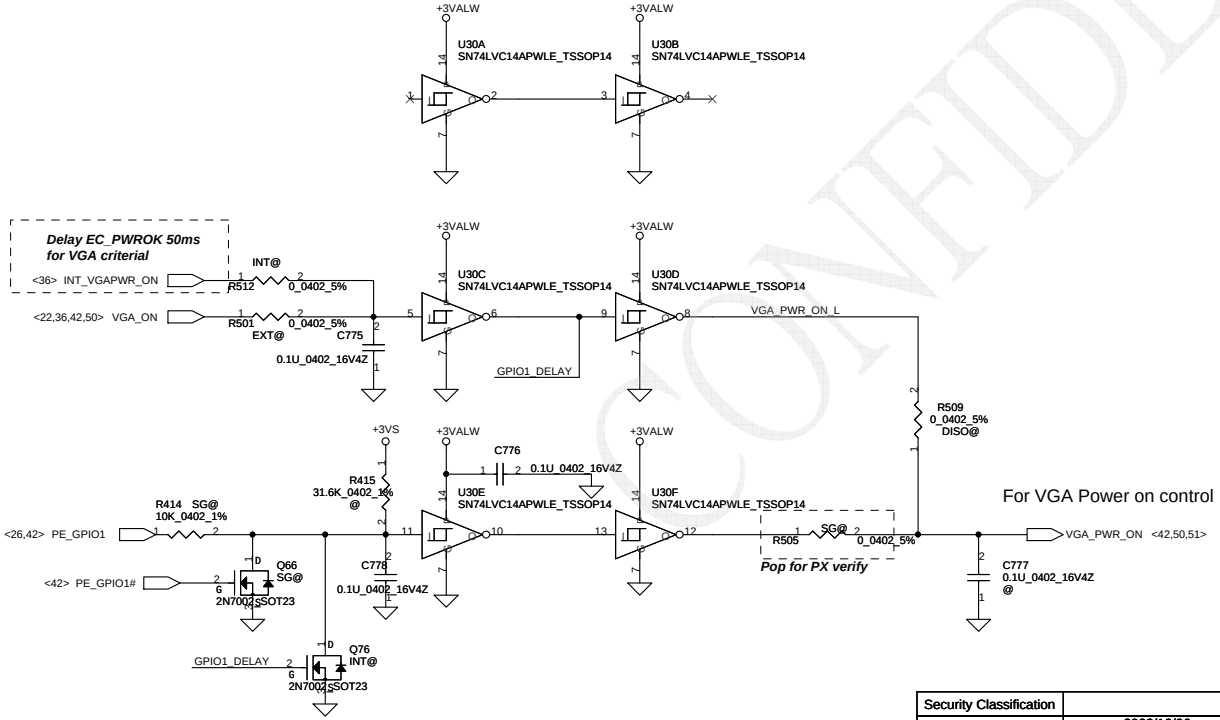


PX MODE SELECT CONTROL <AMD Suggestion>



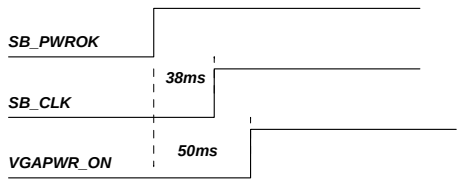
	PX_EN#	AUX0N EDP_DISABLED	I2C_DATA EDP_ENABLED	INT_VGA_EN#	DISPLAY OUTPUT
IGP only mode	1	X	X	0	IGP(LVDS,EDP,VGA,DP)
VGA only mode	1	X	X	1	VGA(LVDS,EDP,CRT,DP)
PX (MUXED)	0	0/1	0/1	1	VGA/IGP(CRT, LVDS, EDP); MXM(DP)
PX (MUXLESS)	0	X	X	0	IGP(LVDS,EDP,CRT,DP)

VGA Power ON Circuit

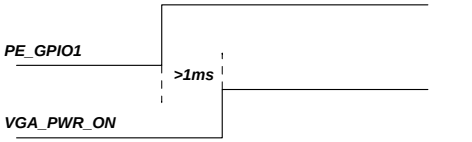


For VGA Power on control

For PX sequence and internal clock mode, VGA PWR need ramp up after SB_CLK oscillate



For PX sequence, >1mS delay is required between PE_GPIO1 and VGA_PWR_ON



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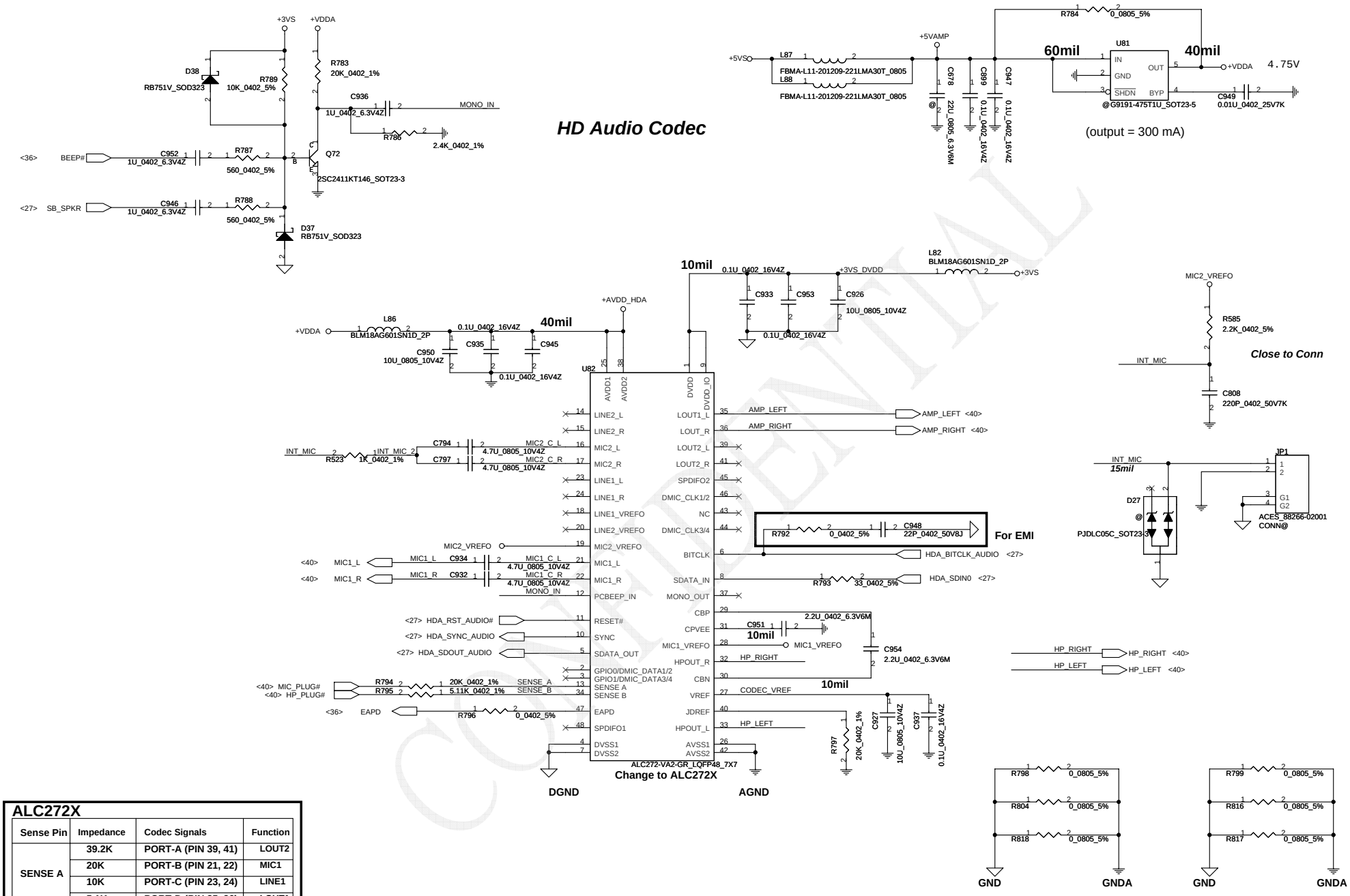

ALC272X

Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	LOUT2
	20K	PORT-B (PIN 21, 22)	MIC1
	10K	PORT-C (PIN 23, 24)	LINE1
	5.1K	PORT-D (PIN 35, 36)	LOUT1
SENSE B	39.2K	PORT-E (PIN 14, 15)	LINE2
	20K	PORT-F (PIN 16, 17)	MIC2
	10K		
	5.1K	PORT-I (PIN 32, 33)	HP

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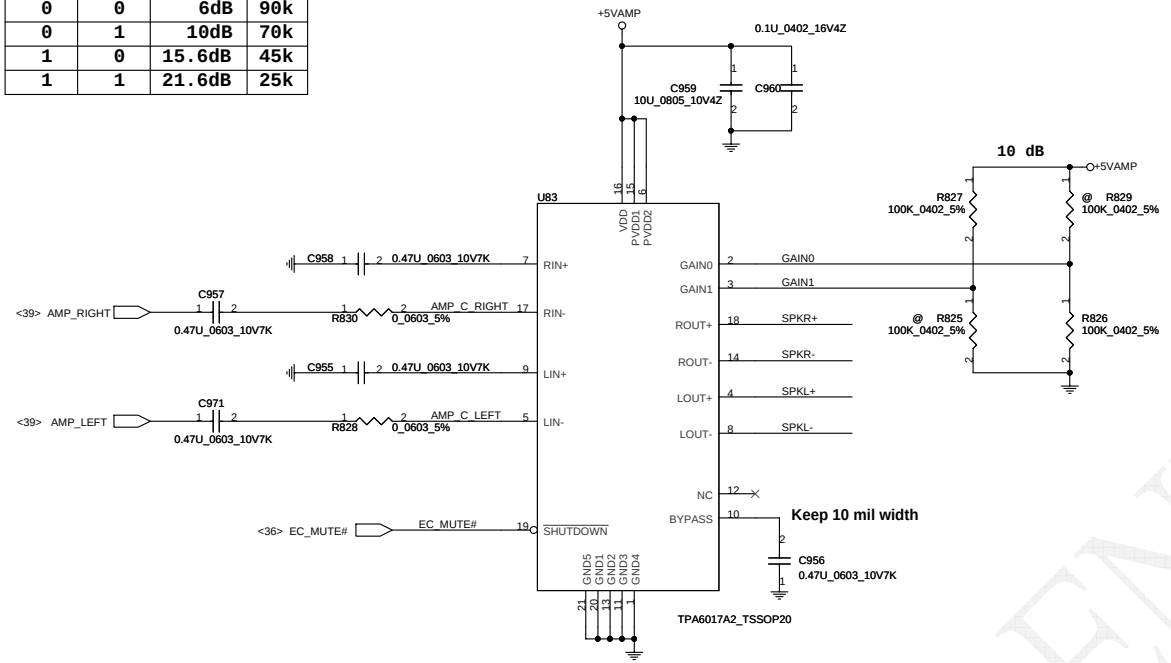
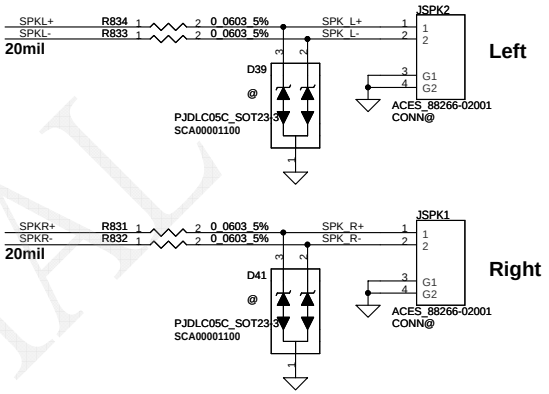
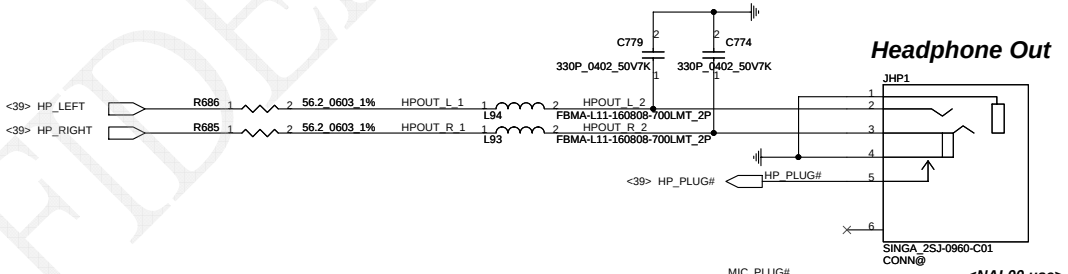
GAIN0	GAIN1	AV(inv)	Ri
0	0	6dB	90k
0	1	10dB	70k
1	0	15.6dB	45k
1	1	21.6dB	25k



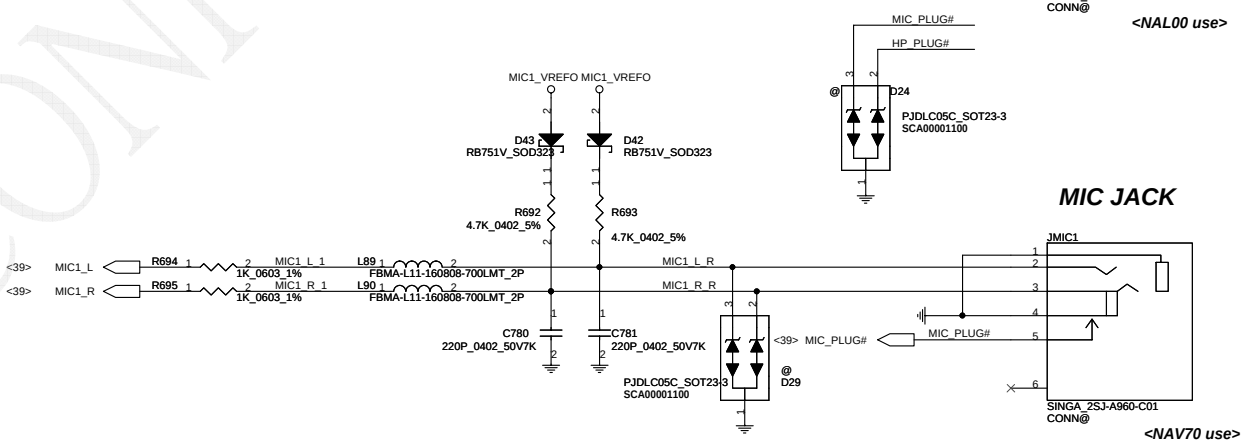
Int. Speaker Conn.



Headphone Out



<NAL00 use>



MIC JACK

<NAV70 use>

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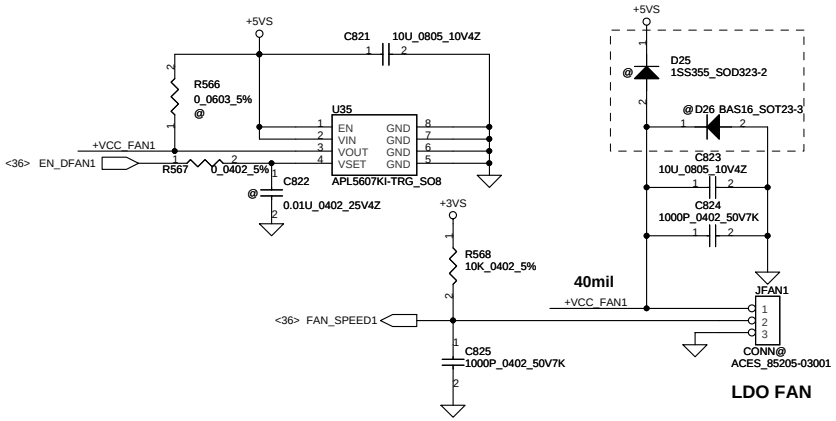
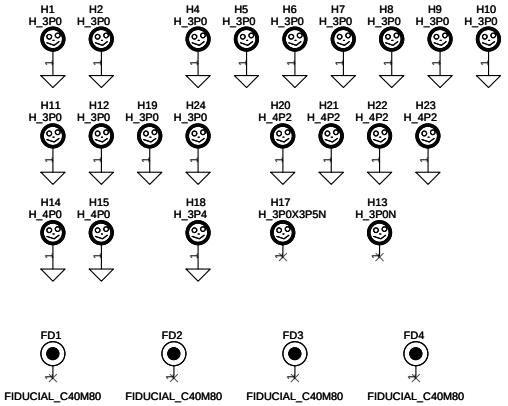
FAN1 Conn



LDO FAN



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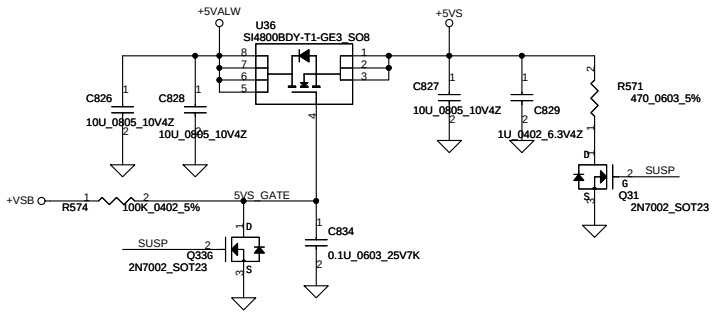
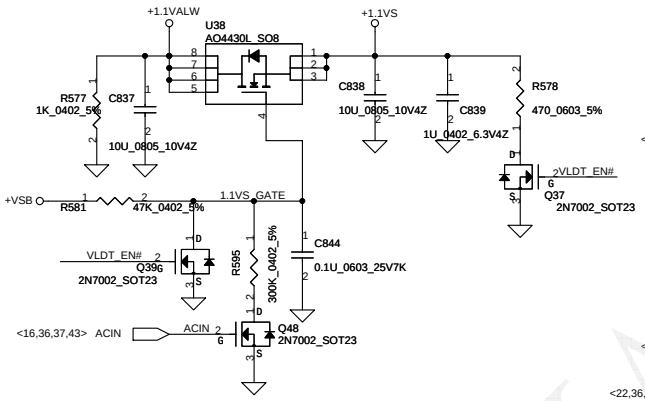
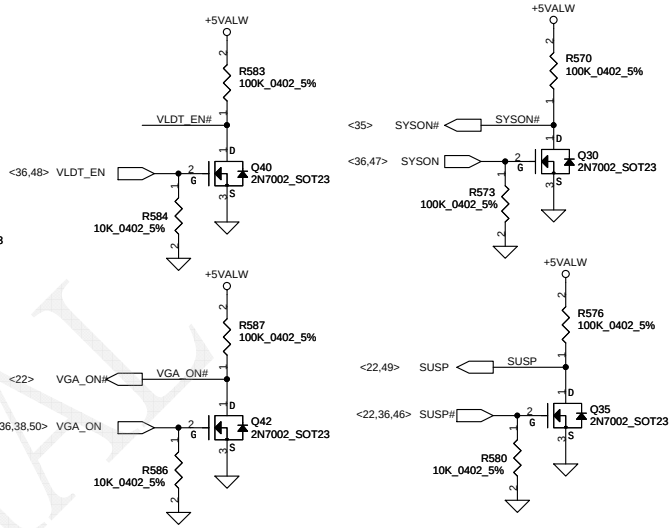
+5VALW TO +5VS

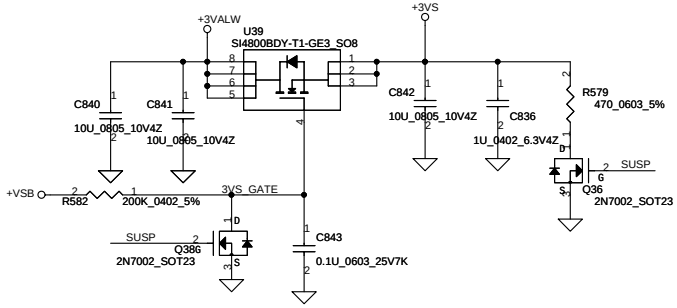


+1.1VALW TO +1.1VS

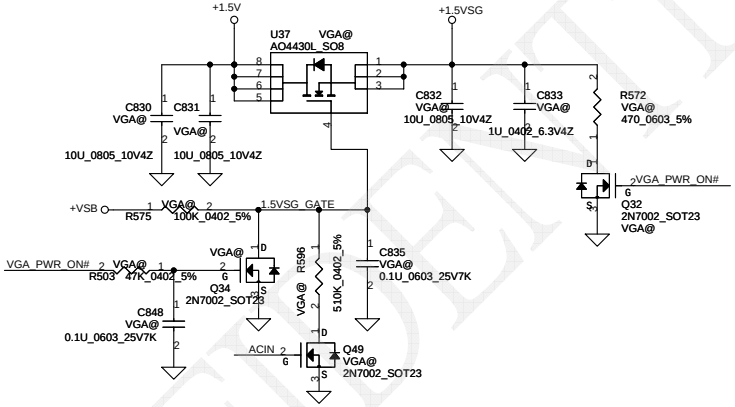


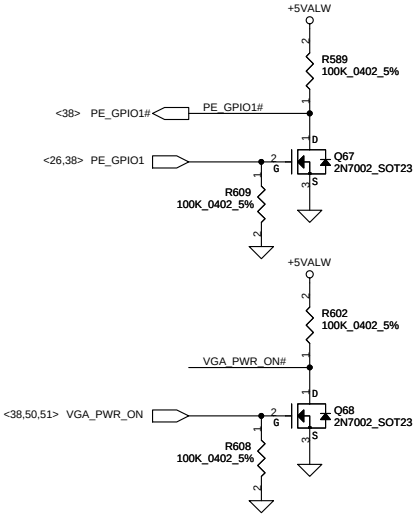


+3VALW TO +3VS

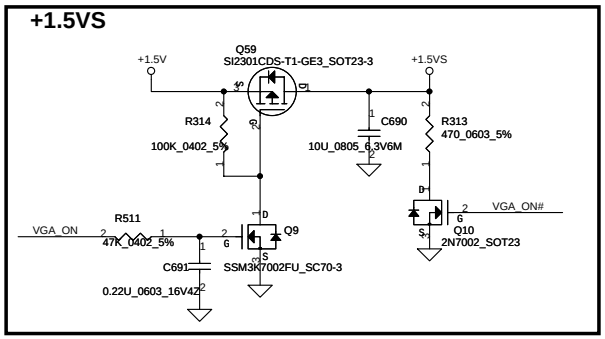


+1.5V to +1.5VSG

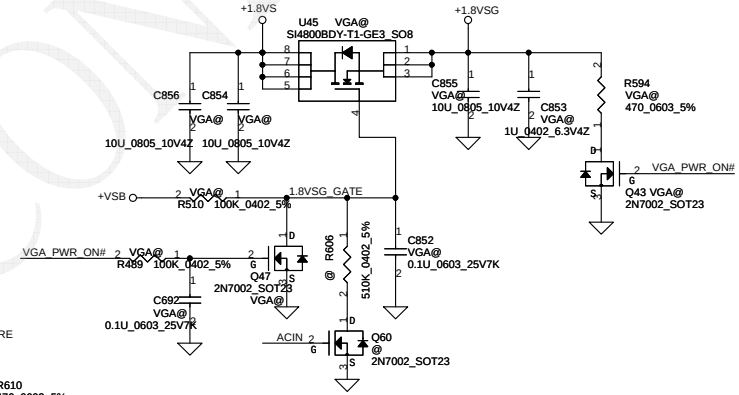




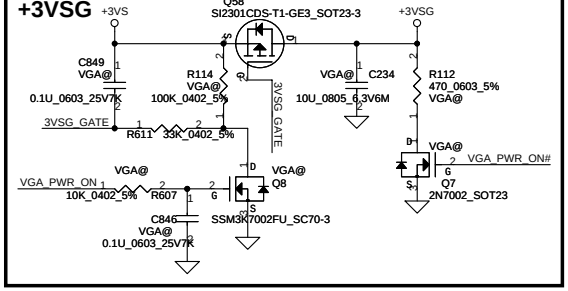
+1.5VS

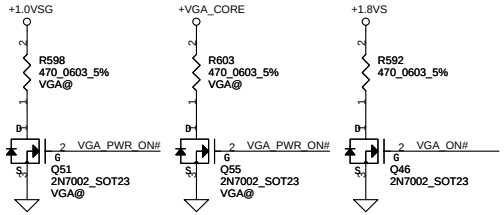


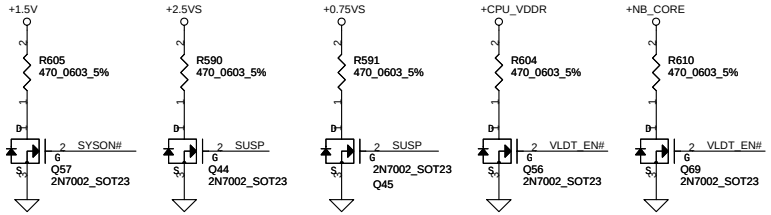
+1.8VS to +1.8VSG



+3VSG







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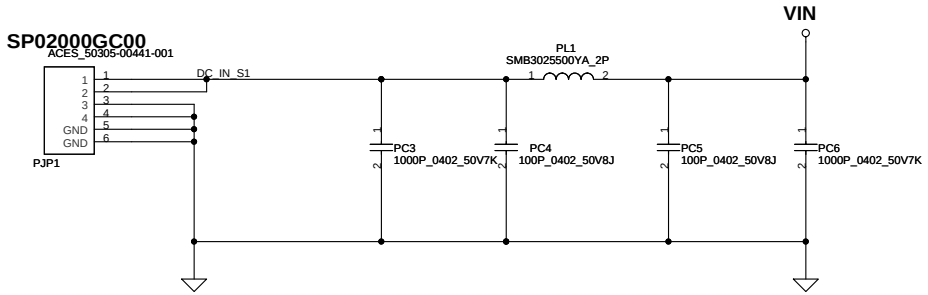
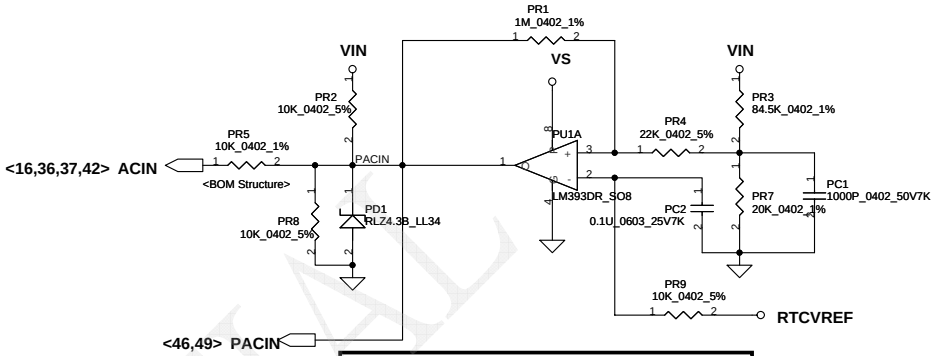
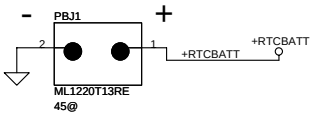
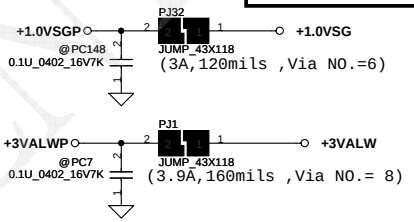


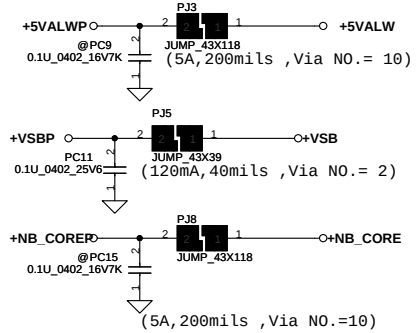


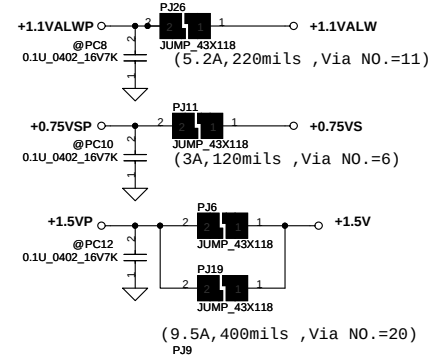
Vin Dectector

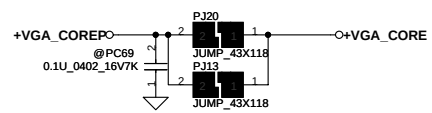
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V

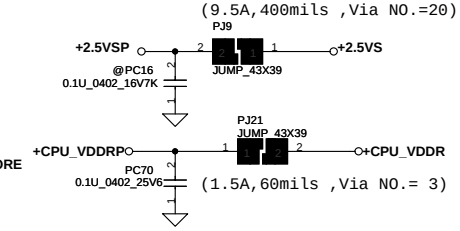


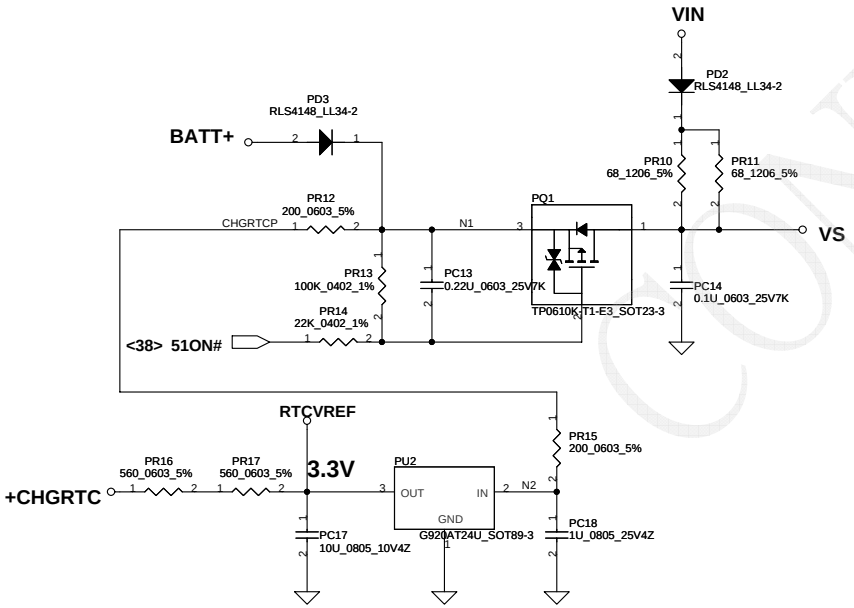












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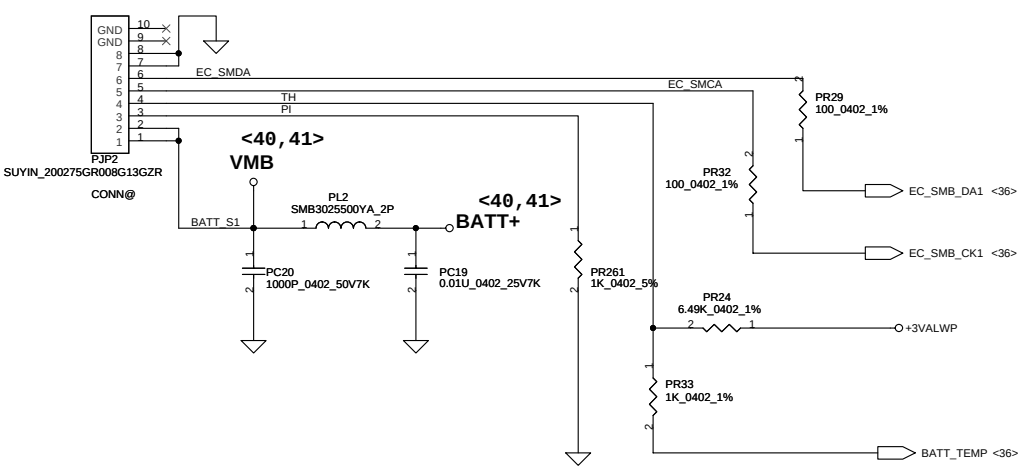
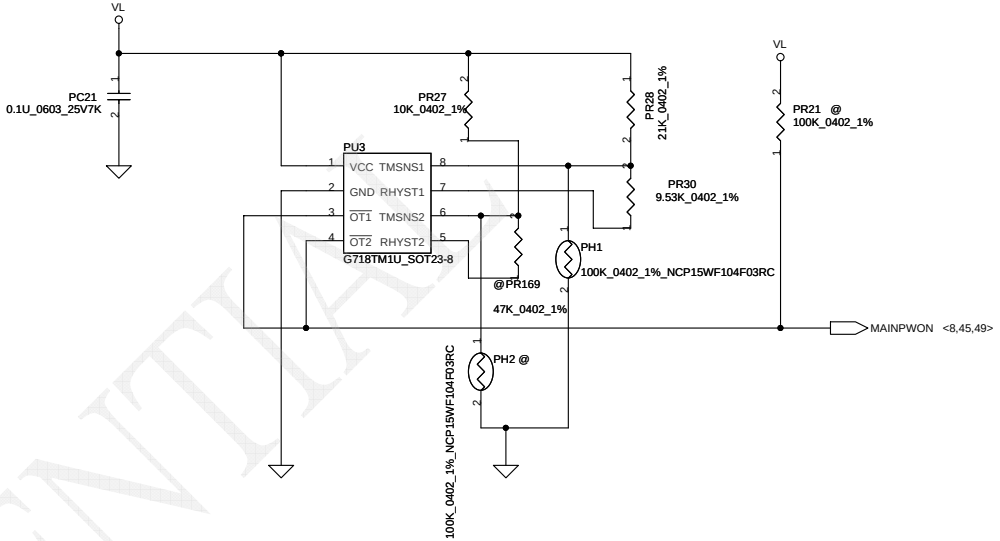
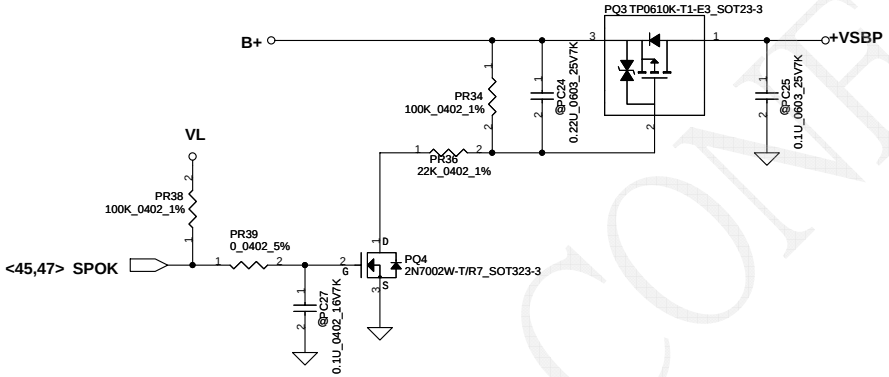
PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C







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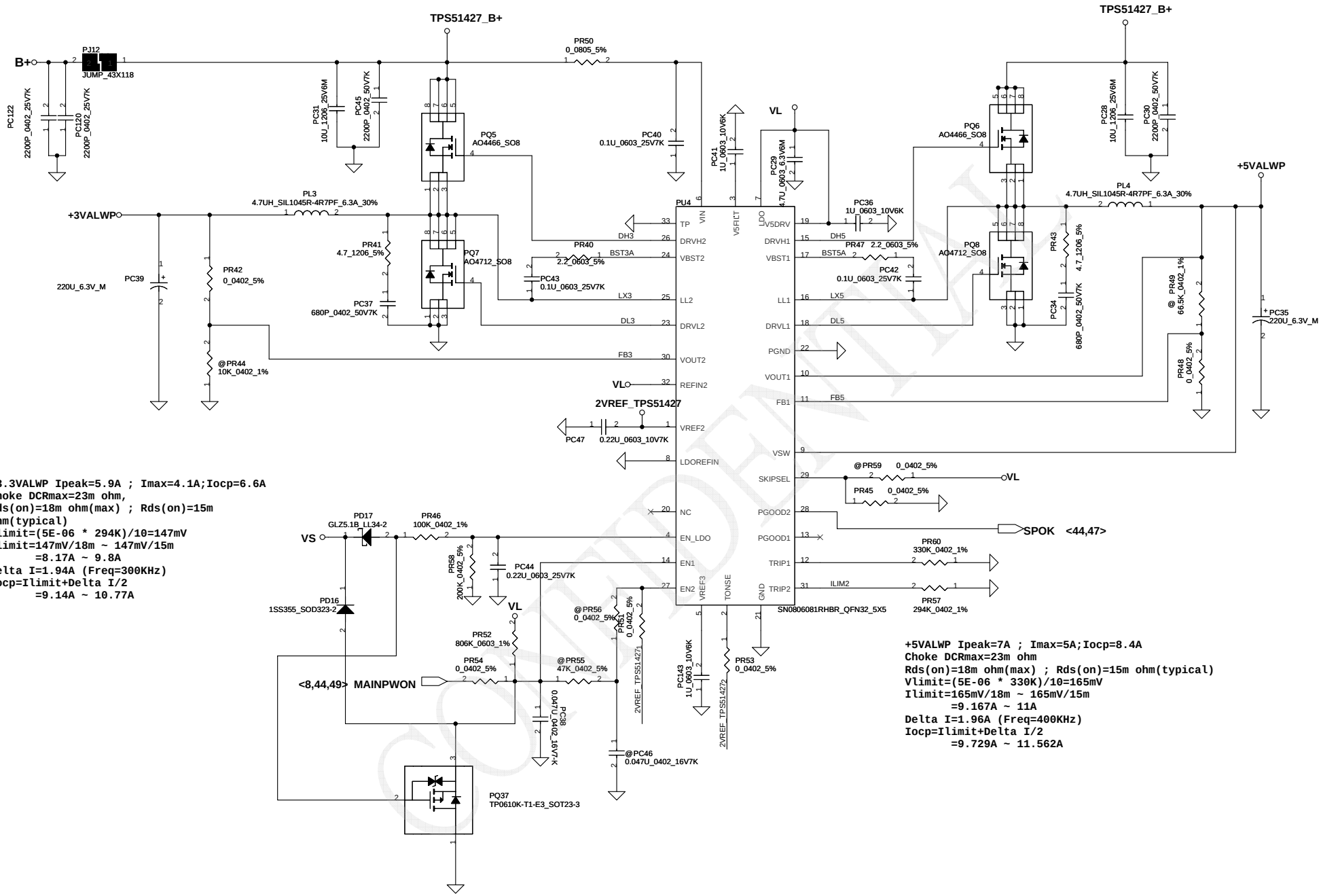

+3.3VALWP Ipeak=5.9A ; Imax=4.1A;Iocp=6.6A
Choke DCRmax=23m ohm,
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 294K)/10=147mV
Ilimit=147mV/18m ~ 147mV/15m
=8.17A ~ 9.8A
Delta I=1.94A (Freq=300KHz)
Iocp=Ilimit+Delta I/2
=9.14A ~ 10.77A

+5VALWP Ipeak=7A ; Imax=5A;Iocp=8.4A
Choke DCRmax=23m ohm
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Delta I=1.96A (Freq=400KHz)
Iocp=Ilimit+Delta I/2
=9.729A ~ 11.562A

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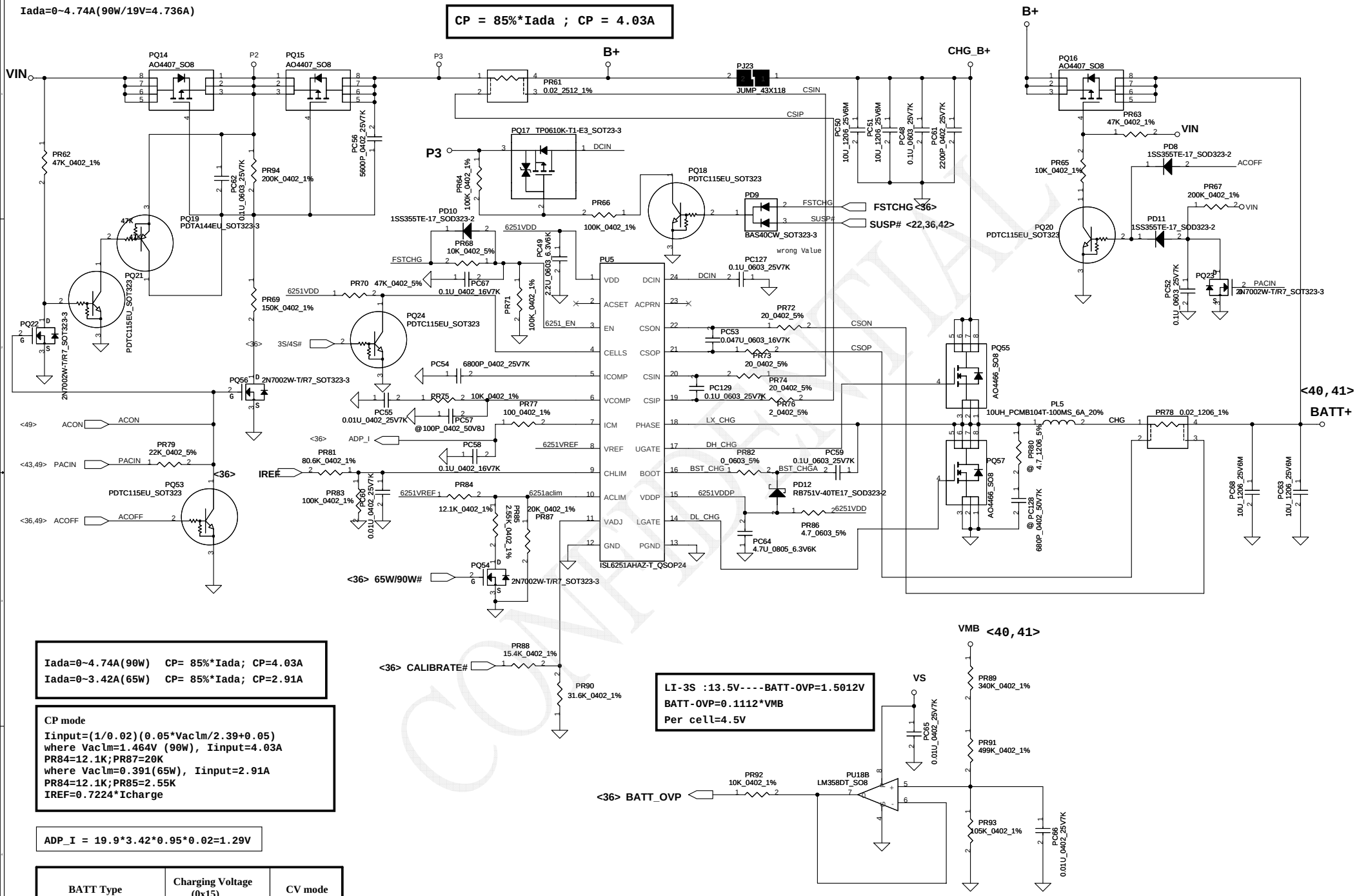
Iada=0~4.74A(90W/19V=4.736A)

CP = 85%*Iada ; CP = 4.03A



Iada=0~4.74A(90W) CP= 85%*Iada; CP=4.03A
Iada=0~3.42A(65W) CP= 85%*Iada; CP=2.91A

CP mode

Iinput=(1/0.02)(0.05*Vaclm/2.39+0.05)
where Vaclm=1.464V (90W), Iinput=4.03A
PR84=12.1K;PR87=20K
where Vaclm=0.391(65W), Iinput=2.91A
PR84=12.1K;PR85=2.55K
IREF=0.7224*Icharge

ADP_I = 19.9*3.42*0.95*0.02=1.29V

LI-3S :13.5V----BATT-OVP=1.5012V
BATT-OVP=0.1112*VMB
Per cell=4.5V

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

-

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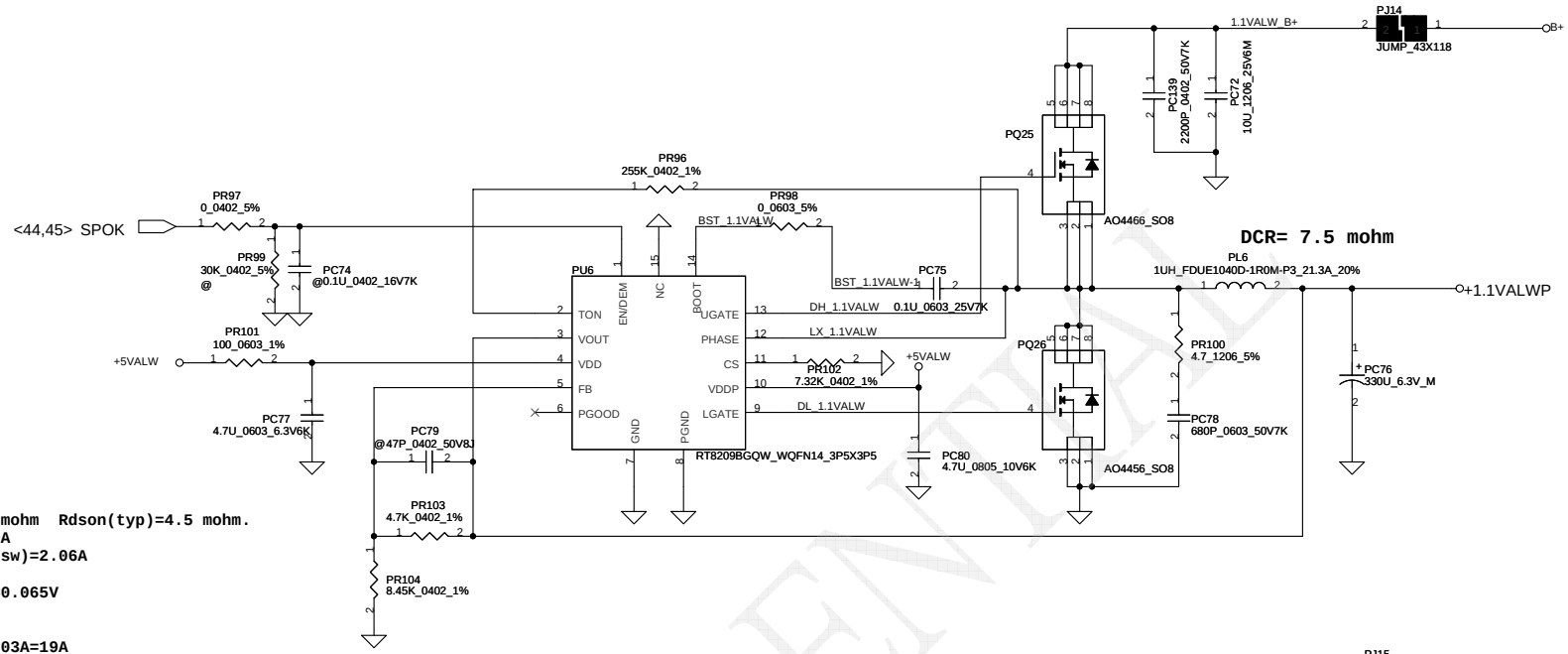
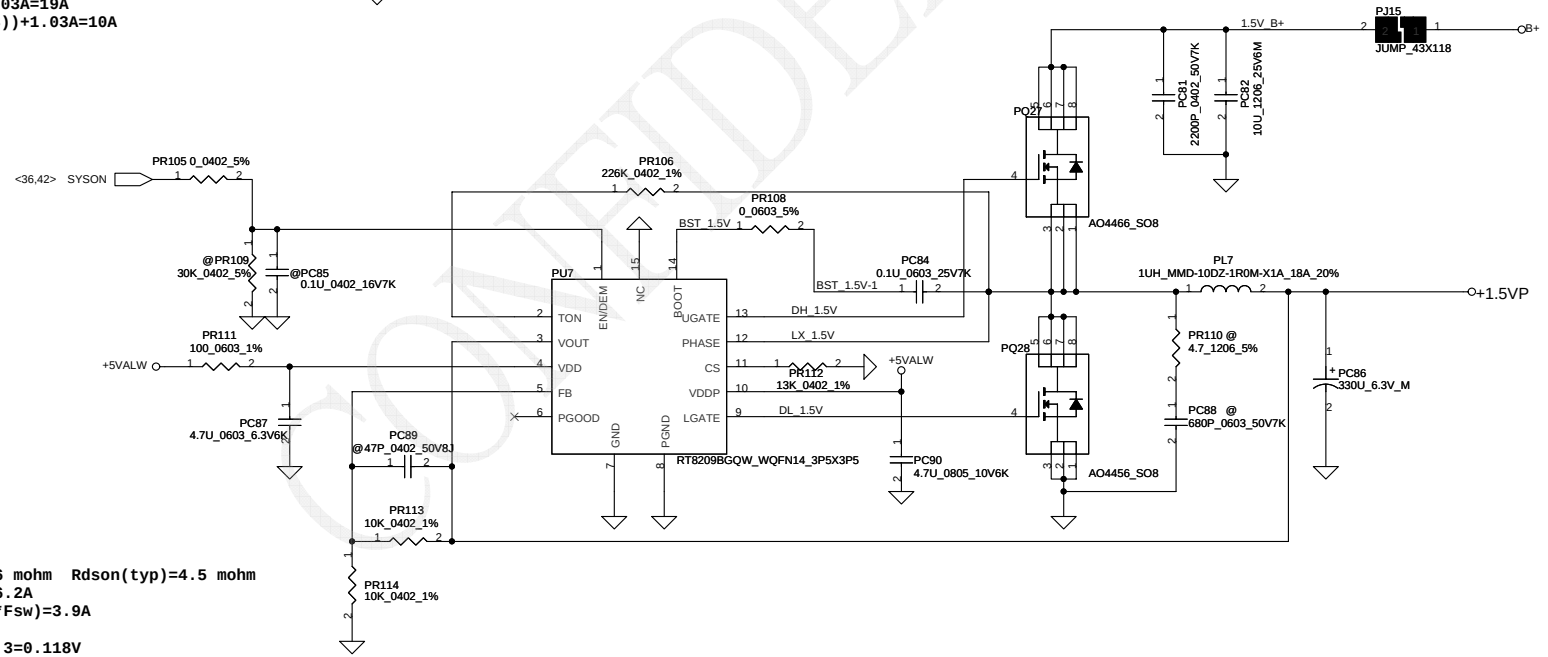


<Vo=1.1V> VFB=0.75V
V=0.75*(1+4.7K/10K)=1.1V
Fsw=280KHz

Cout ESR=15m ohm Rdson(max)=5.6 mohm Rdson(typ)=4.5 mohm.
Ipeak=7.42A, Imax=5.2A, Iocp=8.9A
Delta I=((19-1.1)*(1.1/19))/(L*Fsw)=2.06A
=>1/2Delta I=1.03A
Vtripmax=Iocp*Rdson=8.9*5.6*1.3=0.065V
Rcs=Vtrip/9uA=0.065V/9uA=7.2K
choose Rcs=7.32K
Iocpmax=((7.32K*11uA)/0.0045)+1.03A=19A
Iocpmin=((7.32K*9uA)/(0.0056*1.3))+1.03A=10A
Iocp=10A~19A



<Vo=1.5V> VFB=0.75V
Vo=0.75*(1+10K/10K)=1.5V
Fsw=280KHz

Cout ESR=17 mohm Rdson(max)=5.6 mohm Rdson(typ)=4.5 mohm
Ipeak=13.5A, Imax=9.5A, Iocp=16.2A
Delta I=((19-1.5)*(1.5/19))/(L*Fsw)=3.9A
=>1/2Delta I=1.95A
Vtripmax=Iocp*Rdson=16.2*5.6*1.3=0.118V
Rcs=Vtrip/9uA=0.118V/9uA=13.1K
choose Rcs=13K
Iocpmax=((13K*11uA)/0.0045)+1.95A=32A
Iocpmin=((13K*9uA)/(0.0056*1.3))+1.95A=18A
Iocp=18A~32A

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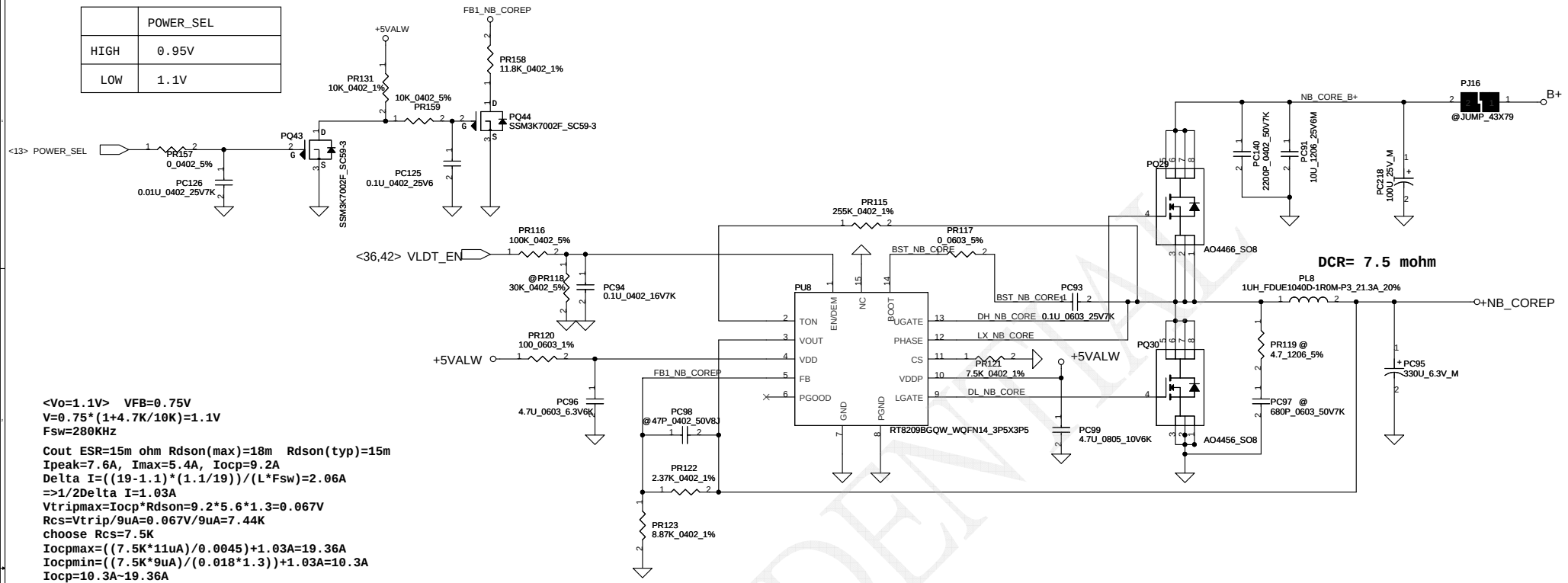
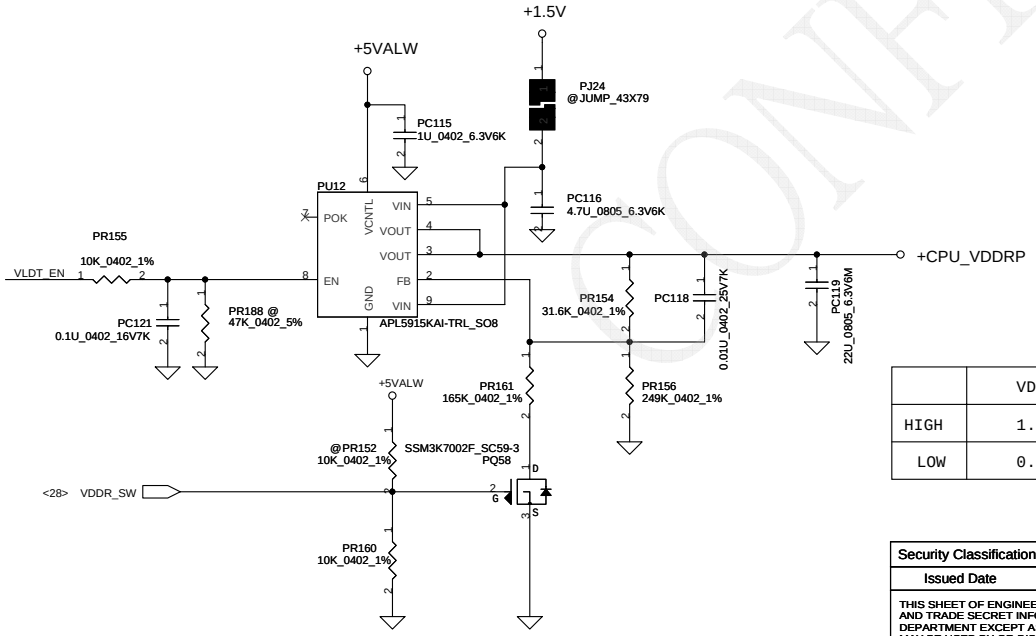
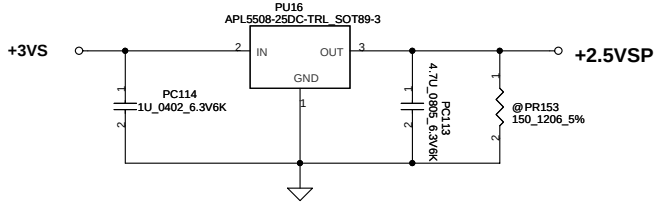
	POWER_SEL
HIGH	0.95V
LOW	1.1V



<Vo=1.1V> VFB=0.75V
V=0.75*(1+4.7K/10K)=1.1V
Fsw=280KHz

Cout ESR=15m ohm Rdson(max)=18m Rdson(typ)=15m
Ipeak=7.6A, Imax=5.4A, Iocp=9.2A
Delta I=((19-1.1)*(1.1/19))/(L*Fsw)=2.06A
=>1/2Delta I=1.03A
Vtripmax=Iocp*Rdson=9.2*5.6*1.3=0.067V
Rcs=Vtrip/9uA=0.067V/9uA=7.44K
choose Rcs=7.5K
Iocpmax=((7.5K*11uA)/0.0045)+1.03A=19.36A
Iocpmin=((7.5K*9uA)/(0.018*1.3))+1.03A=10.3A
Iocp=10.3A~19.36A





	VDDR_SW
HIGH	1.05V
LOW	0.9V

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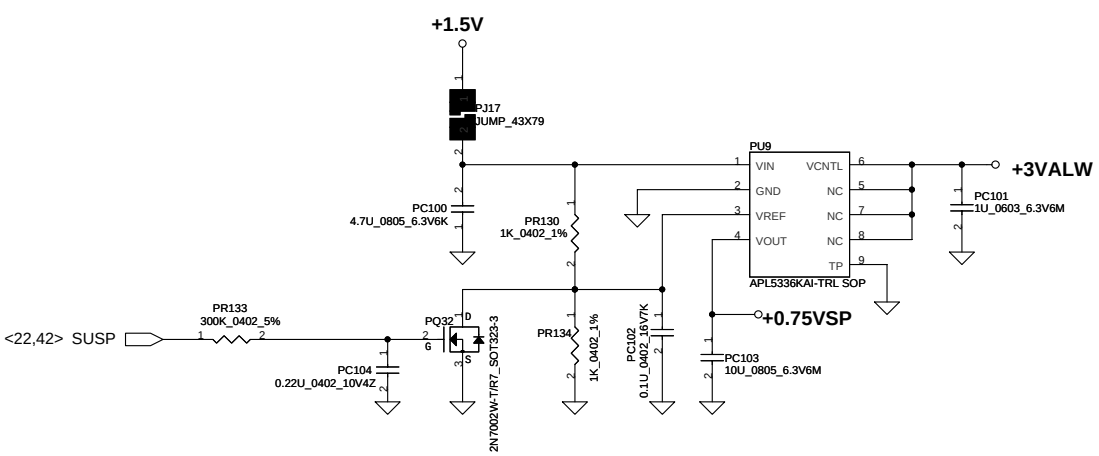
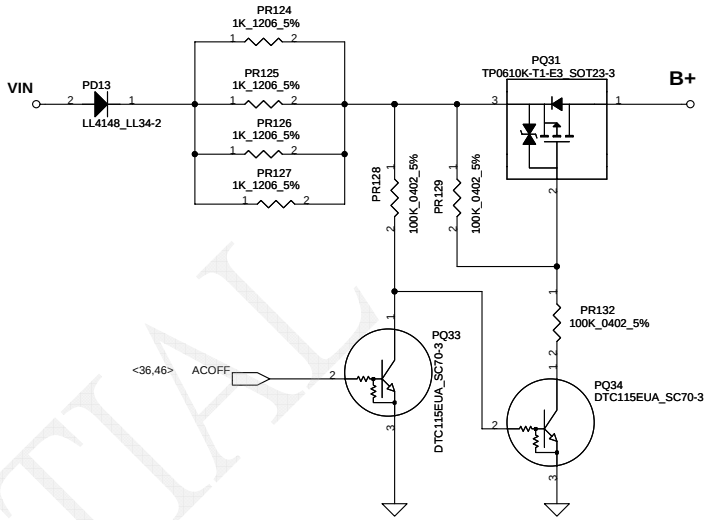
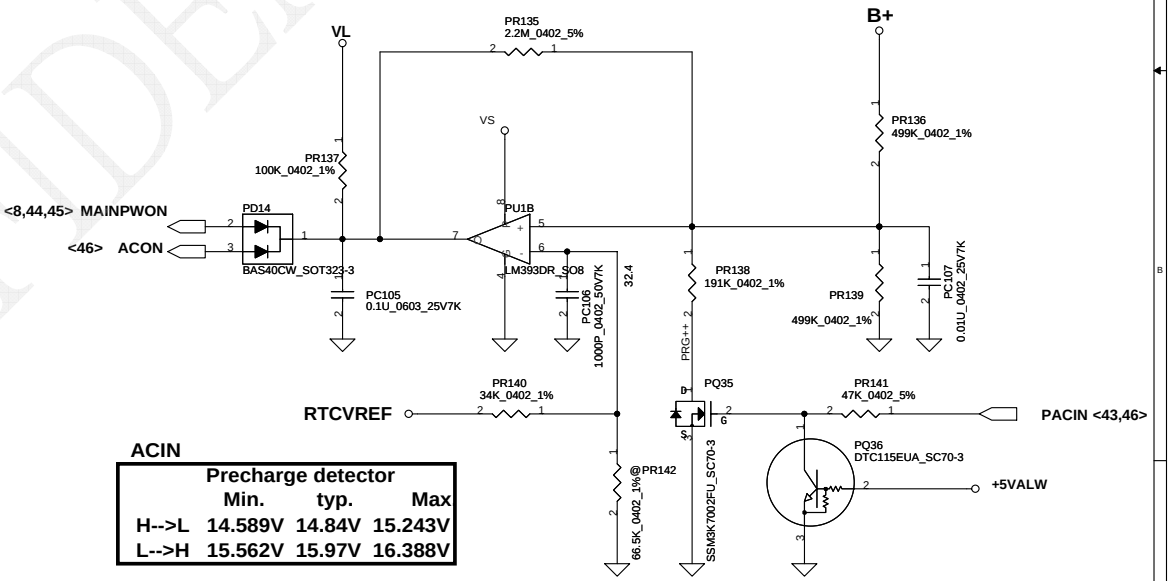


Ipeak=1A, Imax=0.7A





ACIN

Precharge detector	Min.	typ.	Max
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector	Min.	typ.	Max
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

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Title	SCHEMATIC, MB A5911		
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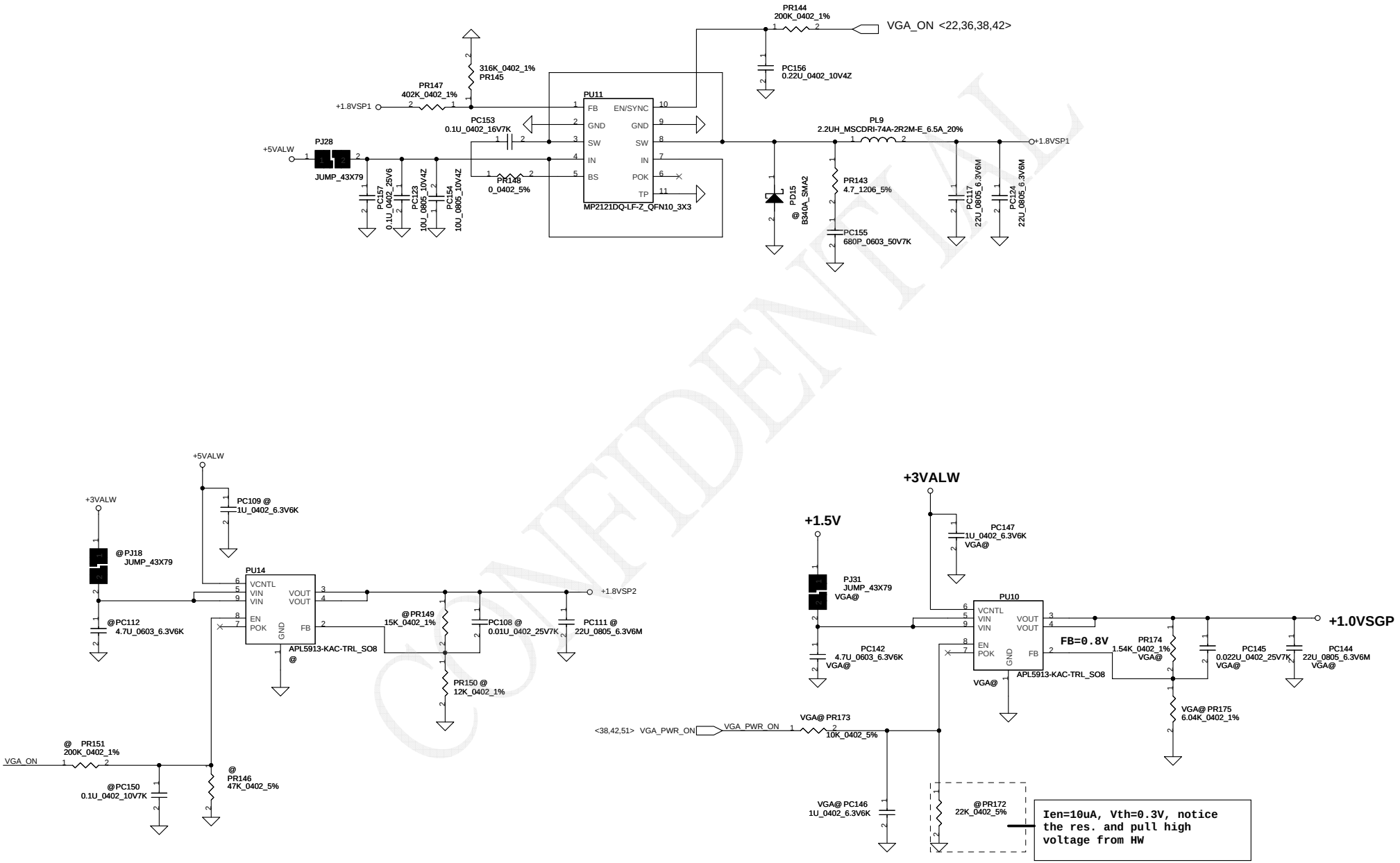

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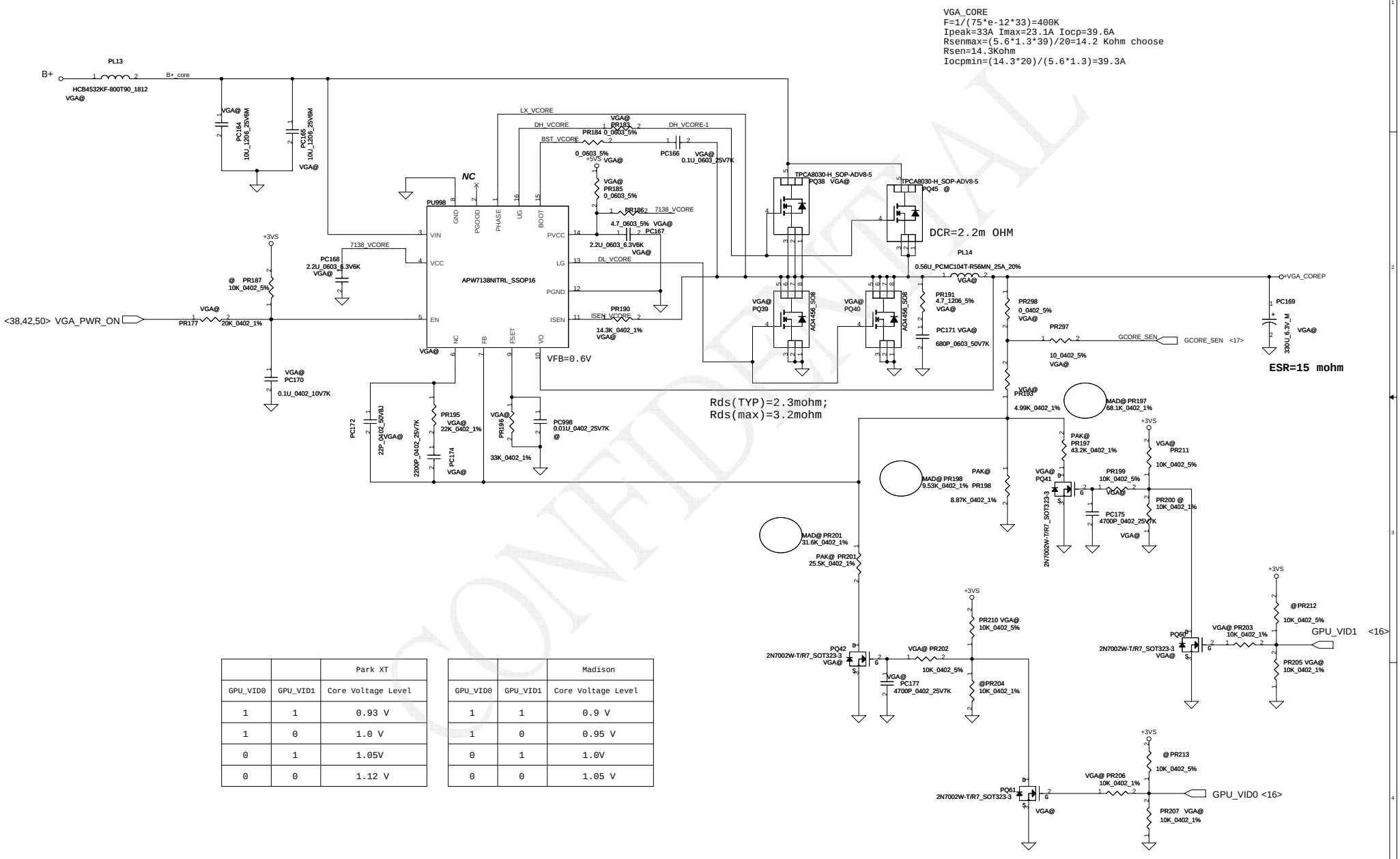

		Park XT
GPU_VID0	GPU_VID1	Core Voltage Level
1	1	0.93 V
1	0	1.0 V
0	1	1.05V
0	0	1.12 V

		Madison
GPU_VID0	GPU_VID1	Core Voltage Level
1	1	0.9 V
1	0	0.95 V
0	1	1.0V
0	0	1.05 V

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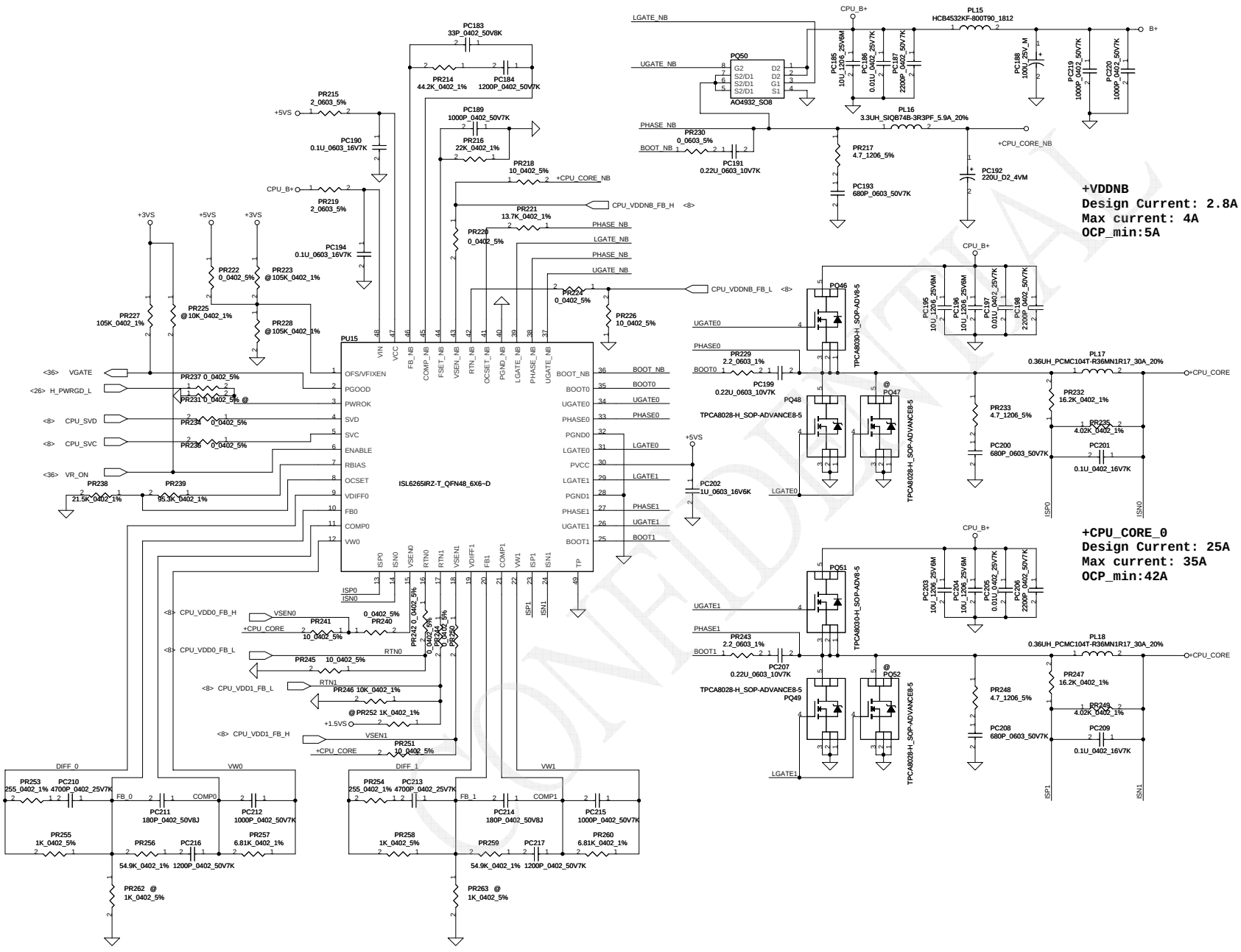

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Version change list (P.I.R. List)

for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	ADD 2 switch mos and remove 2 pull high resistance to modify VGA_CORE switch level	Before modify to fault, we recognize that VGAPWRSEL pin is open drain state. But after check with AMD AE regoer to clear the foul that VGAPWRSEL pin has driviing ability.so i take away 2 pull high resistance and add 2 switch mos to modify the switch level.	0.1	52	ADD PQ60 and PQ61 remove PR212(10K,0402) and PR213(10K.0402)	2009/08/21	EVT_NEW75
2	change thermister , tune PH1 protection and recovery set point	change thermister from 150K to 100K	0.1	44	thermister part number SL200000V00 and PR28 change to 21K, PR30 change to 9.53K	2009/08/27	EVT_NEW75
3	Add GPU voltagr sence net	Cause GPU have GCORE_SEN and FB_GND pin so power add receive net.	0.1	51	ADD GCORE_SEN and FB_GND net, also add PR296(0_0402_1%), PR297(10_0402_5%) and PR298(0_0402_5%)	2009/09/04	EVT_NEW75
4	change DC-IN connector part number	to meet pin definition	0.1	43	change part number is SP020908120	2009/09/10	EVT_NEW75
5	change reistance PR81 value	Cause meet battery Ki value setting from 1.106 to 0.7224. change PR81 from 154K(0402_1%) to 80.6K(0402_1%)	0.1	46	change resistance PR81 value from 154K to 80.6K	2009/09/22	EVT_NEW75
6	ADD switch circuit for 1.05V	Cause follow AMD electrcial sheet, VDDIO/ VDDR voltage setting procedure. AMD processor will switch between 1.05V and 0.9V by VDDIO and VDDR	0.1	48	ADD PR161 (165K_0402_1%), PQ58,PR152(10K_0402_5%),PR160(10K_0402_5%), PC131(0.1U_25V6) , change PR161 value from 100K to 249K, and ADD enable net name -VDDR_SW	2009/09/22	EVT_NEW75
7	change resistance size	cause for component de-rating . Prevent the component break down when inrush current happen.	0.1	46	change PR61 from (0.02_1206_1%) to (0.02_2512_1%)	2009/10/06	EVT_NEW75
8	Modify VGA_CORE mapping table.	cause ATI change power play voltage, so change the table value.	0.1	51	change PR198 from 9.76_0402_1% to 9.53_0402_1%, PR197 from 37.4_0402_1% to 64.9_0402_1% and PR201 from 17.8_0402_1% to 31.6_0402_1%	2009/10/06	EVT_NEW75
9	Change 1.0VSGP enable RC value	Prevent LDO can't turn off when it should turn off	0.1	50	Change PR173 from 100K_0402_5% to 10K_0402_5%, PC146 from 0.1u_0402 to 1u_0402	2009/10/15	EVT_NEW75
10	Change lowside MOS of VGA_CORE	Cause light load efficiency result is fail, and we get result after discuss FAE. The reason is lowside mos Rdson too less and IC will detect not very sensitive	0.1	51	Change PQ39 and PQ40 from TPCA8028(SB00000GL00) to AO4456(SB000009F80)	2009/11/19	EVT_NEW75
11	Change 3/5Valw boost resistance value	For EMI request	0.1	45	Change PR40 and PR47 from 0_0603_5% to 2.2_0603_5%(SD013220B80)	2009/11/19	EVT_NEW75
12	ADD two capacity	For EMI request	0.1	52	Add pc219 and pc220 are both S CER CAP 1000P 50V K X7R 0402	2009/11/23	EVT_NEW75
13	ADD three resistance	Cause madison and park need different voltage switch level so add different resistance value for the problem.	0.1	51	Add PR197(68.1K_0402_1%) , PR198 (9.53K_0402_1%) and PR201 (31.6K_0402_1%)	2009/11/23	EVT_NEW75
14	Change chock	Cause A phase put wrong chock	0.2	37,39,40	Change PL9 from SH00000FK00 to SH000009Q00	2009/11/23	EVT_NEW75

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Version change list (P.I.R. List)

DVT Stage

1. remove Y4 related
2. add a bead on +VDDA11PCIE ---ok (add L28)
3. use 6mohm MOS on +1.1VS ---ok (U38,U37)
4. +1.1VALW vlotage level --check PW rail
5. check EC sequence (syson/vga_on) --ok
6. VRAM ID --ok
7. VRAM_RST circuit -- check slew rate
8. 3G module circuit update --ok
9. EC 500K circuit --ok
10. MEMZN circuit (0ohm/10uF) --ok
11. check GBE PU/PD --ok
12. check capacitor size
13. TXC crystal value --ok (change X1,Y2), Y5
14. internal clock circuit --ok
15. ADD VGAPWR_ON --ok, INT_VGAPWR_ON
16. define PX_FN/CLK_MODE strap pin --ok
17. define CLK_REQ for internal CLKREQ --ok
18. change 4.7u_0805 type --ok
19. BOM change for SG --ok
20. add VGAPWR_ON for SG&int clock use --ok
21. add PJ25 --ok
22. LED1/3 680ohm, LED2/4 3.9Kohm --ok
23. add MUXLESS strap --ok (R521,R612)
24. add LPW planel feature --ok (LOCAL_DIM / COLOY_ENG_EN)
25. EC version control--ok (R529,R528)
26. WiMAX LED combine circuit --ok (R530,R531,D47)
27. change INT_VGAPWR_ON to EC_pin91 --ok
28. add VB function --ok (R533,R532)
29. Add R534,R535,R536 for layout --ok
30. change Y5 to 33p cap
31. pop ESD diode --ok
32. set T25 to BH for main --ok
33. Define Board file ID for SW req. --ok

For PEW change list

1. Change Strap/PID/BID for SW
2. Change EC version to E0
3. Change thermal sensor to SB-TSI
4. Define 8L_6L_UMA strap on SB
5. Change EC version to D3 06/29

PVT Stage

1. un-pop D39,D41	p.40
2. pop D27	p.39
3. un-pop Q73,Q74,Q75,Q70,R500,R502	p.38
4. Change R470 to 8.2K	p.36
5. Change R600,R510,R489 to 100K	p.22/p.42
6. Change C847 to 0.1u	p.22
7. Change C739,C740 to 15p	p.36
8. Change LED resistance R477,R499 change to 2.2K	p.37
9. Change R611 to 33K	p.42
10. Change HDMI_HPD PU from +3VSG to +3VS	p.24
11. Change C957,C971 to 0.47u_0603	p.40
12. Remove VGA option solution unpop R147,R420,R421,R248 pop R161	p.16/p.22/p.17
13. Pop R595,R596,Q49,Q48 change R595 to 300k	p.42
14. Change LED1,LED3 to SC591NB5A30	p.37
15. Change Q5,Q26 to SB00000DH00	p.16/p.37
~~16. Change C468~C475 to MAD@~~	~~p.20~~
17. Change C305,C306 to 0603 size	p.18
18. Change LED control circuit, Pop R537,R457	p.34/p.35
19. Update AMP GAIN to 10dB	p.40
20. Change C11,C56,C723 to SGA00002N80	p.8/p.9/p.35
21. Change TPC24 to TPC12 for layout	

MP Stage

1. Add R541, R542 for TSI leakage current issue. (option)	p.36
~~2. Change C21 from 3300pF to 100pF~~	
3. Unpop C21	
4. Unpop SW3	
5. Change C305 to MAD@	
6. Change VGA to R3 P/N	0419
7. Unpop ESD Diode D24 / D27 / D29	0512

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Version change list (P.I.R. List)

for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
15	Change chock	Cause NB_CORE and 1.1VALW efficiency measurement result fail. so change inductor from 1.8uH to 1.0 uH, and change the tye from ferrite to moding	0.2	47,48	Change PL6 and PL8 from SH000009680 to SH000009U00	2009/12/01	EVT_NEW75
16	Change resistance value	Cause change low side MOS from TPCA8028 to AO4456. And there have different Rds(on). then OCP will different, so i need to change ocp setting resistance.	0.2	51	Change PR190 from SD000004100 (S RES 1/16W 8.2K +-1% 0402) to SD00000QM80 (S RES 1/16W 14.3K +-1% 0402)	2009/12/01	EVT_NEW75
17	ADD sunbber	Cause VGA_CORE phase ringing too strong, so add sunbber to reduce the ringing	0.2	51	ADD PR191(SD001470B80 ,S RES 1/4W 4.7 +-5% 1206) and PC171(SE025681K80 S CER CAP 6,80P 50V K X7R 0603)	2009/12/01	EVT_NEW75
18	Change resistance value	change VGA_CORE switch frequency fromm 300K to 400K, for solve efficiency fail issue	0.2	51	Change PR196 from 44.2K to 33K	2009/12/01	EVT_NEW75
19	Delete component PC73, PC83 and PC92	Cause for design resinable	0.2	47,48	Delete PC73,PC83 and PC92	2009/12/01	EVT_NEW75

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