

# Compal Confidential

## PAV70 Schematics Document

### Intel Pineview Processor with Tigerpoint + DDRII

2010-07-01

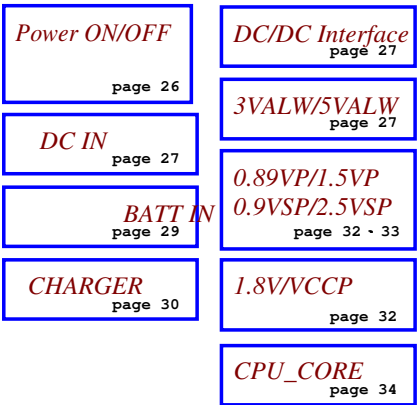
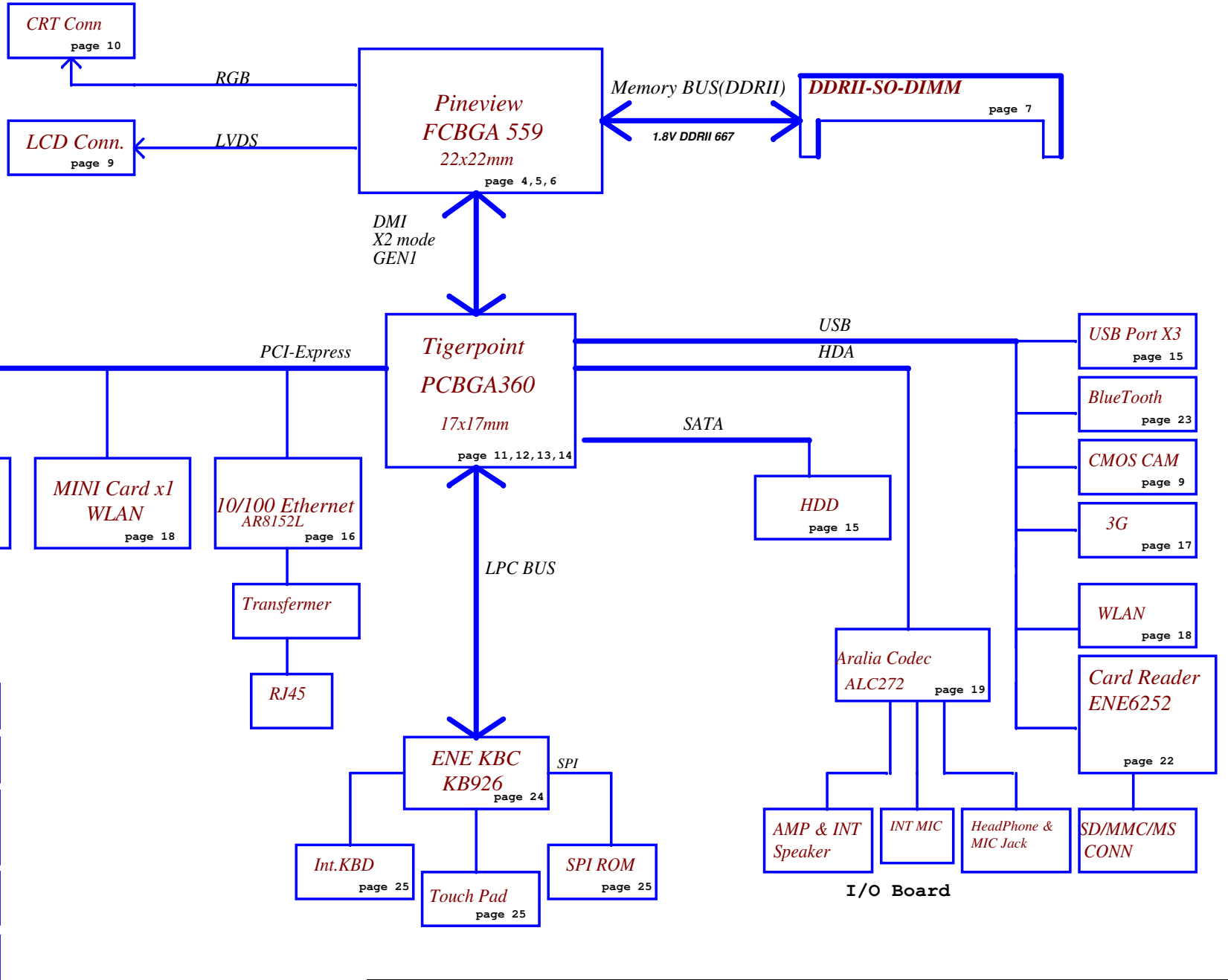
REV: 1.0

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# Compal Confidential

Model Name :  
File Name : LA-6221P

Clock Generator  
CK505  
page 8



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## Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+VCCP	VCCP switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+0.89V	Graphic core power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

## BOARD ID Table(Page 17)

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	V <sub>AD_BID</sub> min	V <sub>AD_BID</sub> typ	V <sub>AD_BID</sub> max
0 (EVT)	0	0 V	0 V	0 V
1 (DVT)	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2 (PVT)	18K +/- 5%	0.436 V	0.503 V	0.538 V
3 (MP)	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

## BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	
3	
4	
5	
6	
7	

## External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
--------	---------	-----------	------

## No PCI Device

## EC SM Bus1 address

## EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X b	EMC1402	100_1100

## Tiger Point SM Bus address

Device	Address
Clock Generator (SLG8SP556VTR)	1101 001Xb
DDR DIMMA	1010 000Xb

## USB table

EHCI1	UHCI1	Port0	MB USB Conn1.
	UHCI2	Port1	MB USB Conn2.
	UHCI3	Port2	MB USB Conn3.
EHCI2	UHCI4	Port3	CMOS
	UHCI5	Port4	Card Reader
	UHCI6	Port5	WWAN
	UHCI7	Port6	BT
	UHCI8	Port7	WLAN
	UHCI9	Port8	
	UHCI10	Port9	
	UHCI11	Port10	
	UHCI12	Port11	

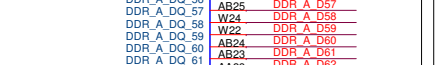
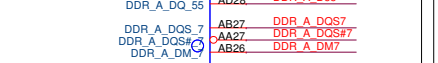
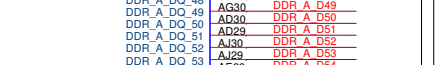
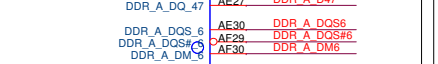
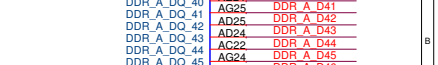
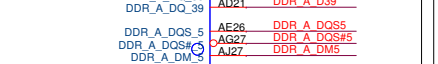
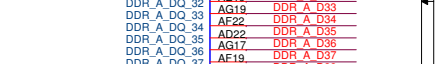
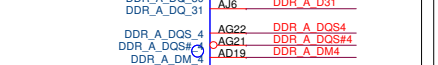
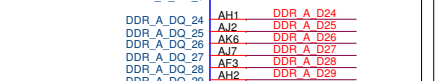
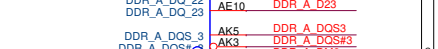
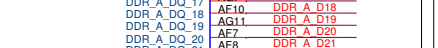
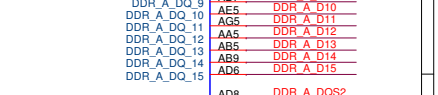
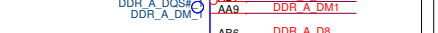
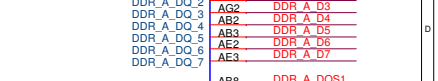
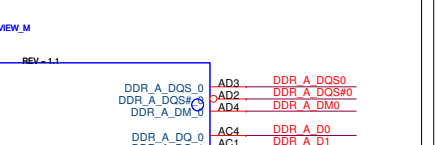
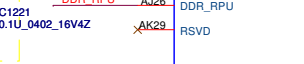
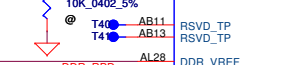
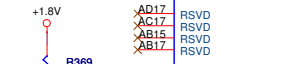
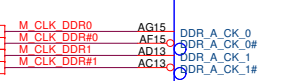
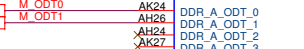
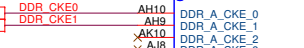
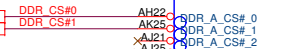
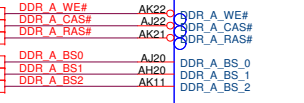
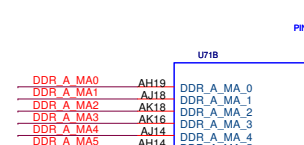
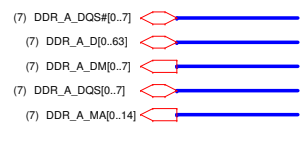
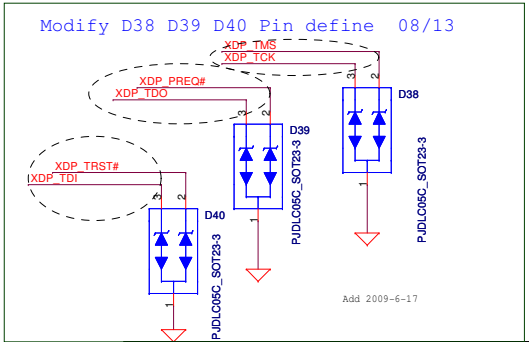
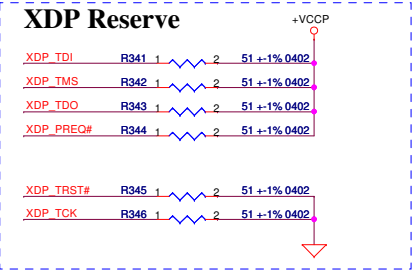
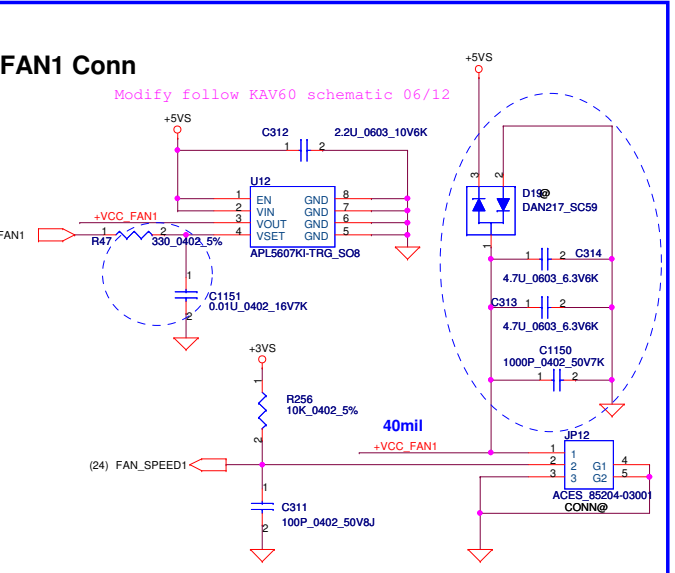
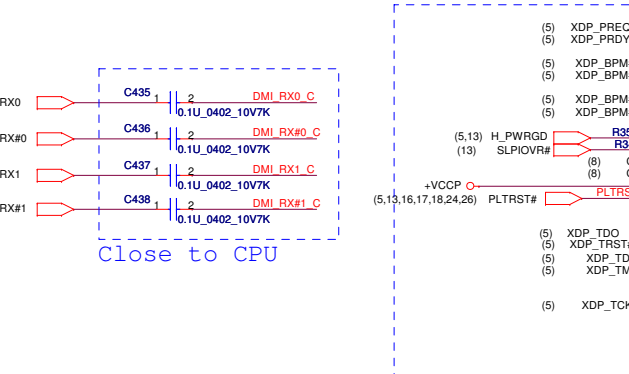
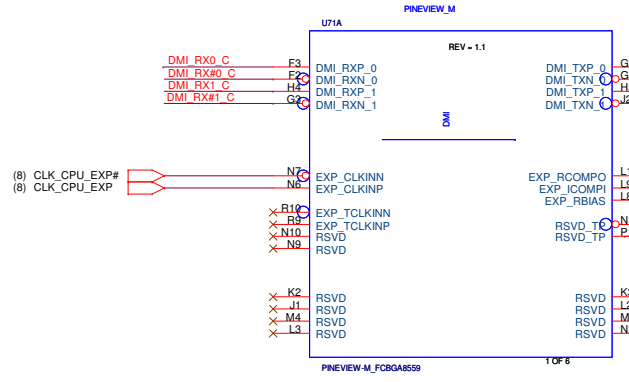
## PCIE table

PCIE port1	LAN
PCIE port2	Wireless Card
PCIE port3	3G
PCIE port4	
PCIE port5	
PCIE port6	

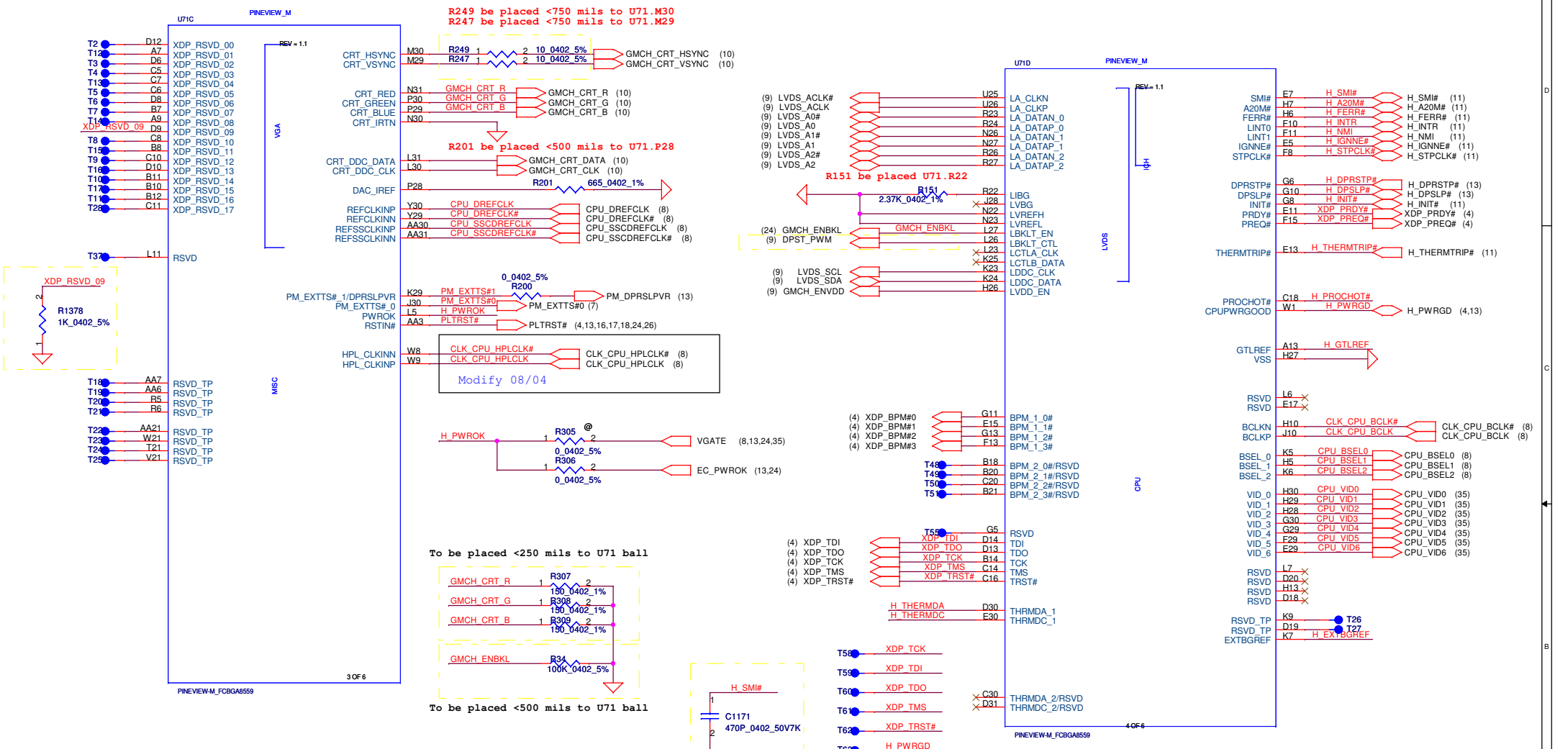
## SATA table

SATA port0	HDD
SATA port1	
SATA port2	
SATA port3	
SATA port4	
SATA port5	

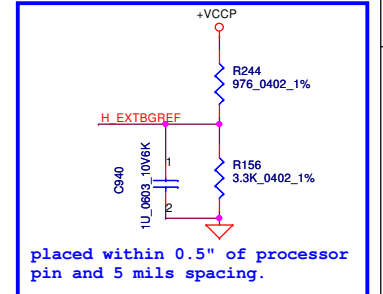
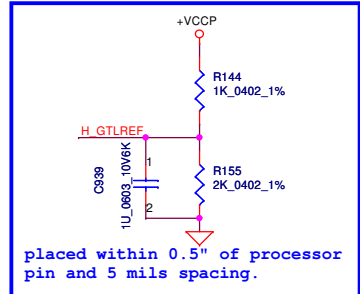
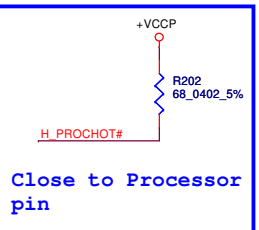
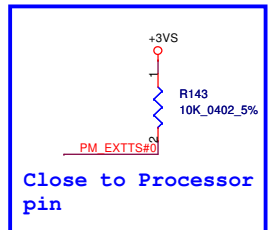
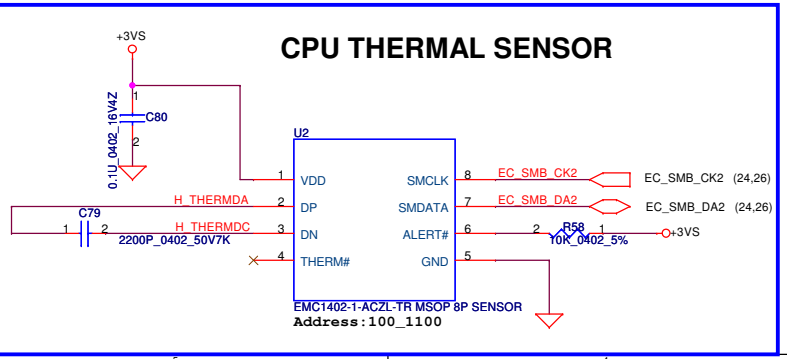
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H\_THERMDA, H\_THERMDC routing together.  
Trace width / Spacing = 10 / 10 mil

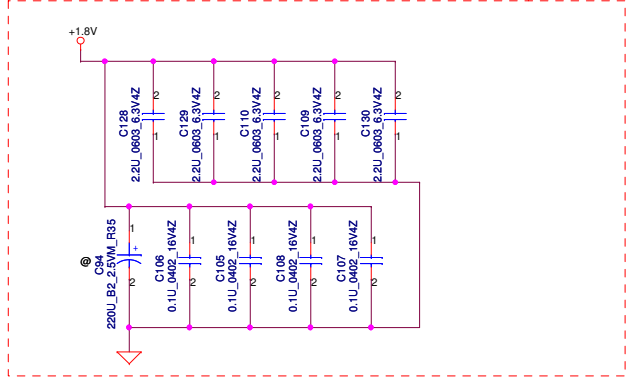
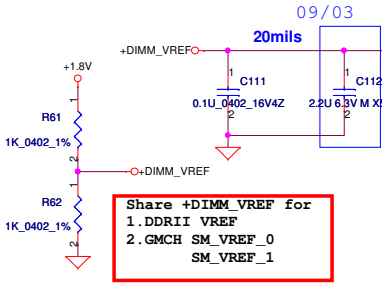


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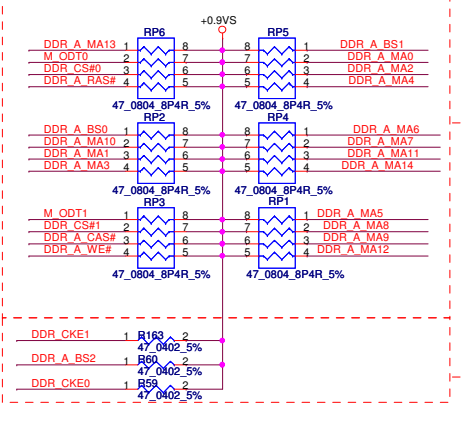
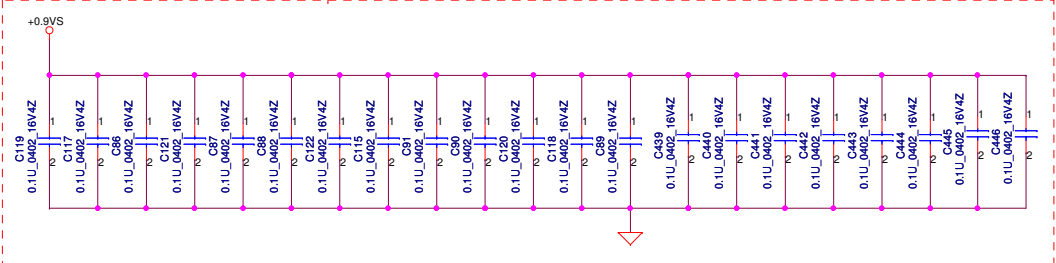


- (4) DDR\_A\_DOS#0..7
- (4) DDR\_A\_D0[0..63]
- (4) DDR\_A\_DM[0..7]
- (4) DDR\_A\_DQS#0..7
- (4) DDR\_A\_MA[0..14]

**Layout Note:**  
Place near JDIM1

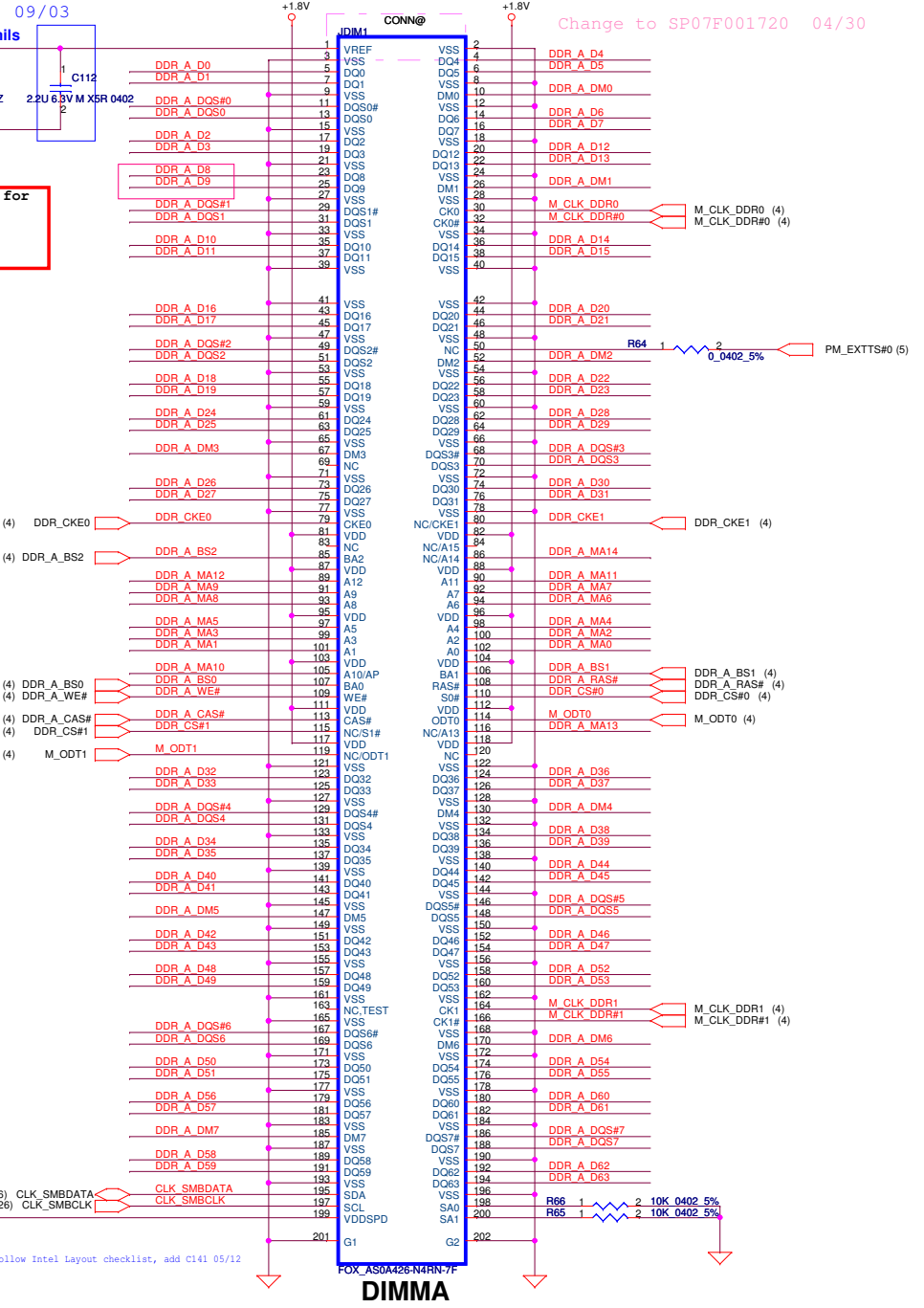
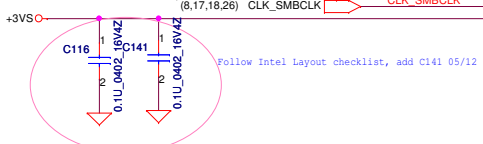


**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9VS



**Layout Note:**  
Place these resistor closely DIMMA, all trace length < 750 mil

**Layout Note:**  
Place these resistor closely DIMMA, all trace length Max=1.3"



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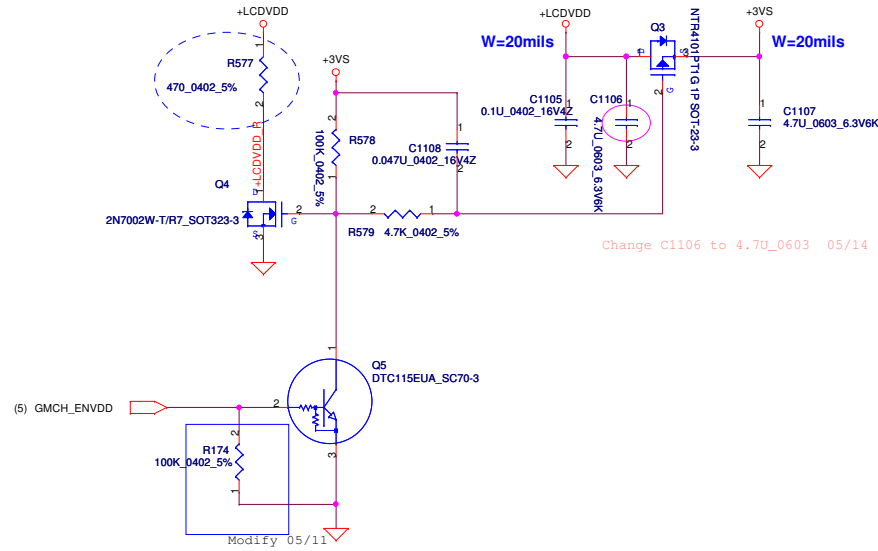






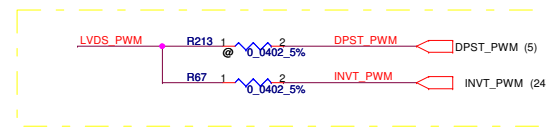
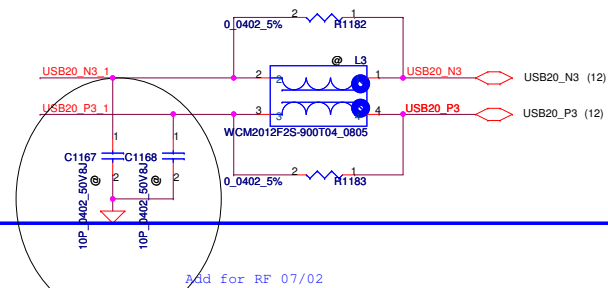
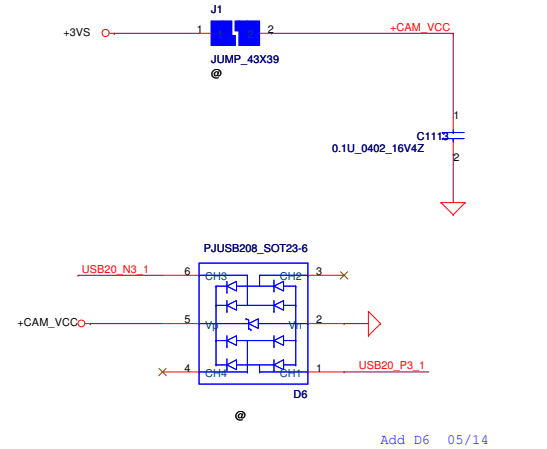
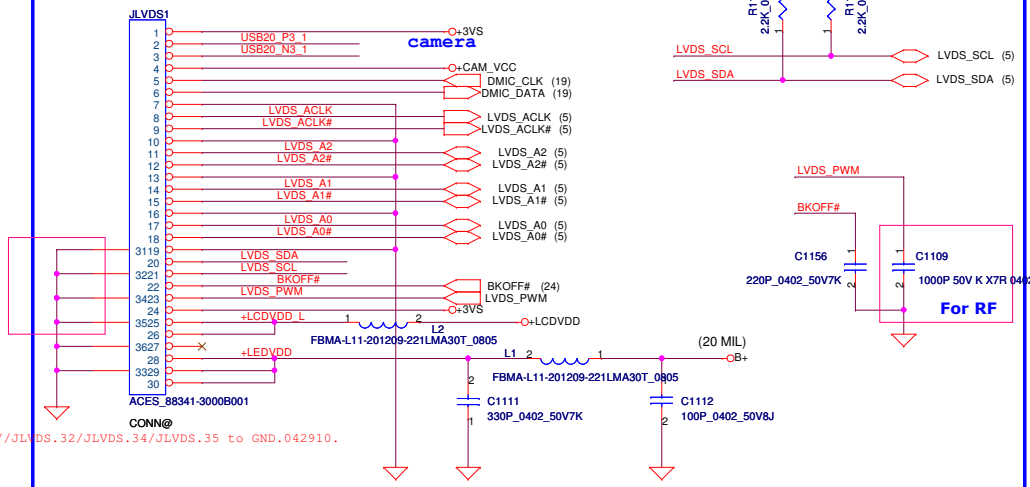
### LCD POWER CIRCUIT

Change R577 to 0402 SIZE 06/16



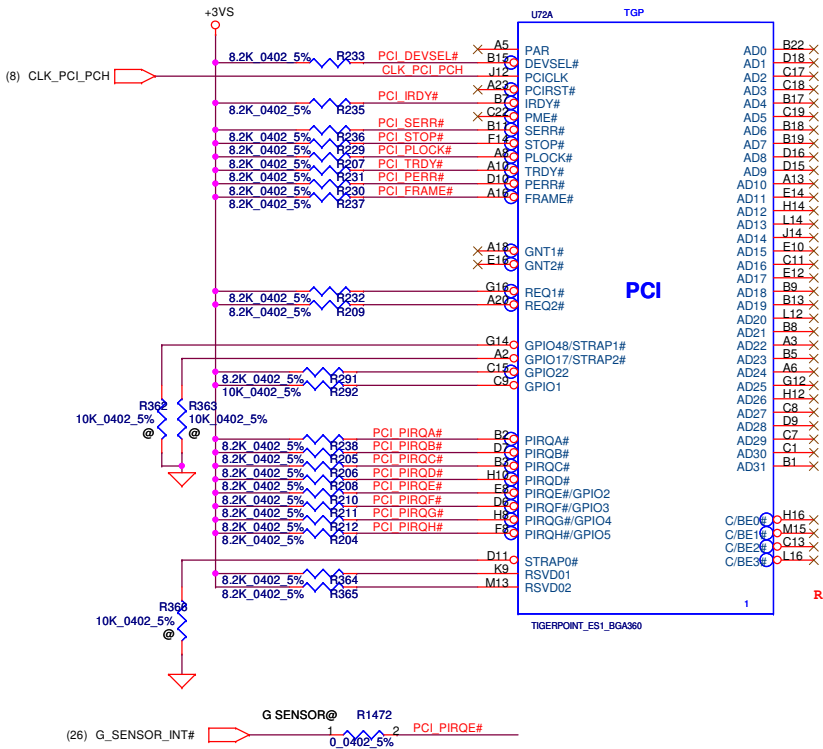
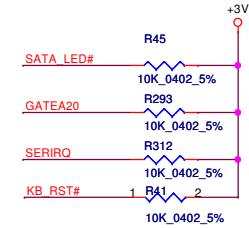
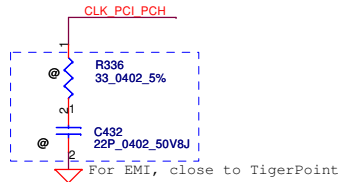
### CMOS & LCD/PANEL BD. Conn.

Modify JLVD51 08/04

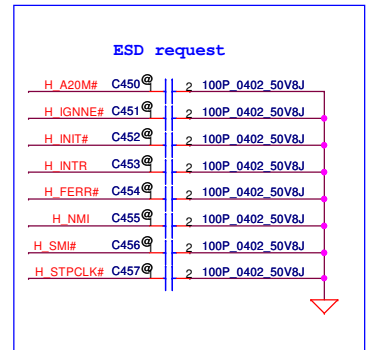
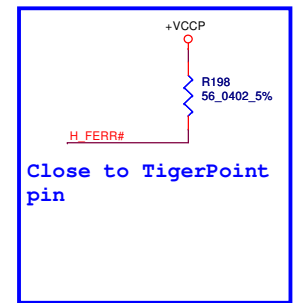
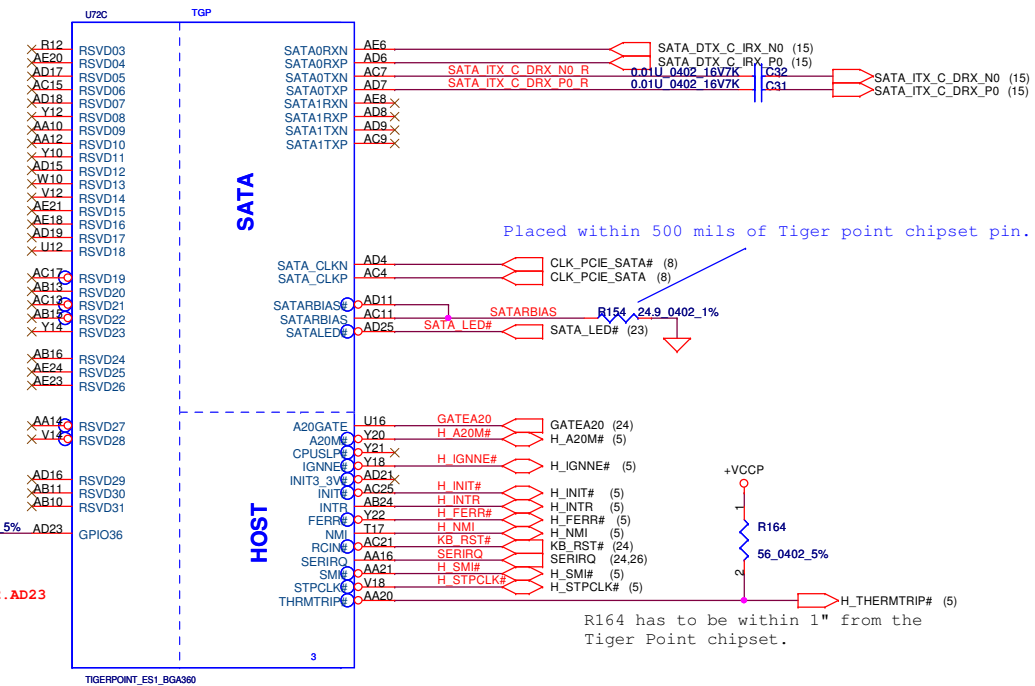


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STRAP2# GPIO17	STRAP1# GPIO48	Boot BIOS
0	1	SPI
1	0	PCI
1	1	LPC

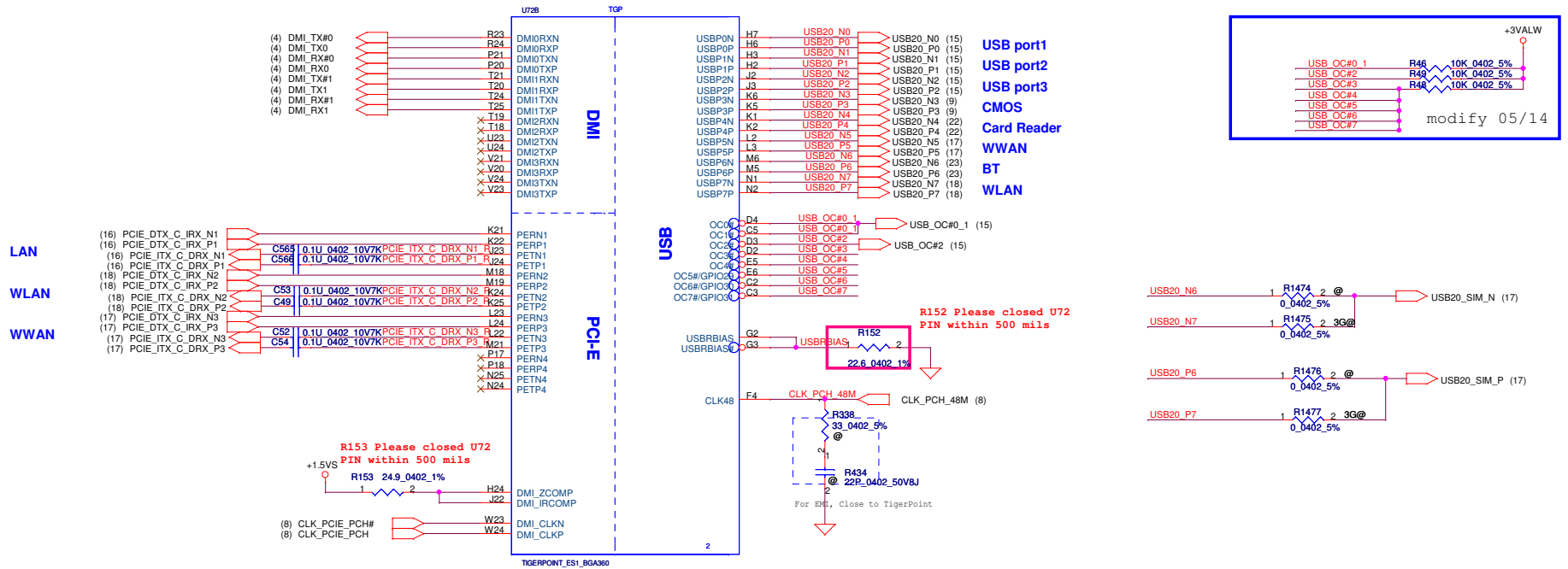


PCIE Port List

1	LAN
2	WLAN
3	WWAN
4	

USB Port List

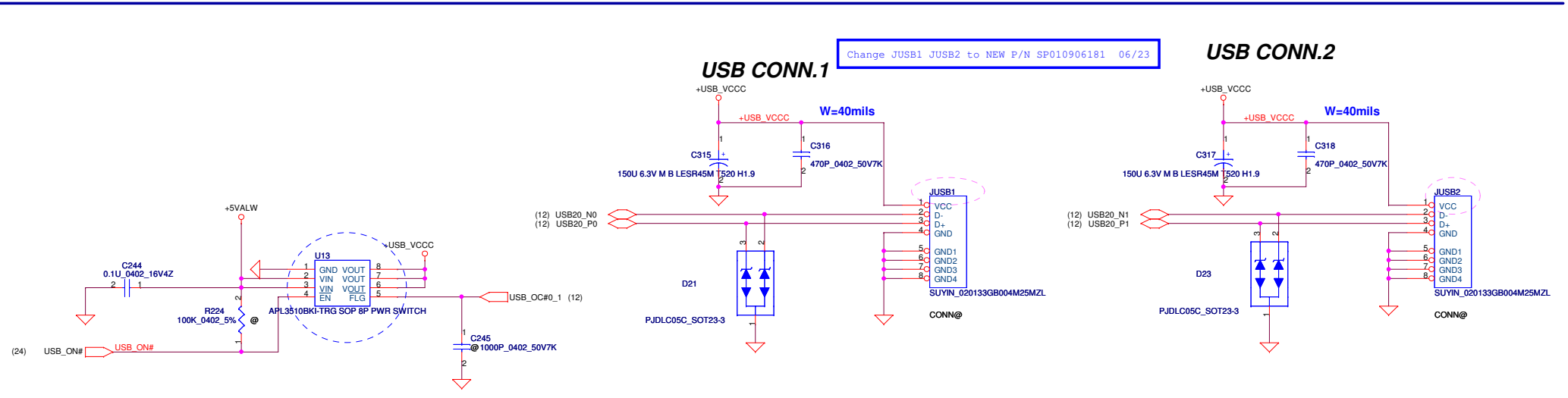
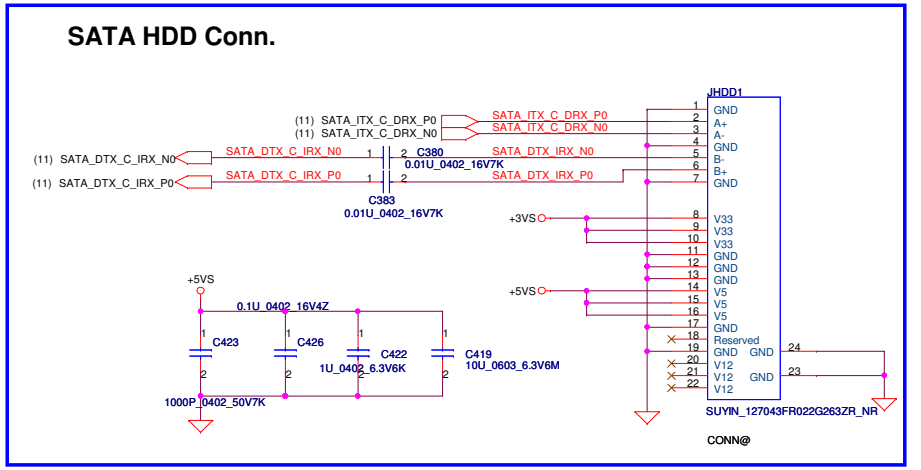
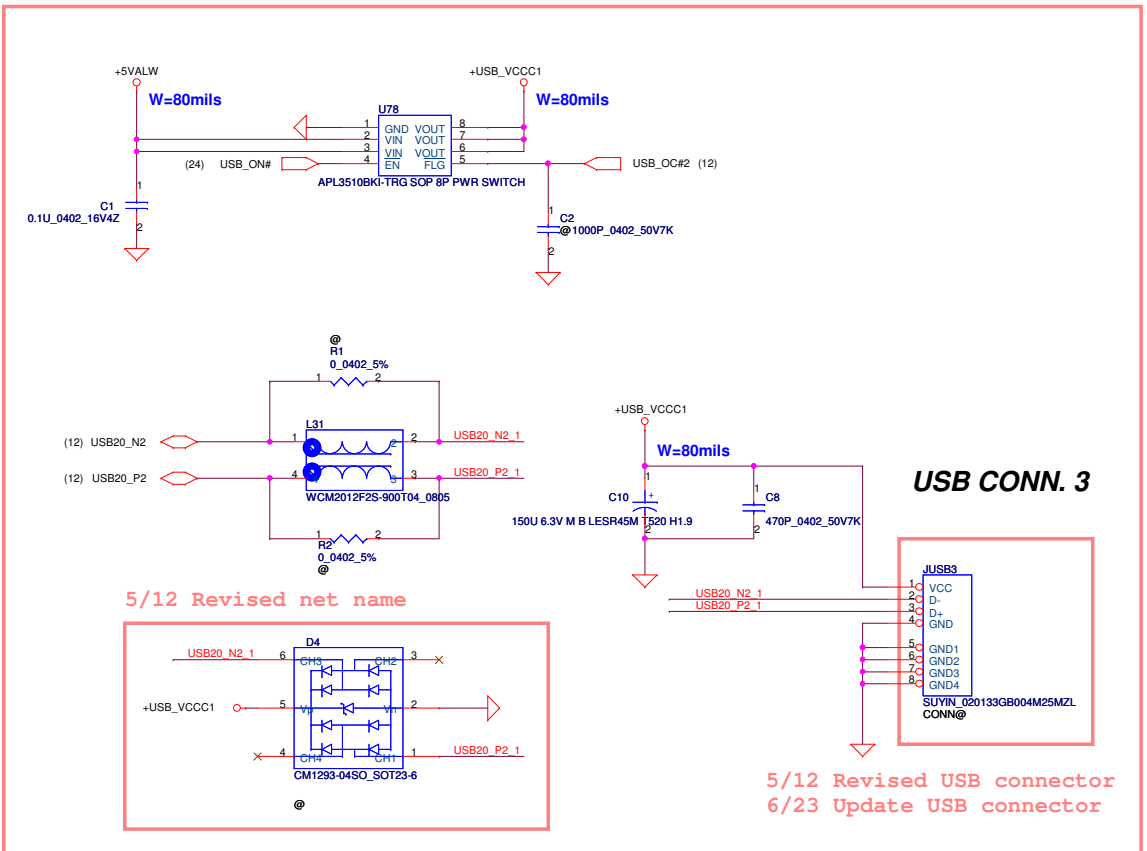
0	USB Left1
1	USB Left2
2	USB Right2
3	CMOS
4	CardReader
5	WWAN
6	BT
7	WIMAX



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				Custom	LA-6221P
				Date:	Thursday, July 01, 2010
				Sheet	12 of 39
				Rev	1.0



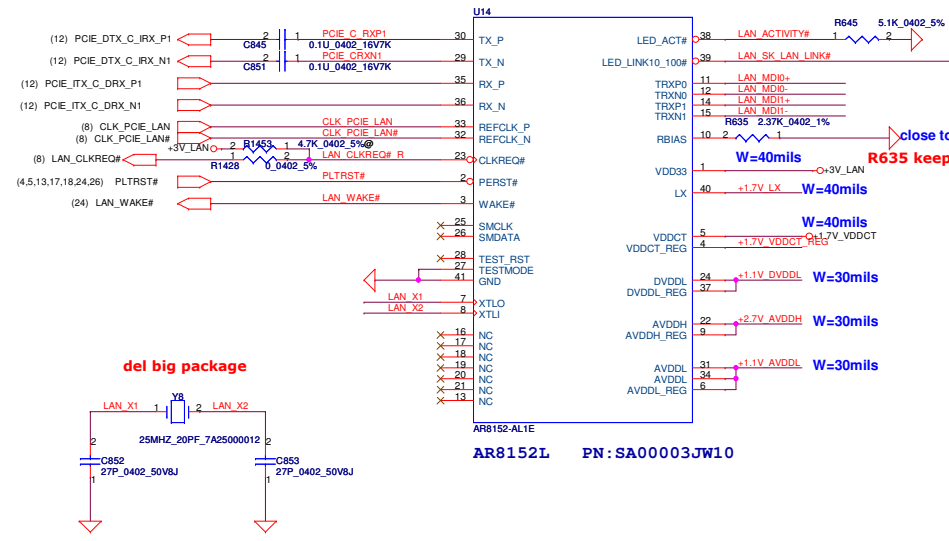




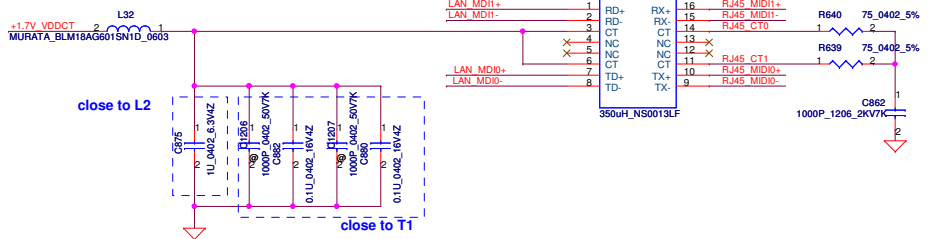
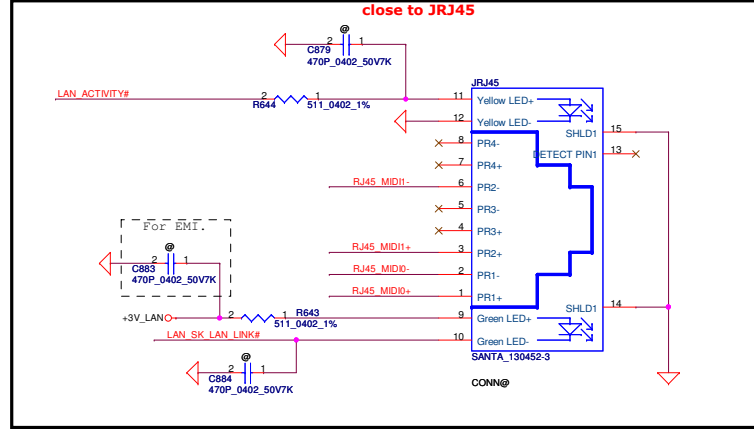
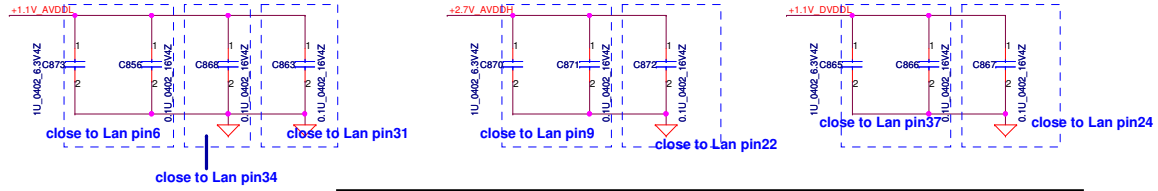
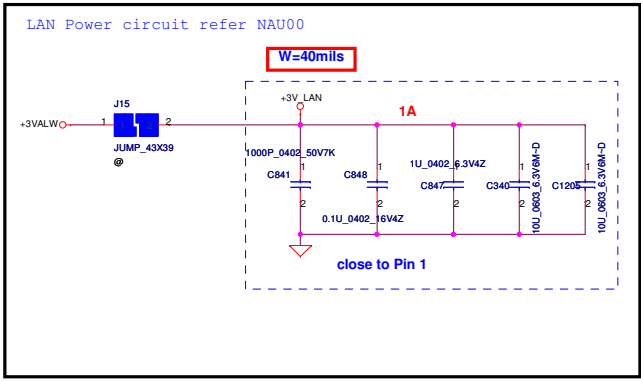
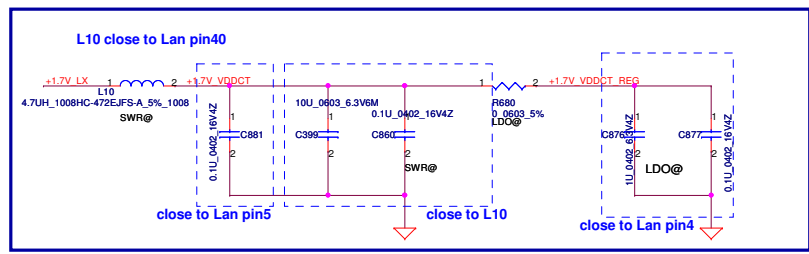
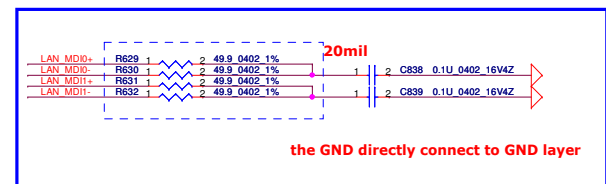
Security Classification	Compal Secret Data			Title		
Issued Date	2006/08/18	Deciphered Date	2007/8/18	SATA,CONN. / USB CONN.		
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				B	LA-6221P	0.2
				Date:	Thursday, July 01, 2010	Sheet 15 of 39



Change LAN chip to AR8152-L for NAV70/80 DDR3 2010/01/22

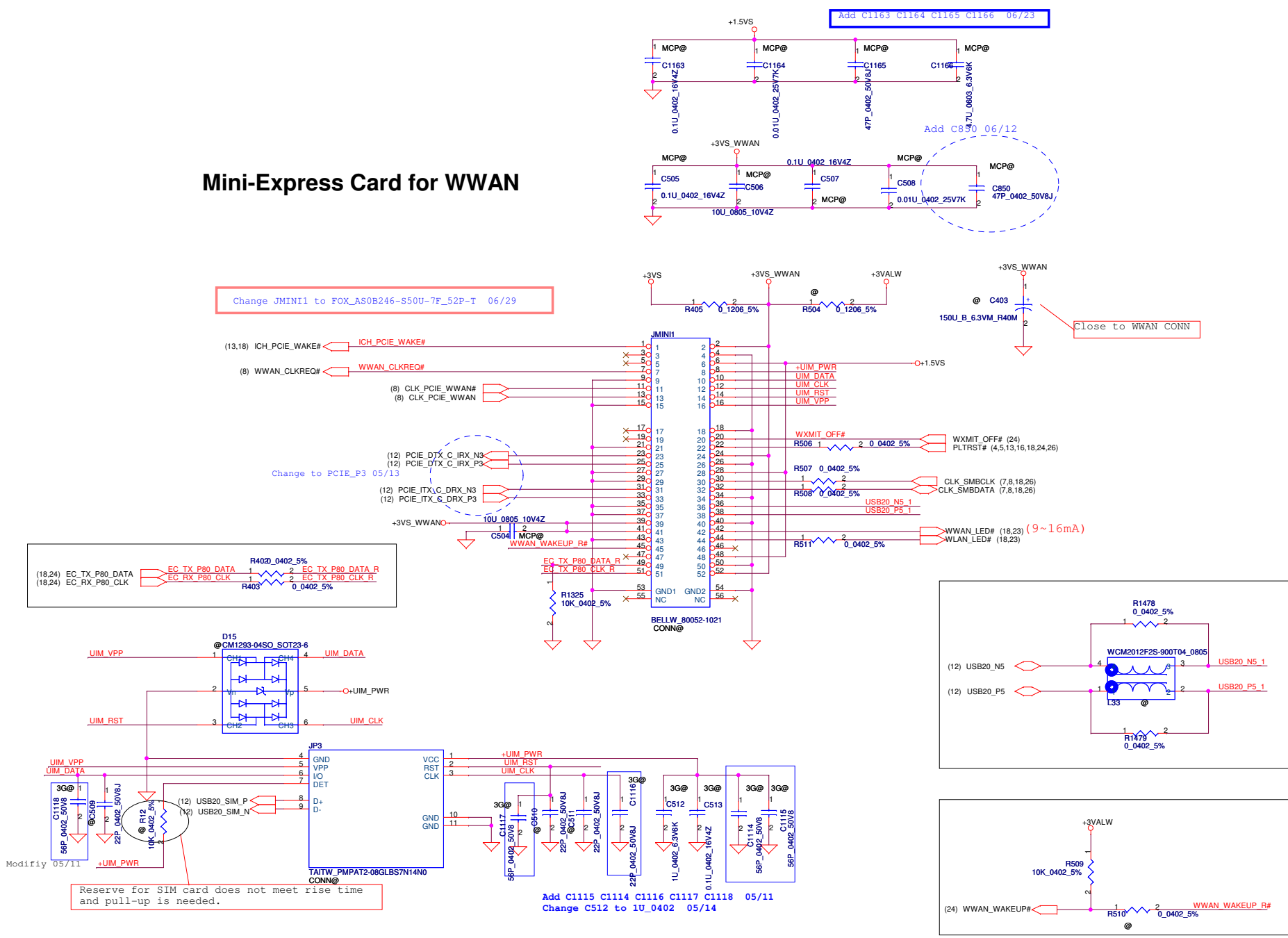


Switch mode:由+1.7V\_LX供給+VDDCT pin39 need to pull high resistor of 5.1k  
LDO mode:由+1.7V\_VDDCT\_REG供給+VDDCT pin39 need to pull low resistor of 5.1k



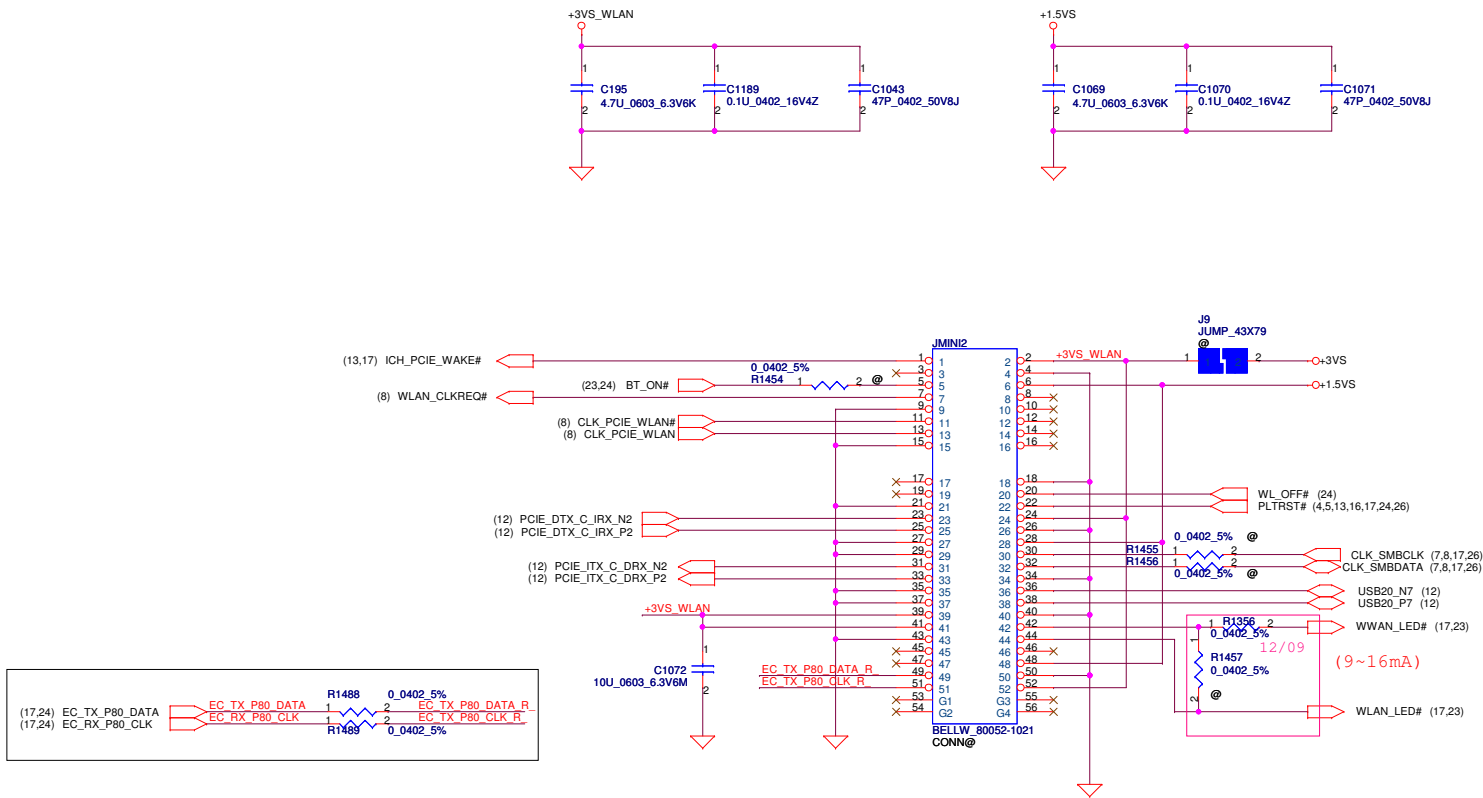
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/7/7	Deciphered Date	2010/7/7	Title
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Size	Custom	Document Number	LA-6221P	Rev
				0.1
Date:	Thursday, July 01, 2010	Sheet	16	of 39

# Mini-Express Card for WWAN



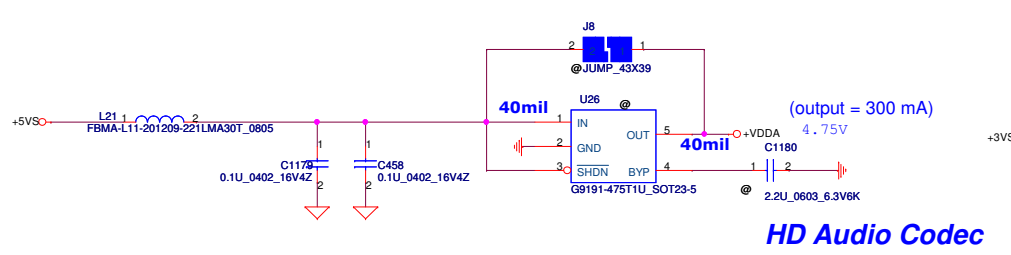
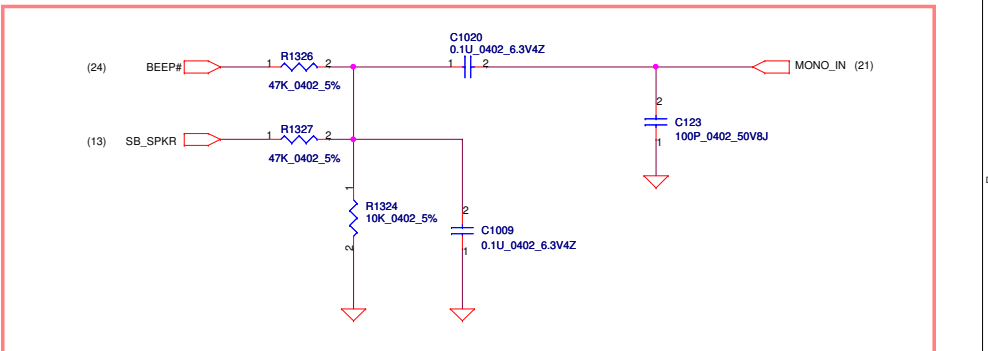
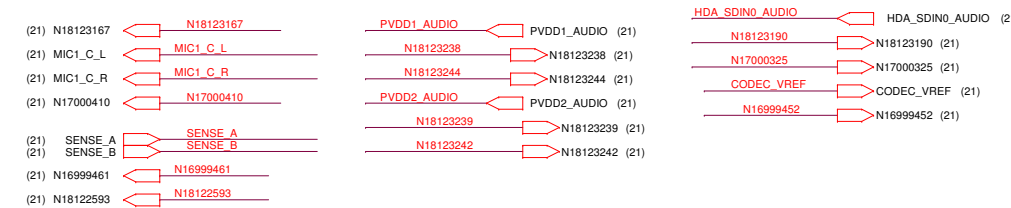
Security Classification		Compal Secret Data		Title	
Issued Date	2006/08/05	Deciphered Date	2007/8/18	Mini-Card	
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Date:	Thursday, July 01, 2010	Sheet	17	of	39

# Mini-Express Card for WLAN

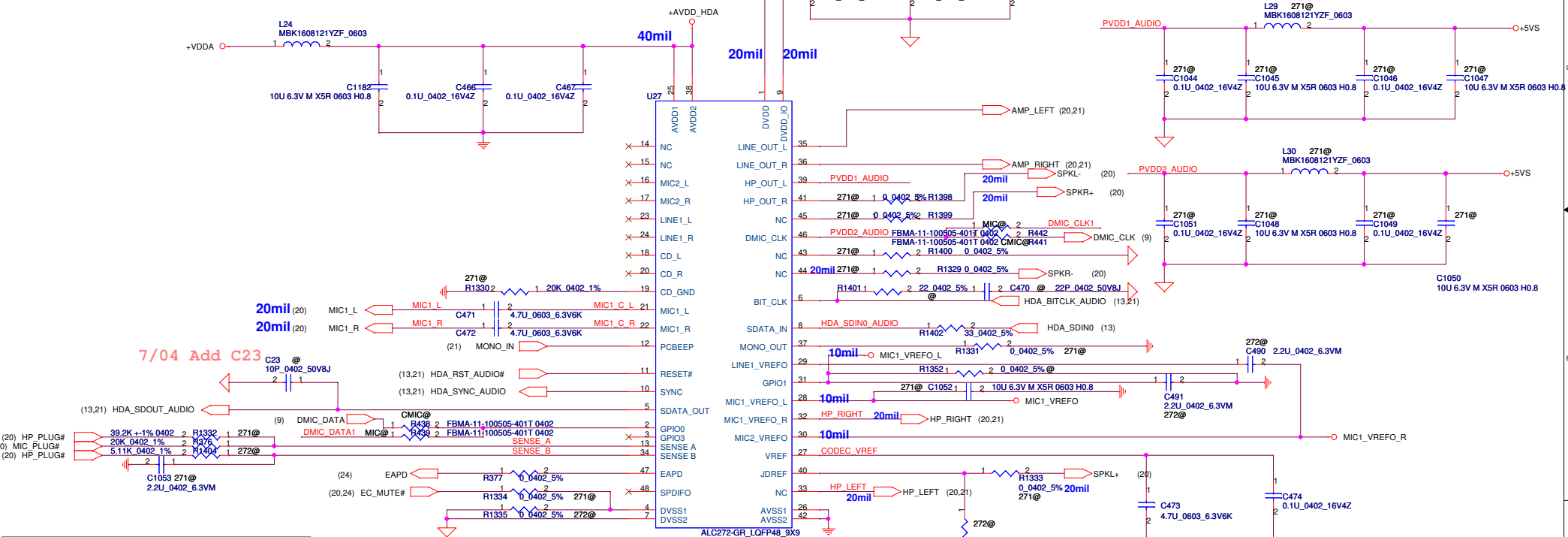


5/12 Update WLAN connector(the same as KAV60)  
 6/1 Revised 37、39、41、42、43 to NC  
 6/12 Update connector to DC040006S00  
 6/26 Update JMINI1 footprint  
 7/01 update pin 23,25,31,33

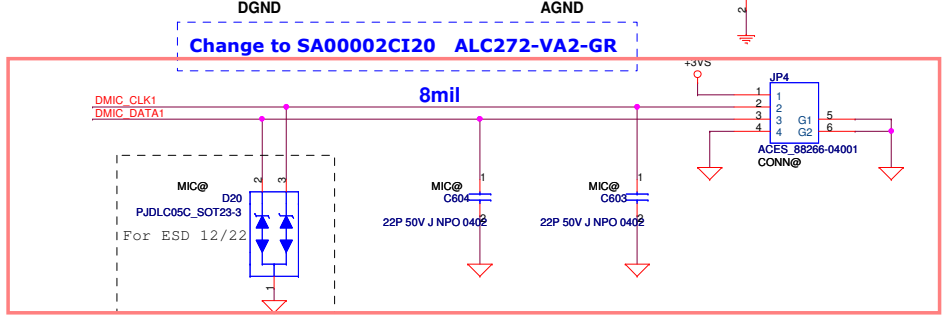
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Issued Date	2006/08/05	Deciphered Date	2007/8/18	Title	
				WLAN	
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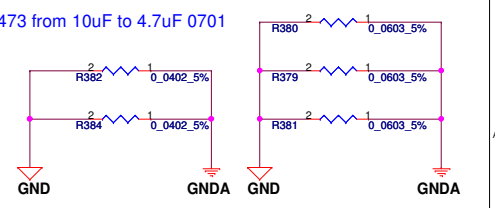
### HD Audio Codec

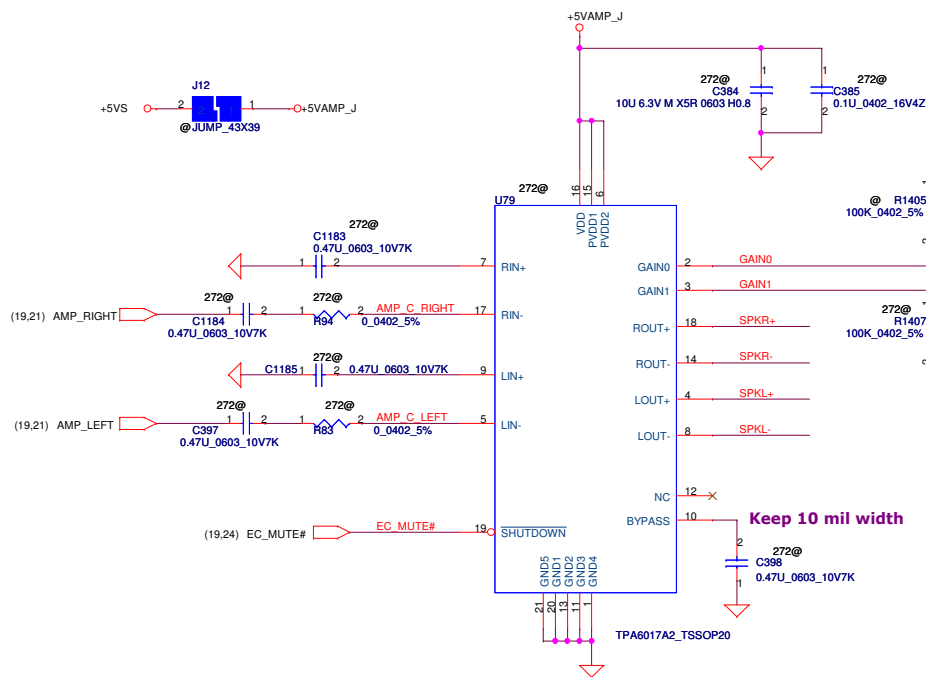


Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
SENSE B	5.1K	PORT-D (PIN 35, 36)
	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)



change C473 from 10uF to 4.7uF 0701

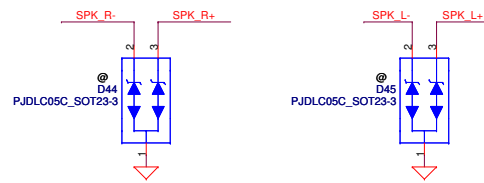
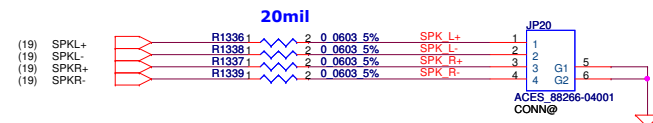




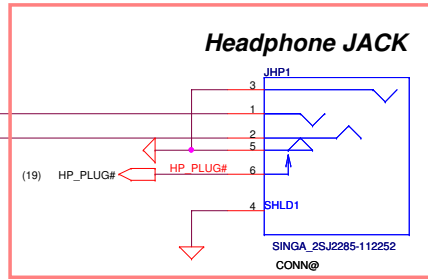
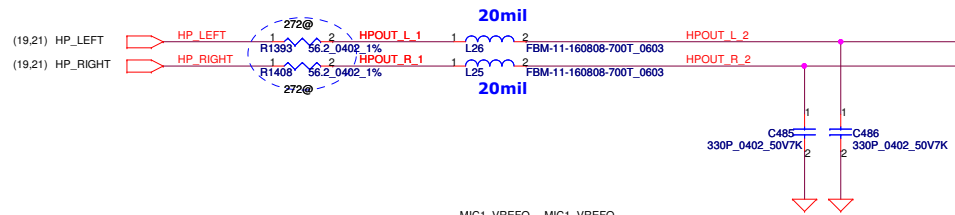
20081029 Update to 6dB

Keep 10 mil width

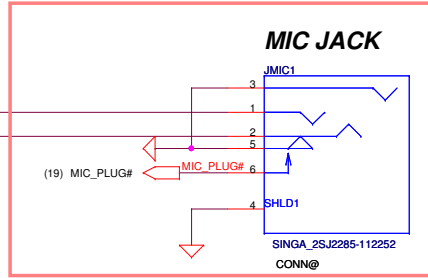
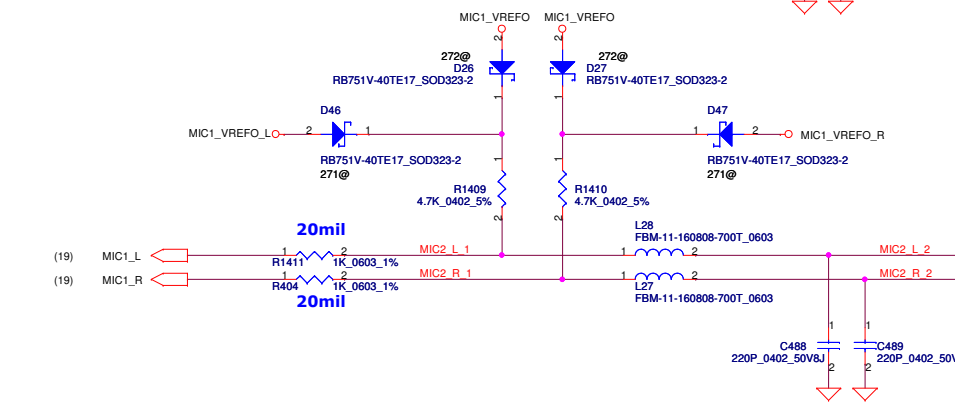
### Int. Speaker Conn.



NU D44 & D45 0623



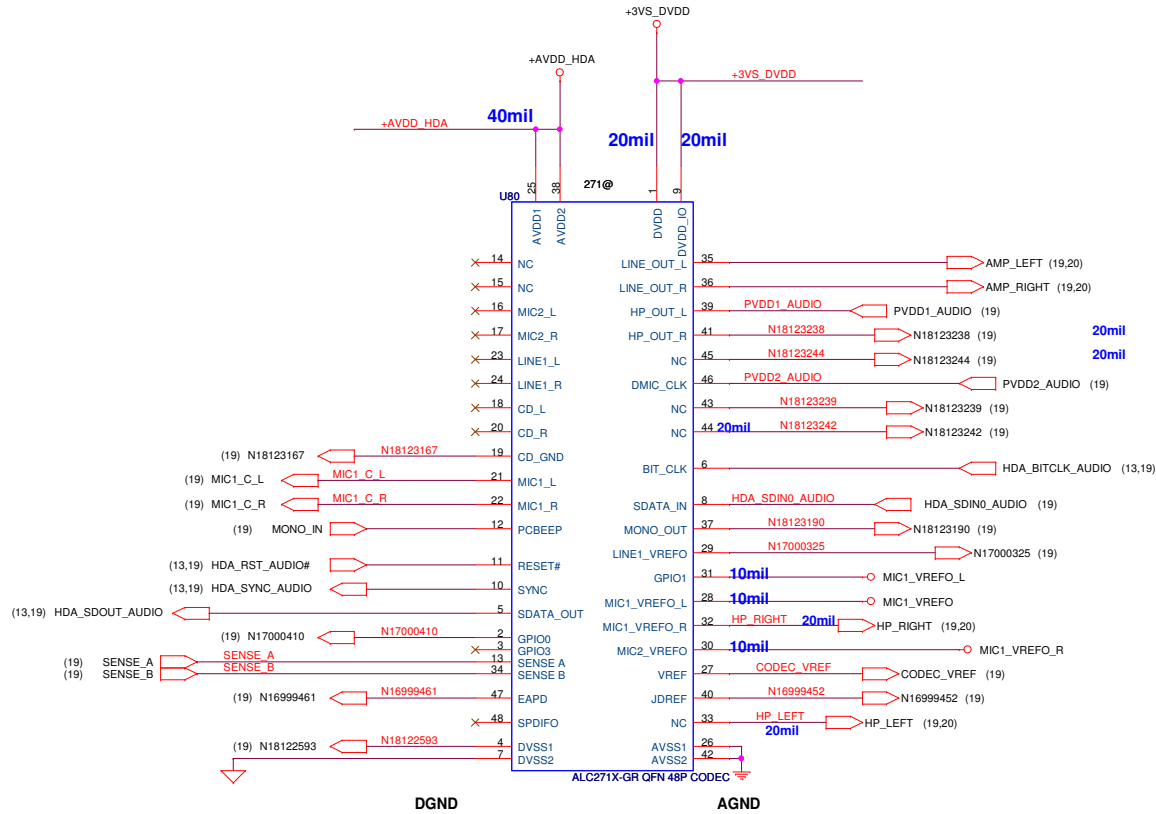
6/19 Update Headphone connector



6/19 Update MIC connector

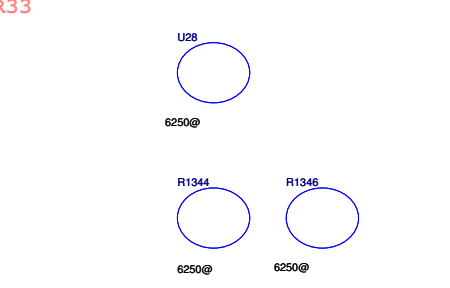
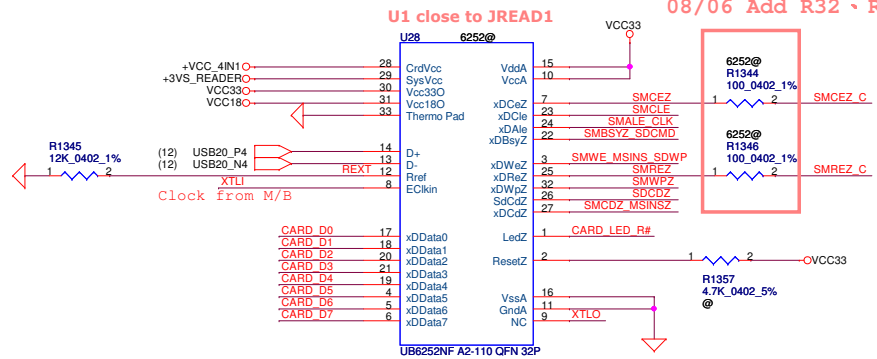
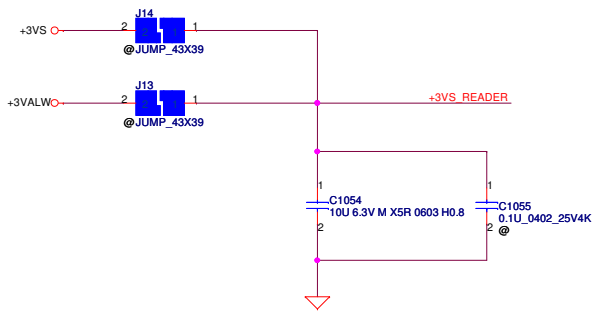
Security Classification	Compal Secret Data		Title	
Issued Date	2006/08/05	Deciphered Date	2007/8/18	Amplifier & Audio Jack
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Date: Thursday, July 01, 2010				LA-6221P
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# HD Audio Codec

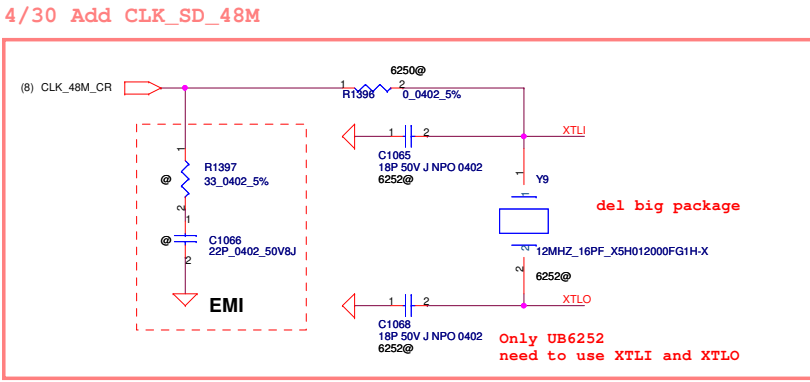
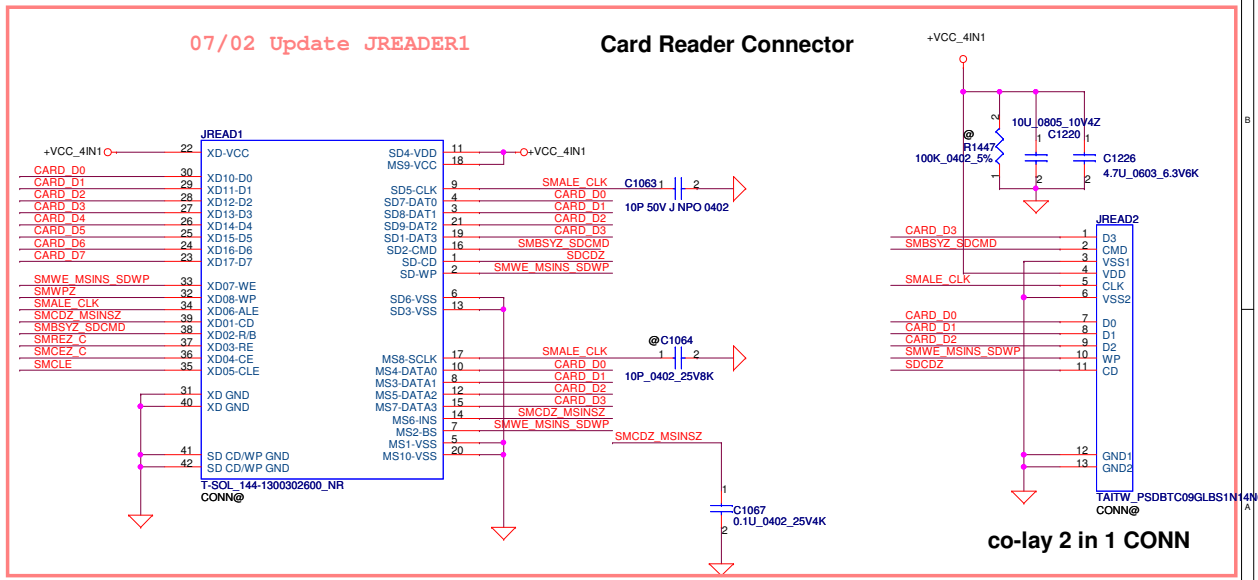
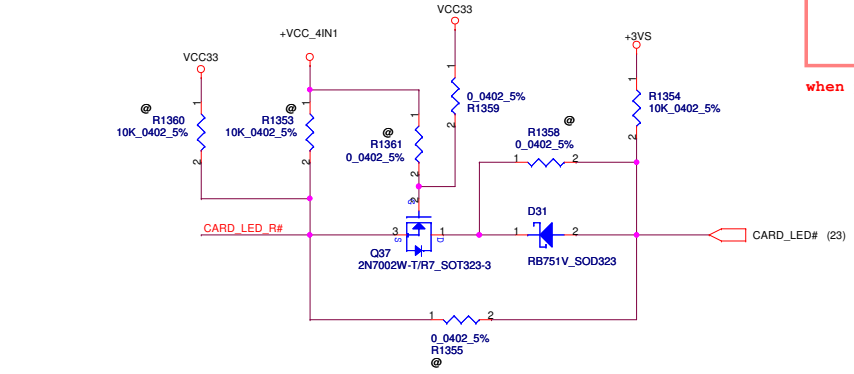
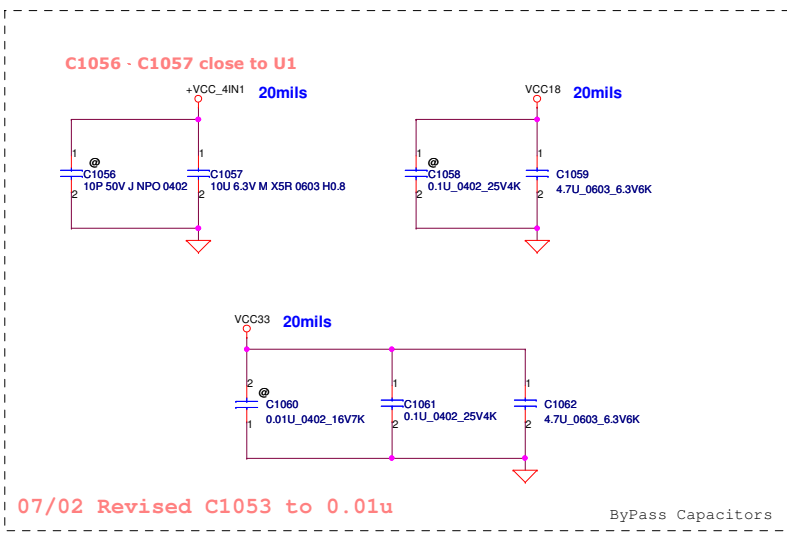
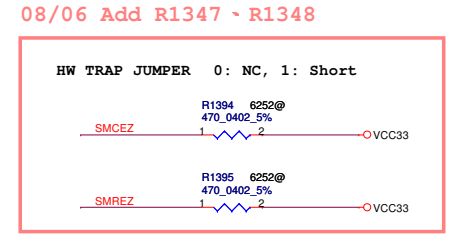


Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

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			Size	Document Number
			LA-6221P	
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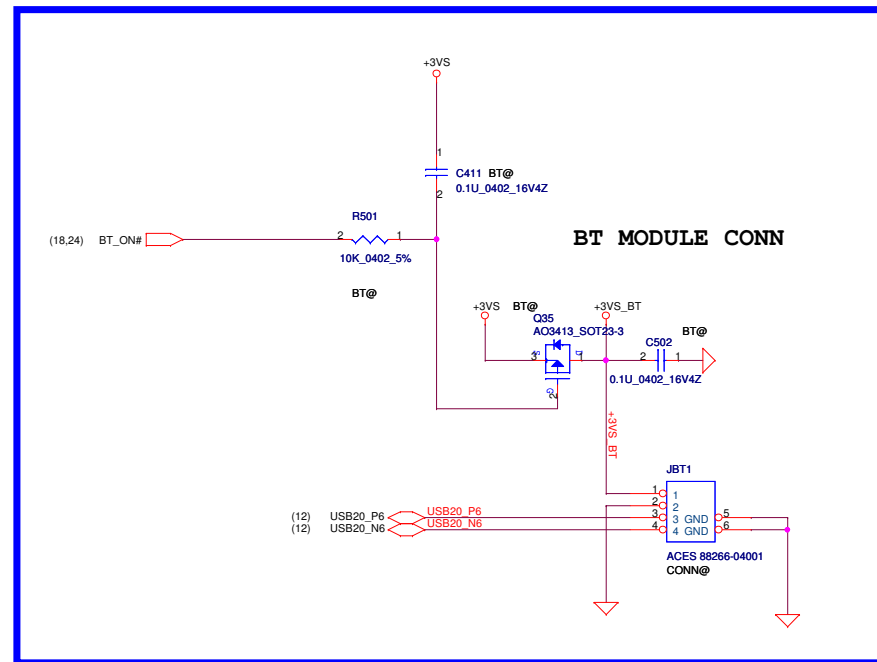
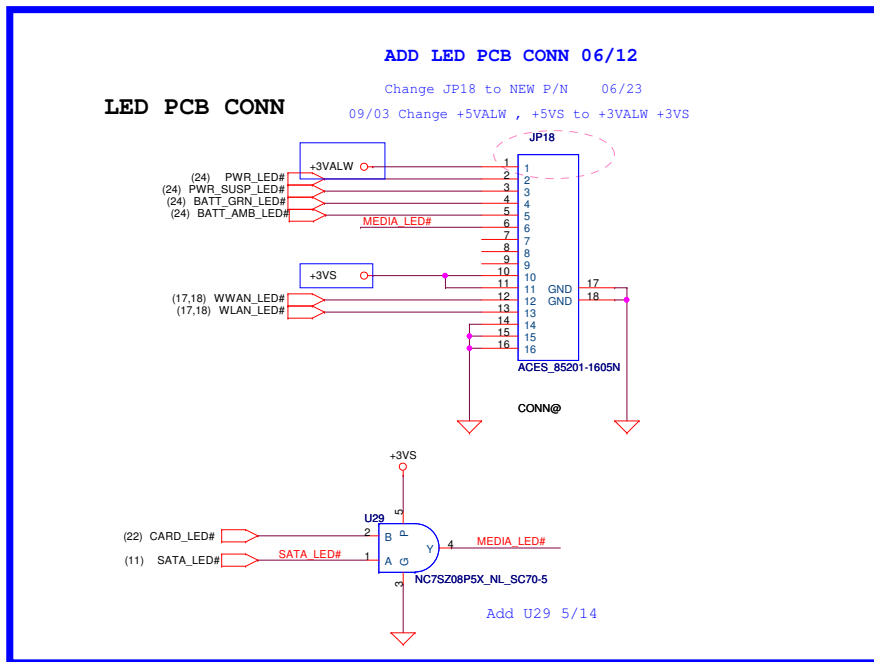


If use external crystal (Y4),  
U1 will change UB6252

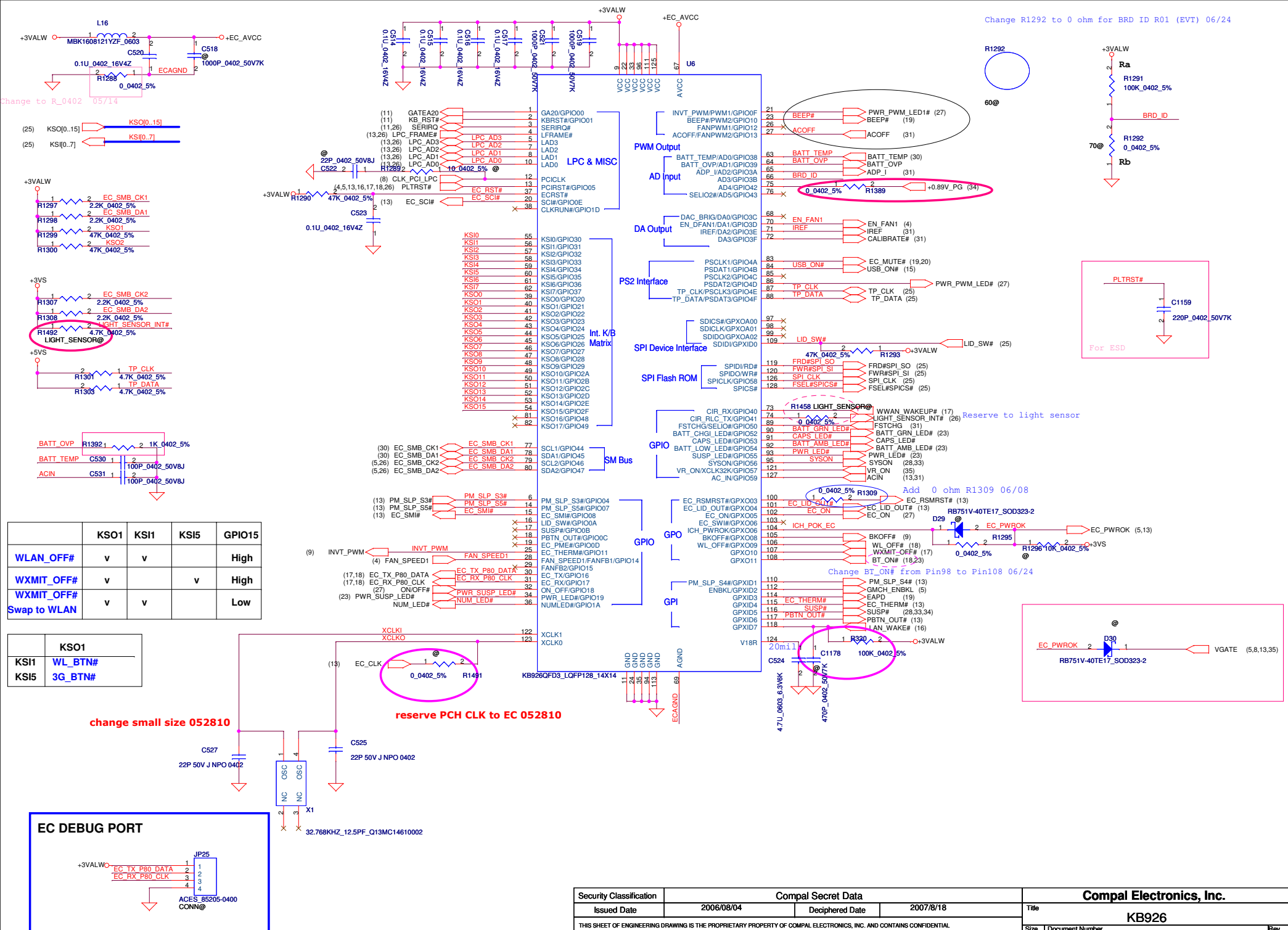


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				Rev	0.2



Change to R\_0402 05/14

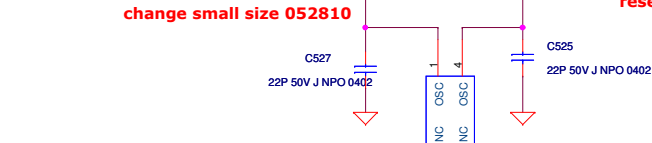
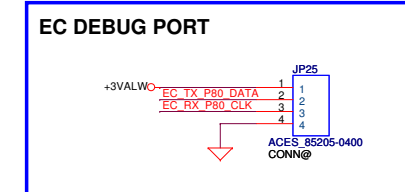
EC SMB CK1  
EC SMB DA1  
EC SMB CK2  
EC SMB DA2  
LIGHT\_SENSOR\_INT#  
LIGHT\_SENSOR#

TP\_CLK  
TP\_DATA

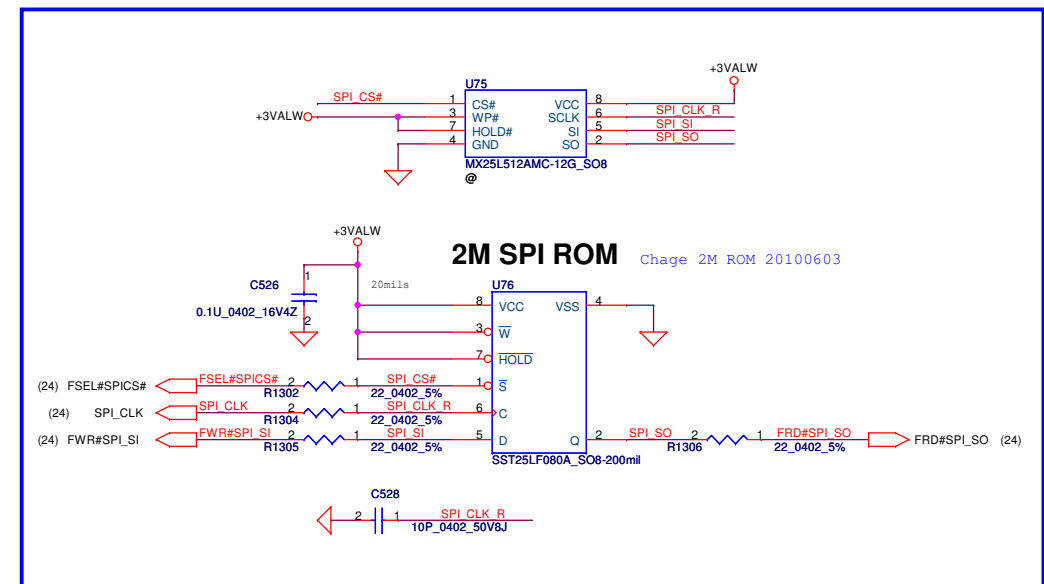
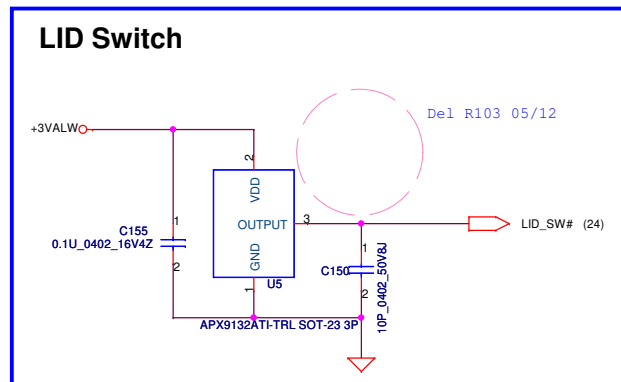
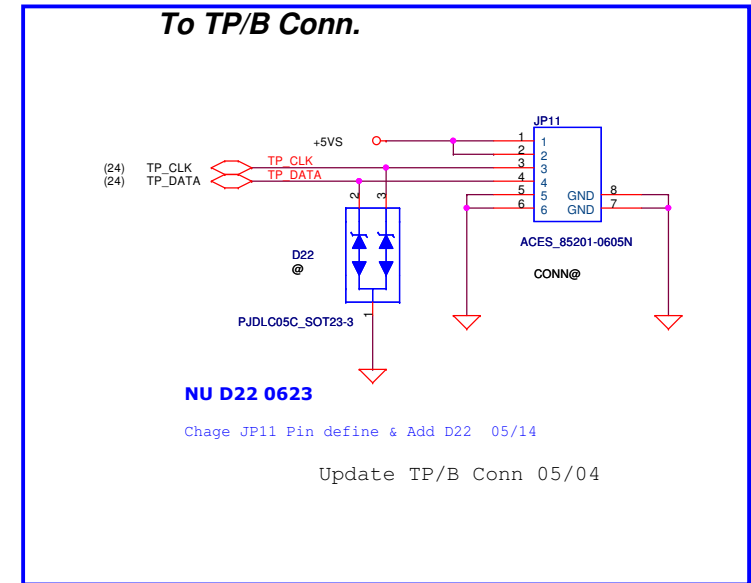
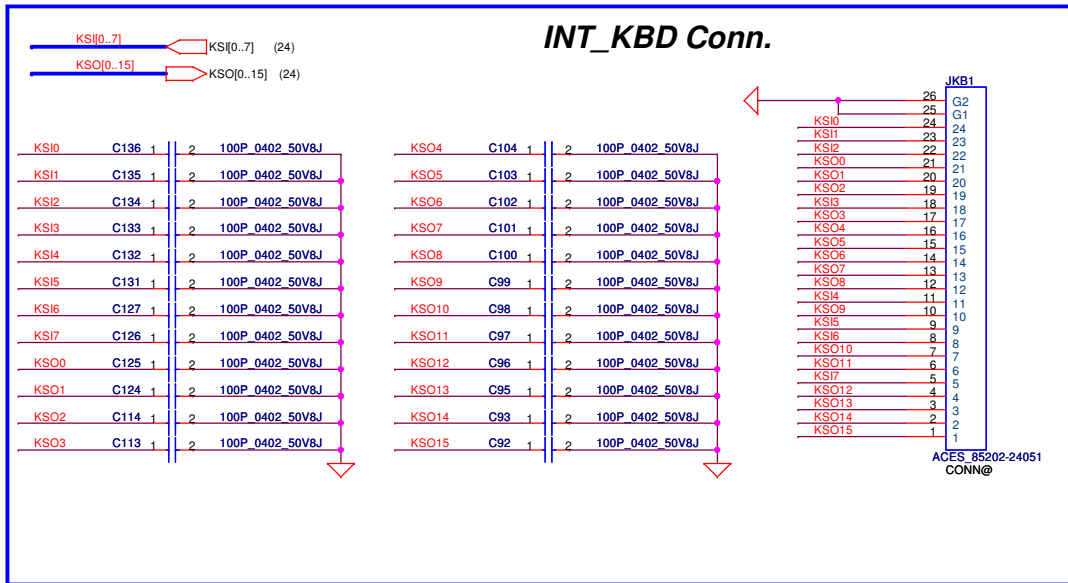
BATT\_OVP  
BATT\_TEMP  
ACIN

	KSO1	KSI1	KSI5	GPIO15
WLAN_OFF#	v	v		High
WXMIT_OFF#	v		v	High
WXMIT_OFF#	v	v		Low

	KSO1
KSI1	WL_BTN#
KSI5	3G_BTN#

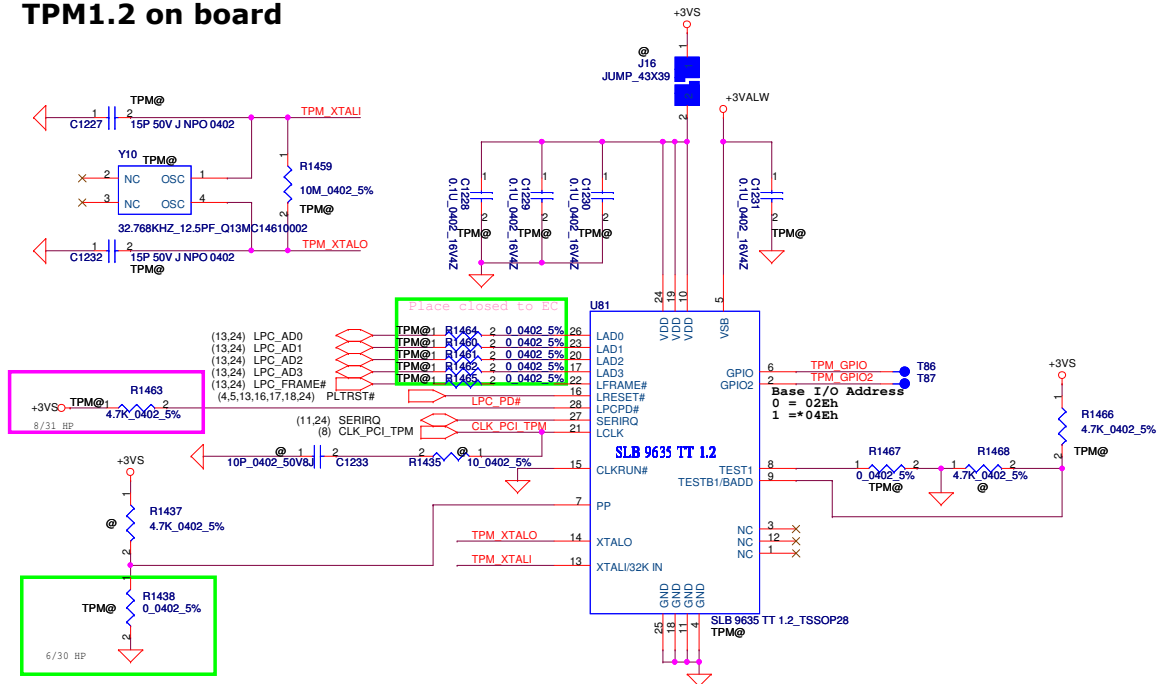


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/08/04	Deciphered Date	2007/8/18	Title	KB926
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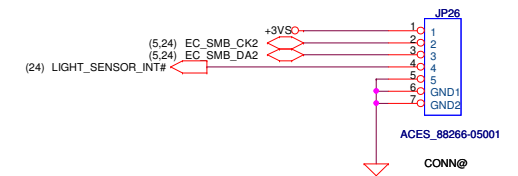


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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
				KB/TP/LID SW/ SPI	
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				B	0.2
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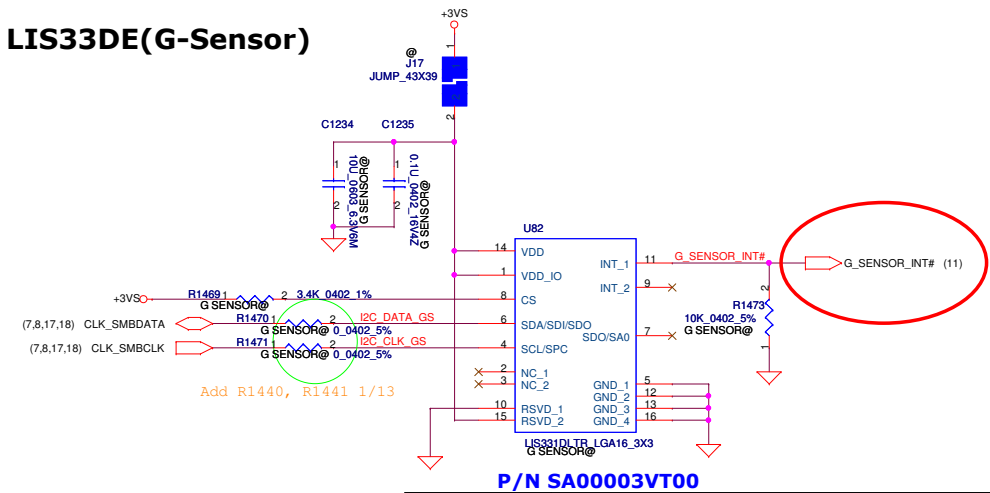
### TPM1.2 on board



### ALS (Ambient Light Sensor)

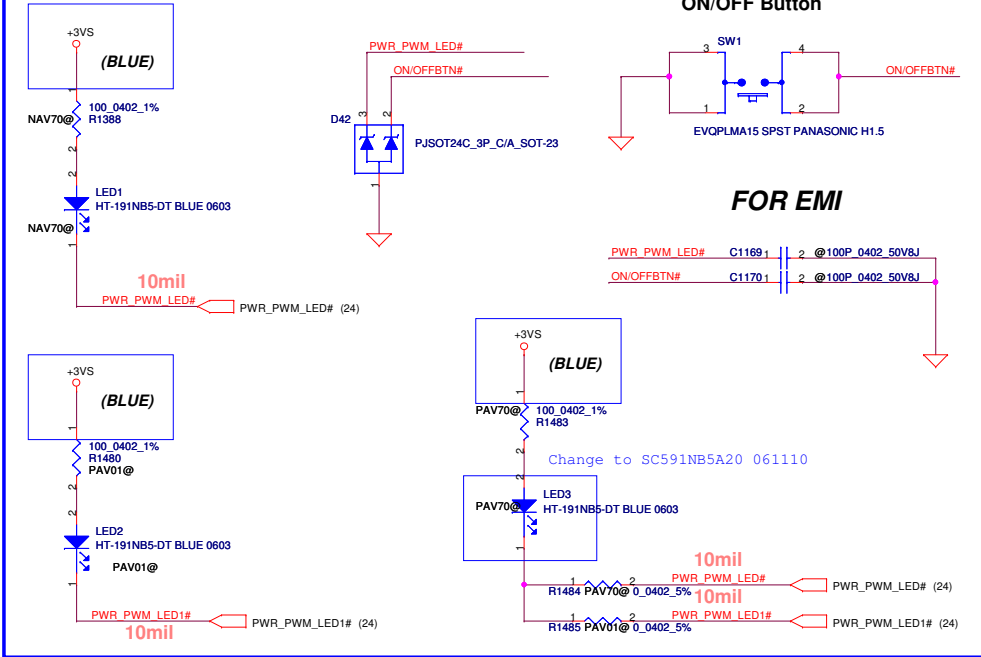


### ST LIS33DE(G-Sensor)

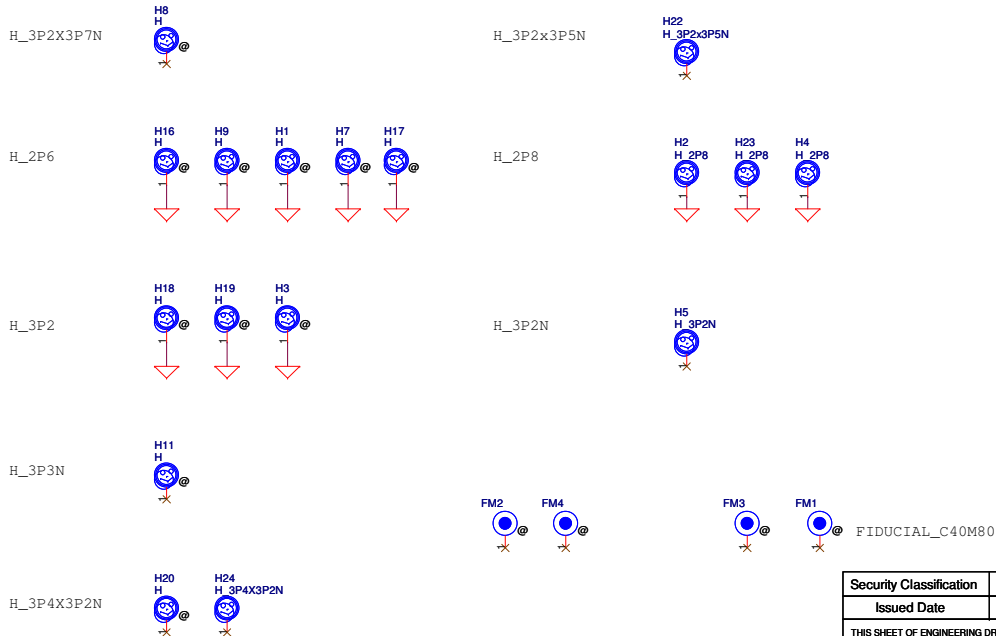
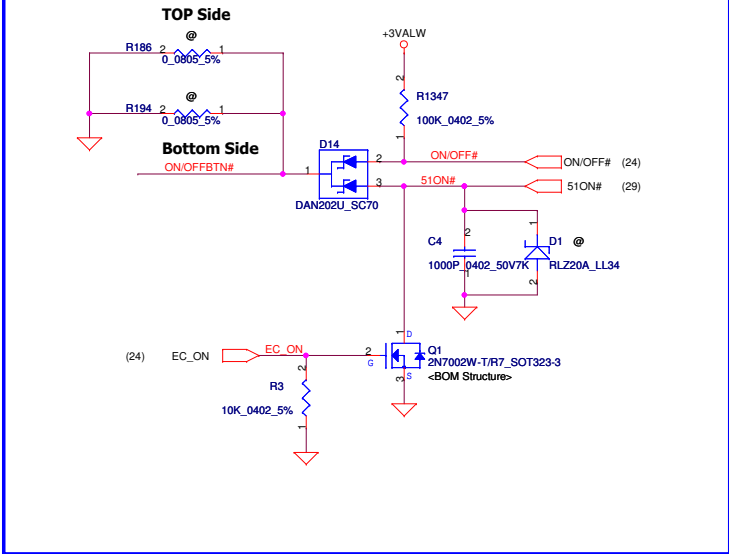


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Issued Date	2008/09/15	Deciphered Date	2009/12/31	Compal Electronics, Inc.	
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				Size	Document Number
Date: Thursday, July 01, 2010				Sheet	26 of 39

Add For NAV50 07/06  
09/03 Change +5VS to +3VS



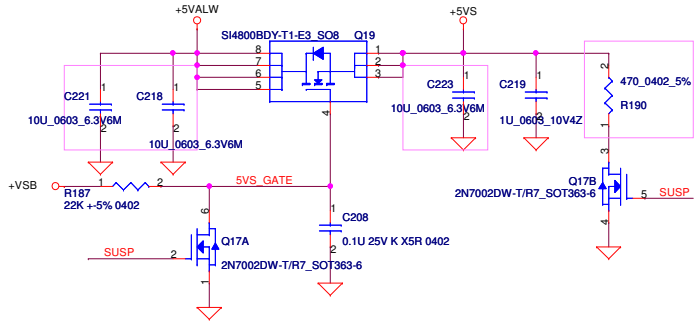
### Power Button Logic



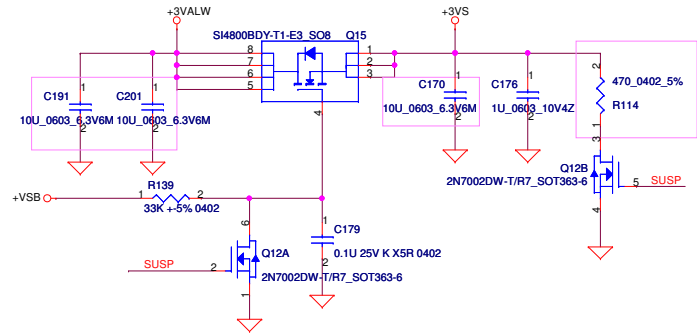
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2006/08/04	Deciphered Date	2007/8/18	Title <b>ON/OFF /SCREW</b>		
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Change R51 R57 R70 R63 R317 R114 R190 to 0402 SIZE 04/30  
 Change C221 C218 C223 C 191 C201 C170 C392 C393 C394 to 0603 SIZE 04/30

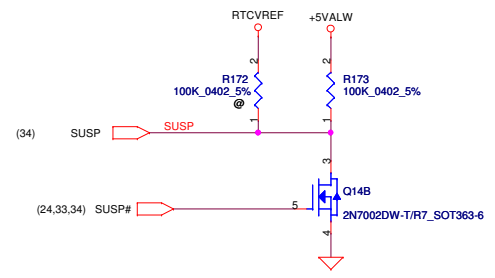
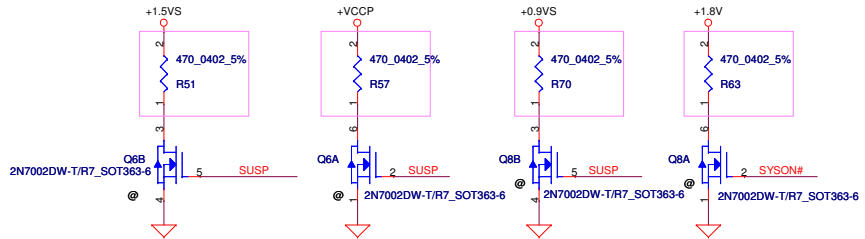
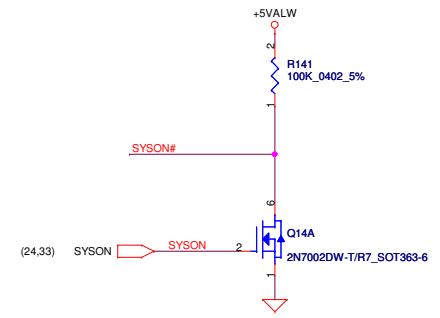
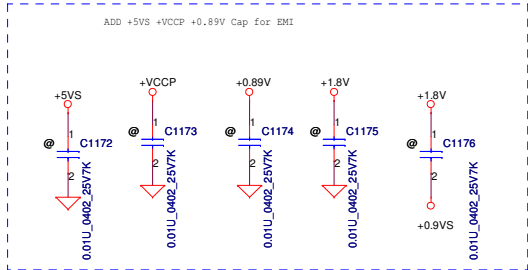
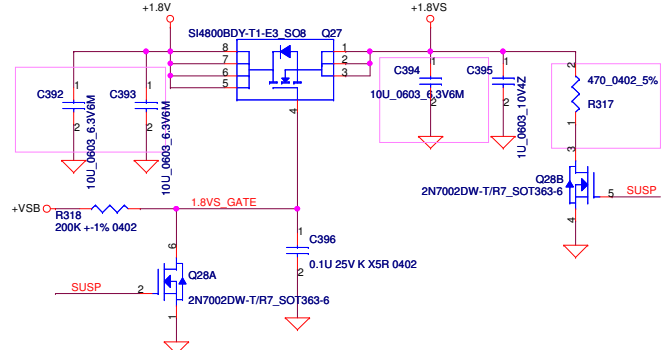
**+5VALW TO +5VS**



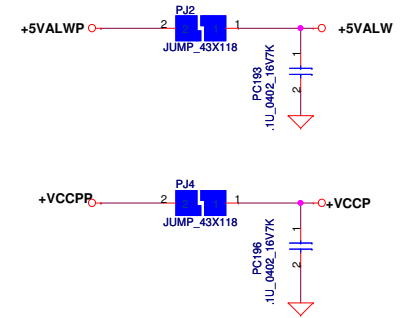
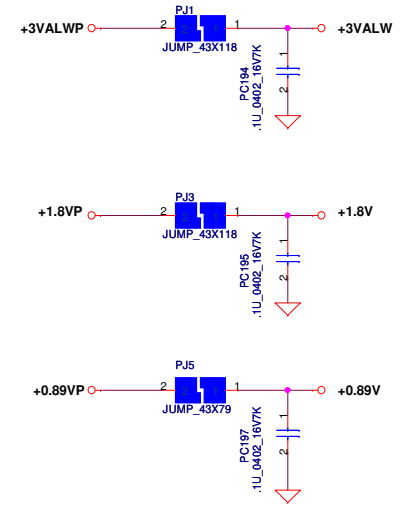
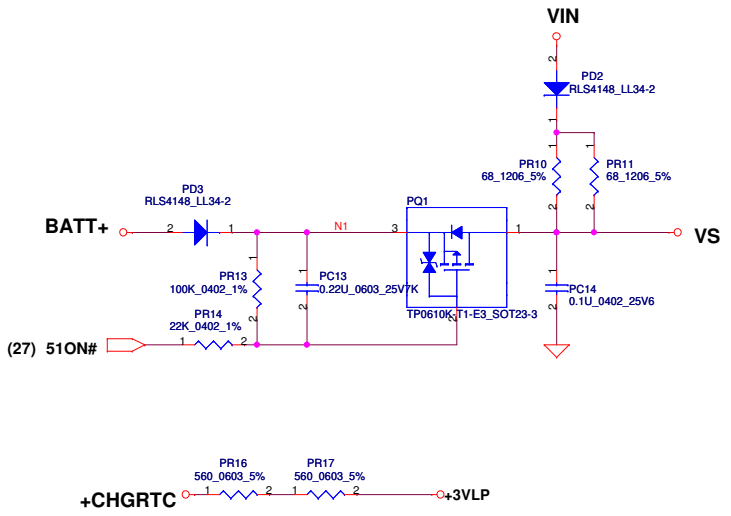
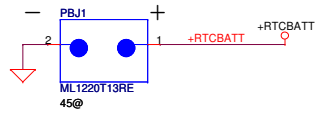
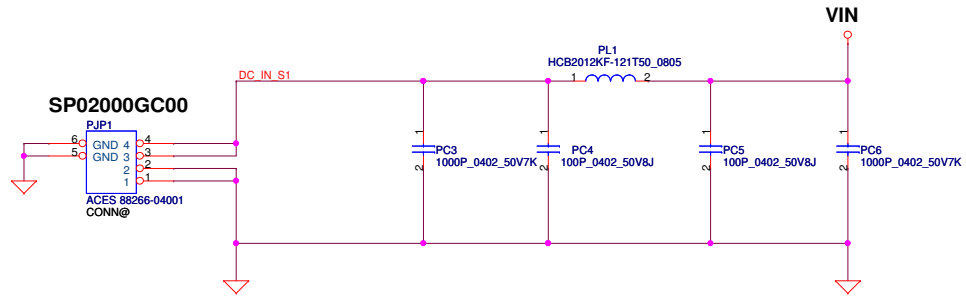
**+3VALW TO +3VS**



**+1.8V to +1.8VS**



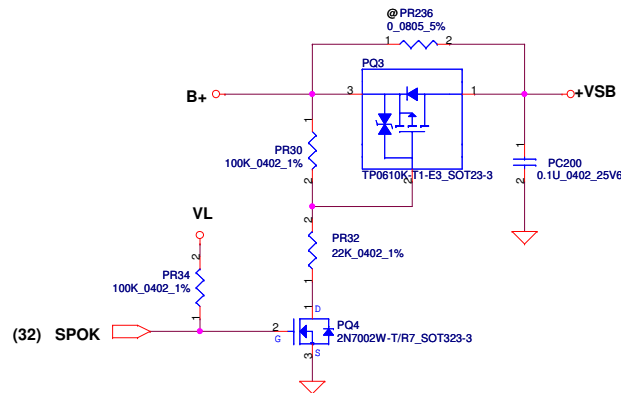
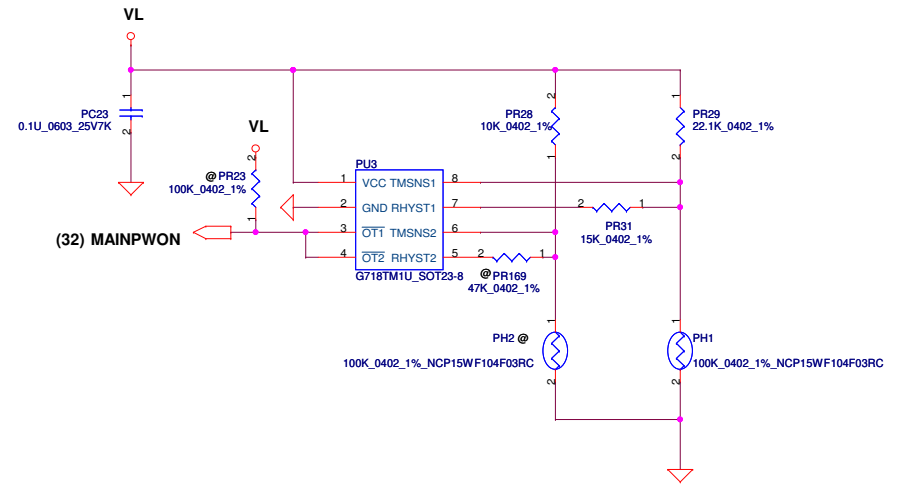
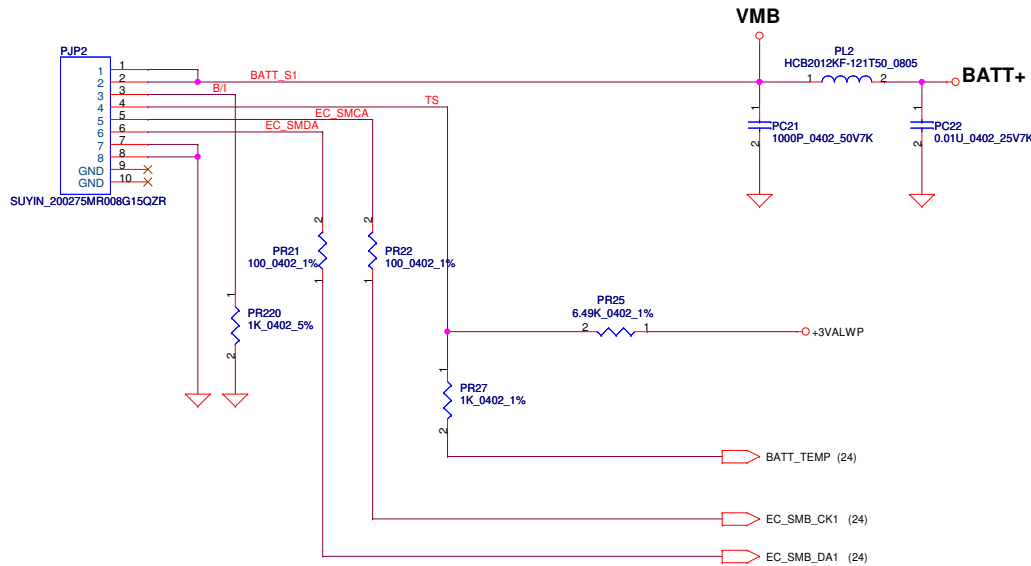
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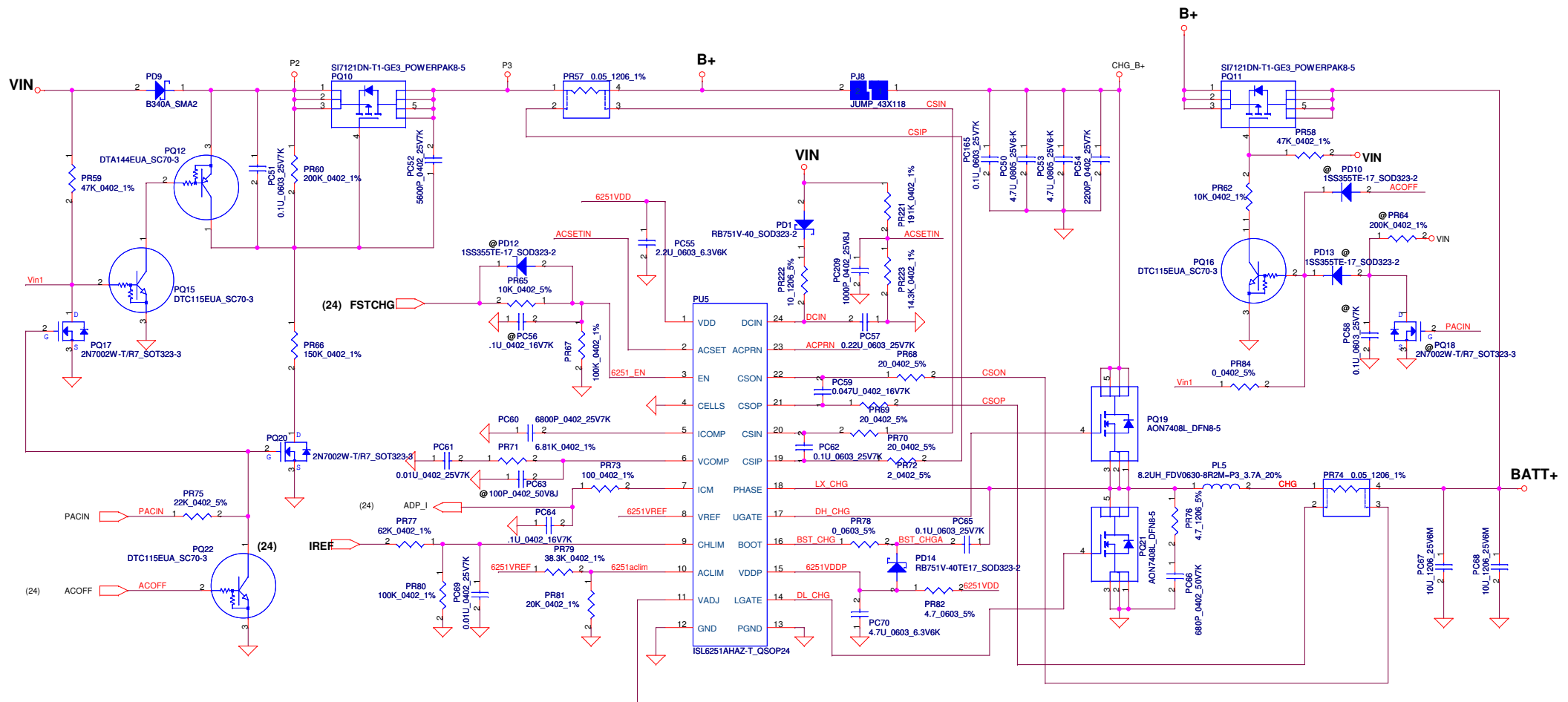
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PH1 under CPU botten side :  
 CPU thermal protection at 92 degree C  
 Recovery at 72 degree C



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$I_{ada} = 0 \sim 1.58A (30W)$      $CP = 85\% * I_{ada}$  ;  $CP = 1.343A$

CP mode  
 $V_{acLim} = 2.39 * (20K / (20K + 38.3K)) = 0.8199V$   
 $I_{input} = (1 / 0.05) * ((0.05 * V_{acLim}) / 2.39 + 0.05)$   
 where  $V_{acLim} = 0.8199V$ ,  $I_{input} = 1.343A$

CC=0.3~1.76A  
 $I_{REF} = 1.62 * I_{charge}$   
 $I_{REF} = 0.486V \sim 2.85V$   
 3.24V ==> 2A

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

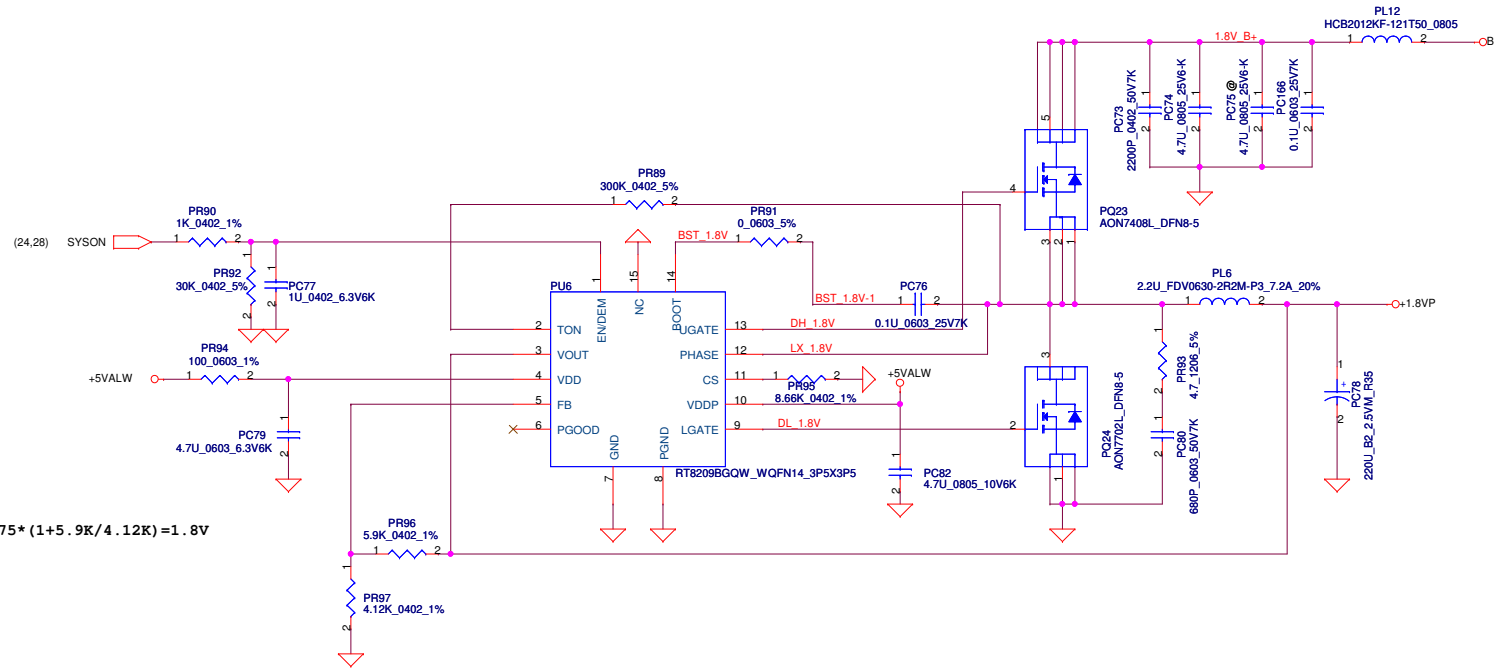
$V_{ADJ} \rightarrow V_{REF} \rightarrow 4.41V$   
 $V_{ADJ} \rightarrow \text{Ground} \rightarrow 3.59V$   
 $V_{cell} = (0.175 * V_{ADJ} + 3.99)$

(24) CALIBRATE#    PR83 15.4K\_0402\_1%    PR85 31.6K\_0402\_1%

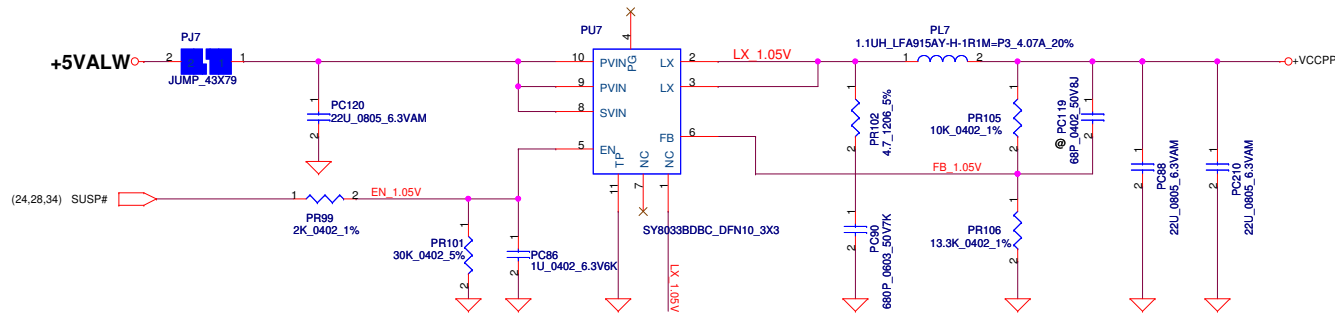
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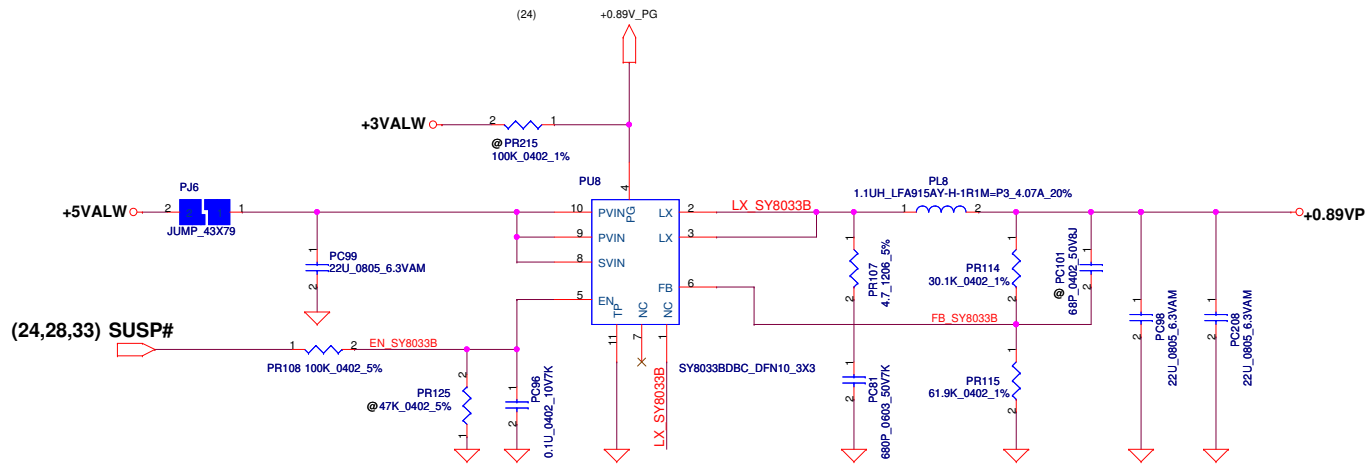


$\langle V_o=1.8V \rangle$   $V_{FB}=0.75V$   
 $V_o=V_{FB} * (1+PR96/PR97)=0.75 * (1+5.9K/4.12K)=1.8V$   
 $F_{sw}=328KHz$

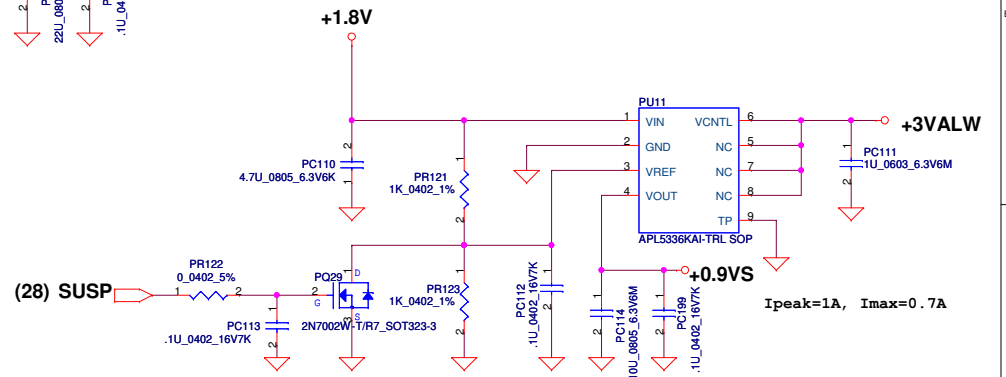
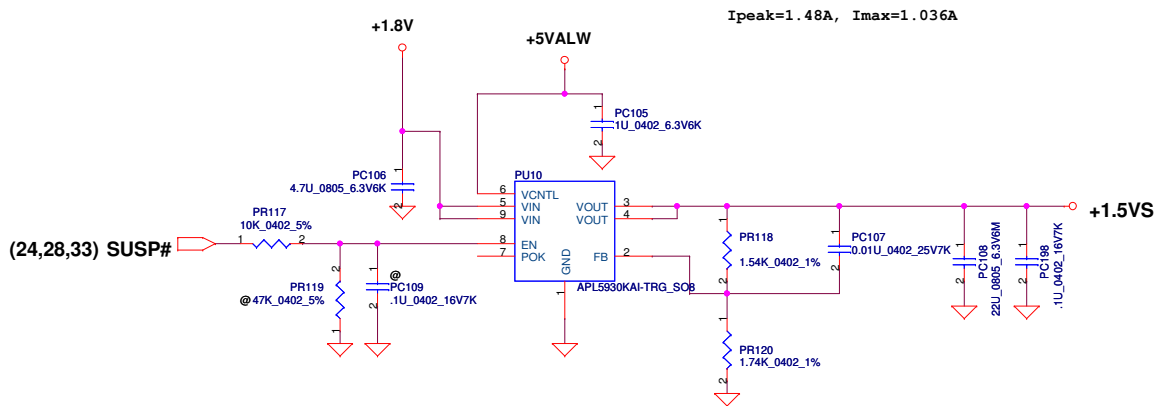


$\langle V_o=1.05V \rangle$   $V_{FB}=0.6V$   
 $V_o=V_{FB} * (1+PR105/PR106)=0.6 * (1+124K/61.9K)=1.05V$   
 $I_{peak}=3.124A$ ,  $I_{max}=2.187A$

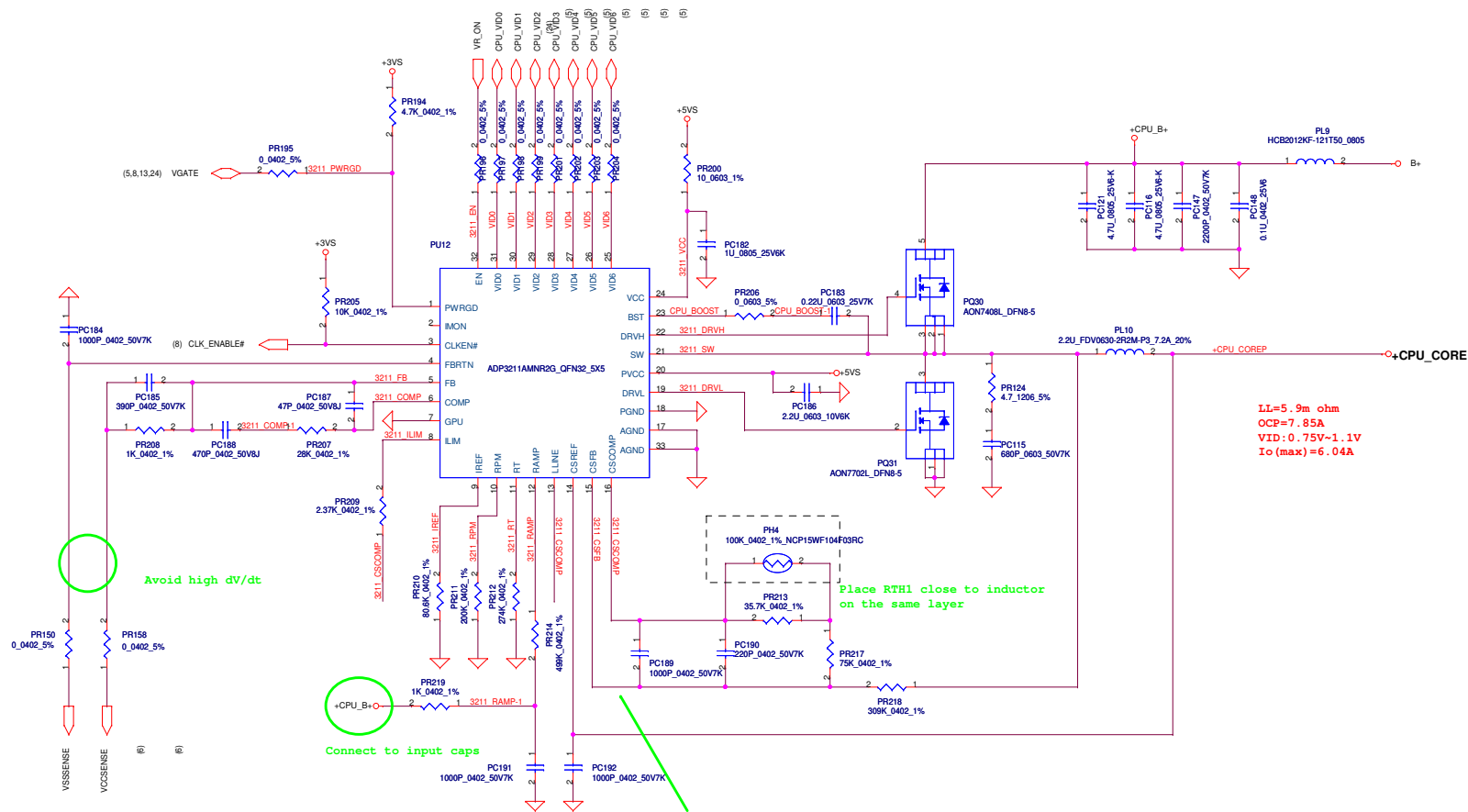
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$V_o = 0.89V$      $V_{FB} = 0.6V$   
 $V_o = V_{FB} * (1 + PR114 / PR115) = 0.6 * (1 + 30.1K / 61.9) = 0.89V$   
 $I_{peak} = 2.64A, I_{max} = 1.848A$



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Avoid high dV/dt

Connect to input caps

Place RTH1 close to inductor on the same layer

Shortest the net trace

LL=5.9m ohm  
 OCP=7.85A  
 VID: 0.75V~1.1V  
 Io(max)=6.04A

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	add PR84	For design change	0.1	30	add PR84 (SD028000080 , S RES 1/16W 0 +-5% 0402)	2010.4.10	EVT
2	Change power solution	For design change	0.1	32	Change PU7 from SA000031D00(S IC RT8209BGQW WQFN 14P PWM) to SA00003RU00(S IC SY8033BDBC DFN 10P SINGLE BUCK)	2010.4.12	EVT
3	Change SY8033B Pin1 net	For design change	0.1	32,33	Change SY8033B Pin1 connect Pin2 & Pin3	2010.4.13	EVT
4	Change PC101 & PC119	For design change	0.1	32,33	Change PC101 & PC119 to SE071680J80 (S CER CAP 68P 50V J NPO 0402)	2010.4.13	EVT
5	Change PR105	For design change	0.1	32	Change PR105 from SD034100200(S RES 1/16W 10K +-1% 0402 ) to SD034100280 (S RES 1/16W 10K +-1% 0402 )	2010.5.13	DVT
6	Change PC30 & PC32 to non-pop	For cost down plan	0.1	32		2010.6.1	PVT
7	Change PL3,PL4,PL5,PL6,PL7,PL8,PL10	For TMP choke shortage issue	0.1	32	Change PL3,PL4,PL5 from SH00000JI00 to SH00000BS00 Change PL6,PL10 from SH00000FD10 to SH000000700 Change PL7,PL8 from SH00000J300 to SH000007N00	2010.6.1	PVT
8	Change PD10.PD13.PC58.PR64. PQ18 to non-pop Change PR84 to pop	For cost down plan	0.1	31		2010.6.11	PVT
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