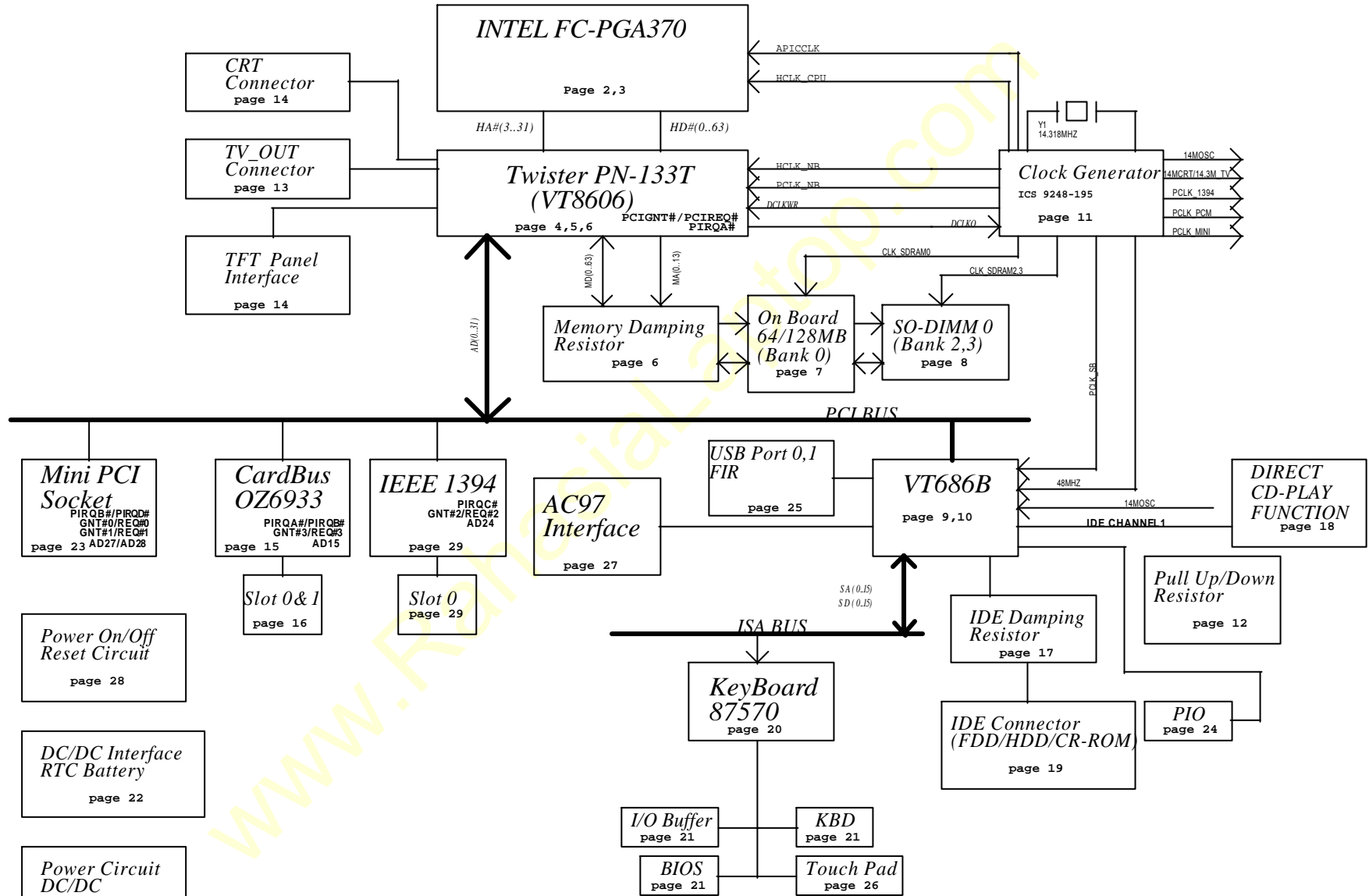
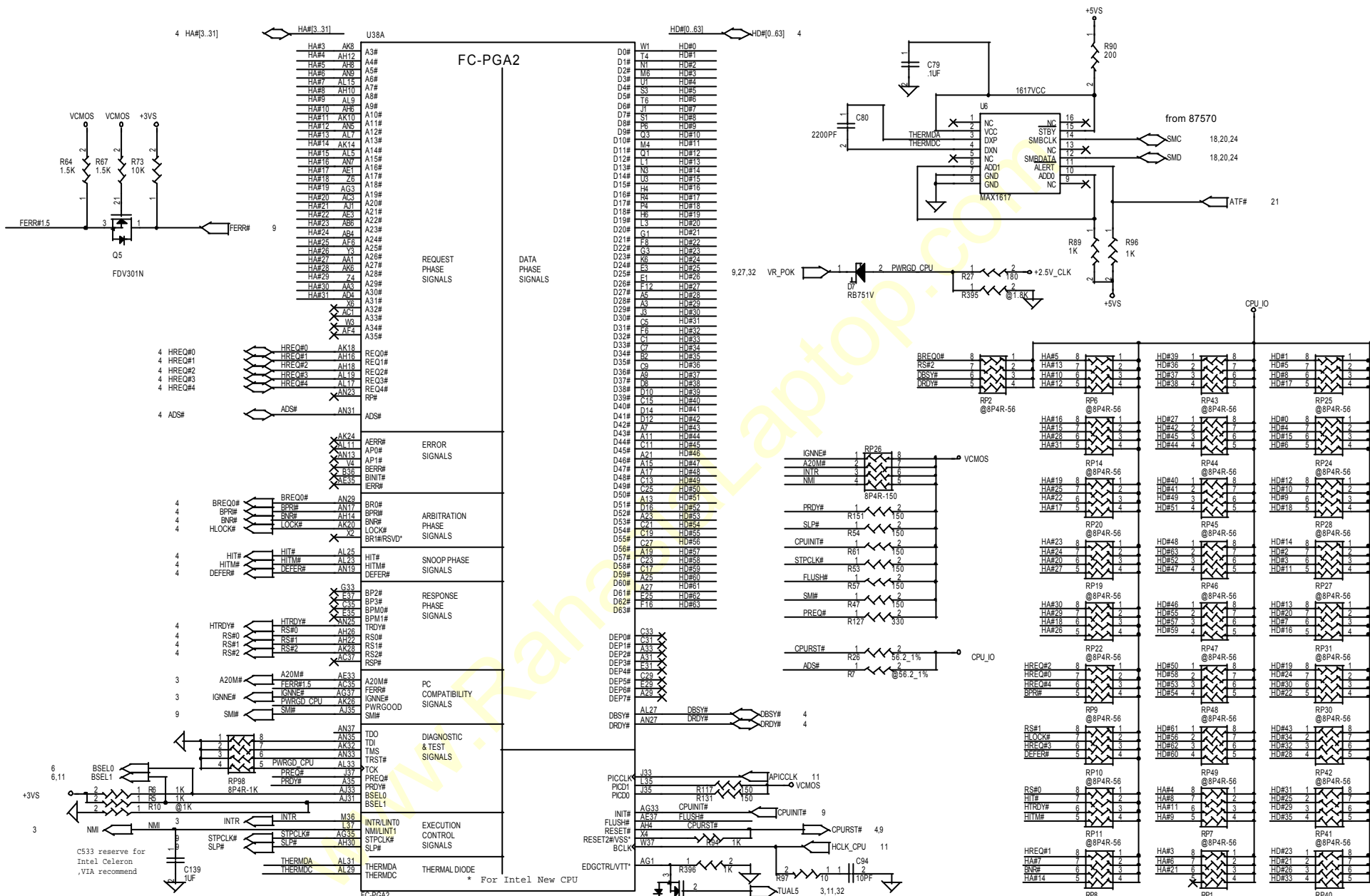


Model Name : CY23 LA-1281 Rev:2.0



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SELPSBIT[0]	STSEM BUS FREQUENCY
00	66MHZ
01	100MHZ
10	RESERVED
11	133MHZ

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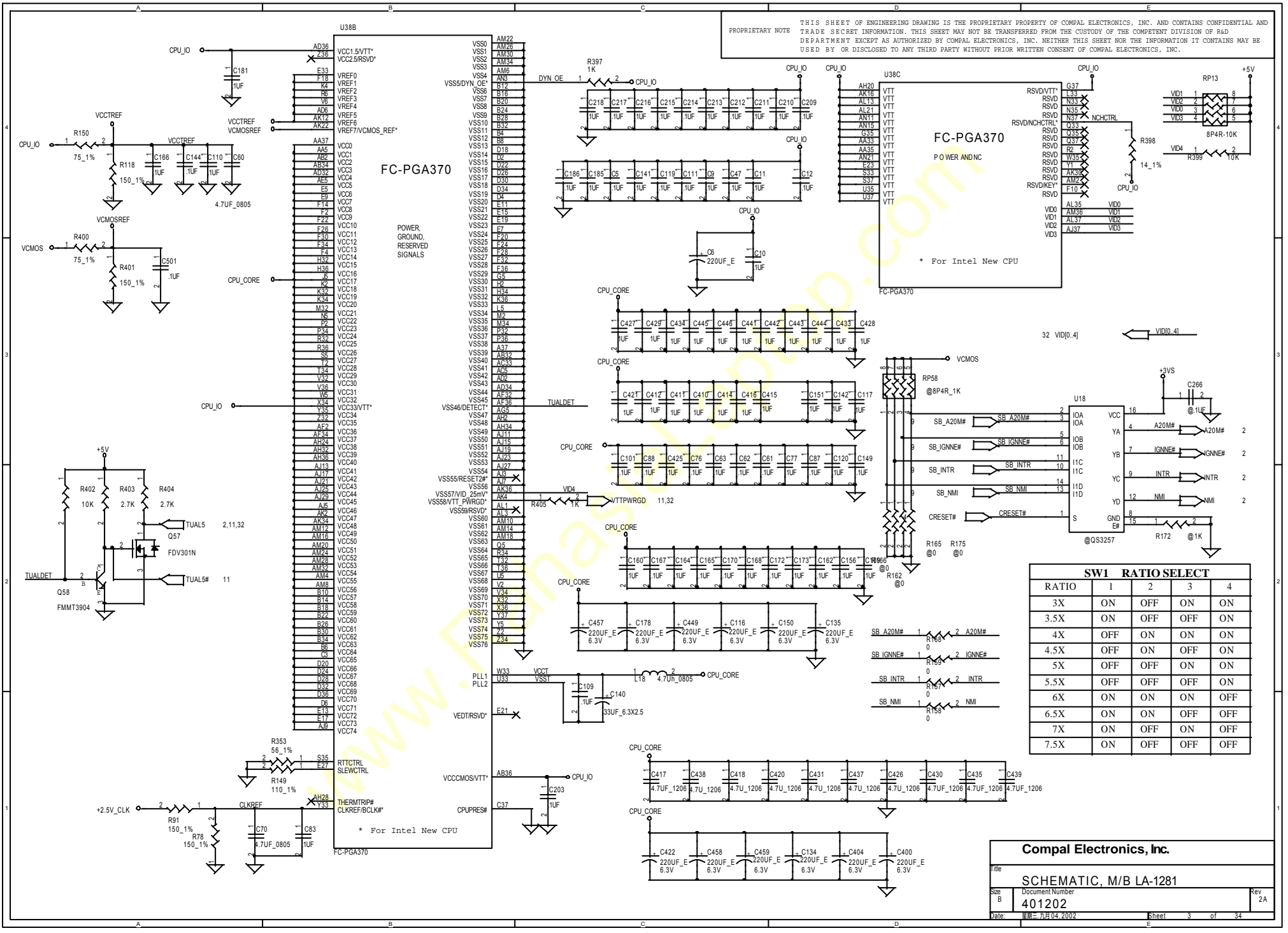
Doc Number: **401202**

Date: 星期三, 2002年04月02日

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SW1 RATIO SELECT				
RATIO	1	2	3	4
3X	ON	OFF	ON	ON
3.5X	ON	OFF	OFF	ON
4X	OFF	ON	ON	ON
4.5X	OFF	ON	OFF	ON
5X	OFF	OFF	ON	ON
5.5X	OFF	OFF	OFF	ON
6X	ON	ON	ON	OFF
6.5X	ON	ON	OFF	OFF
7X	ON	OFF	ON	OFF
7.5X	ON	OFF	OFF	OFF

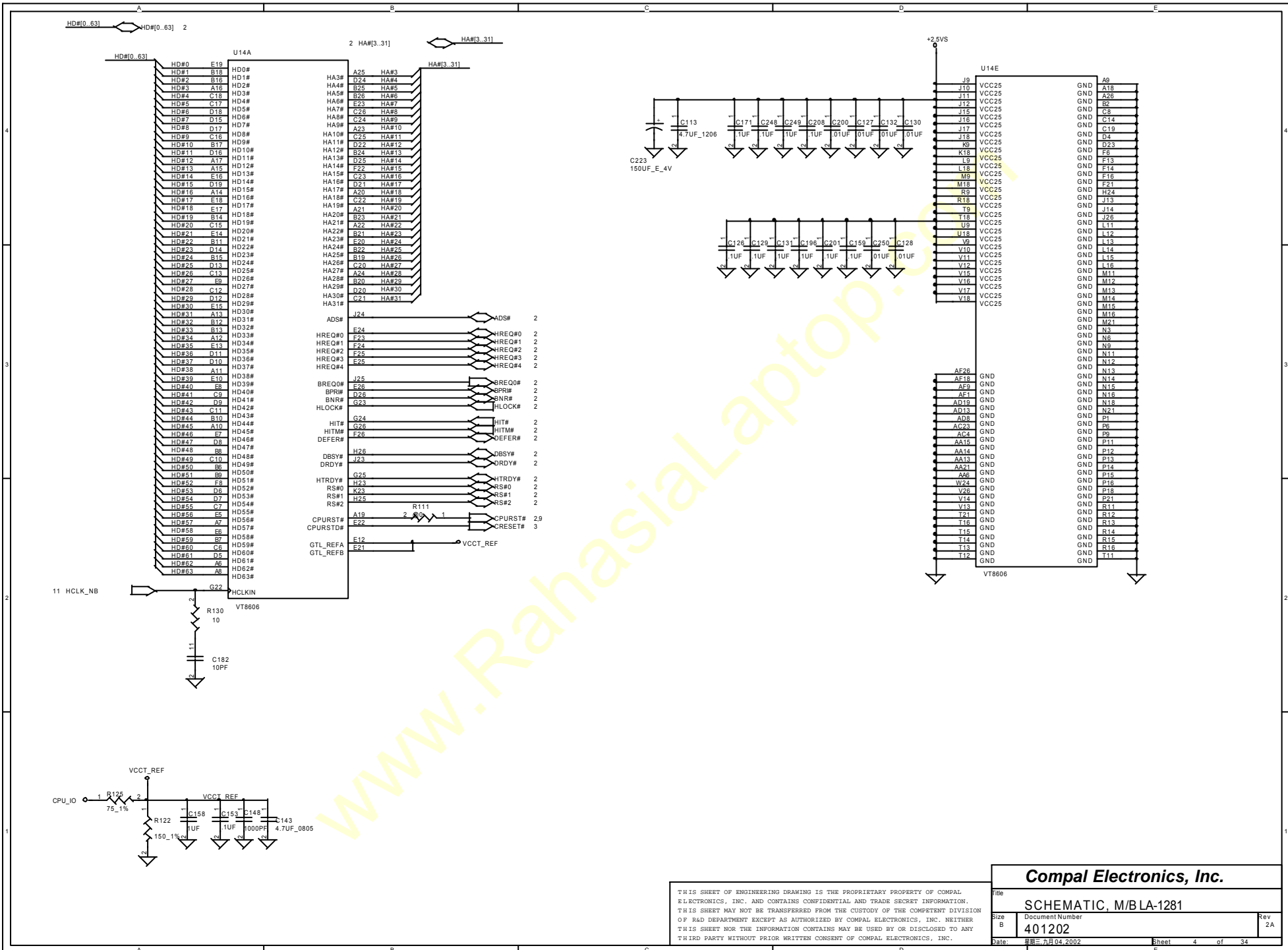
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File: SCHEMATIC, M/B LA-1281

Rev: 2A

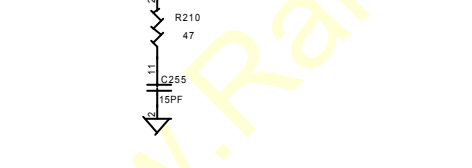
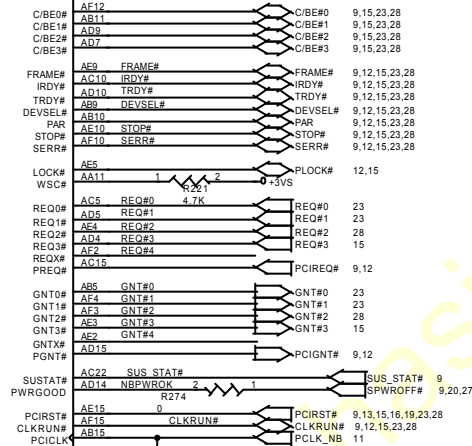
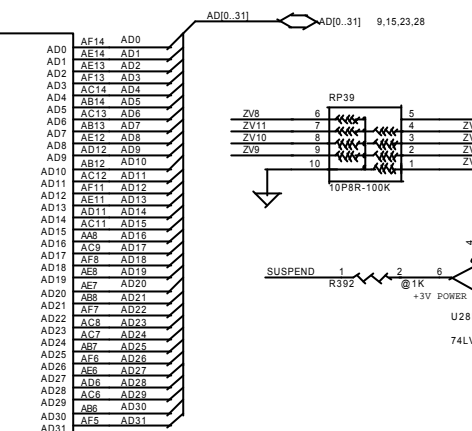
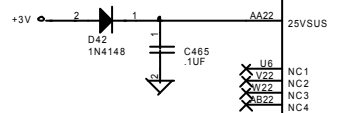
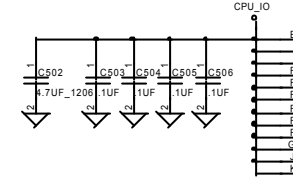
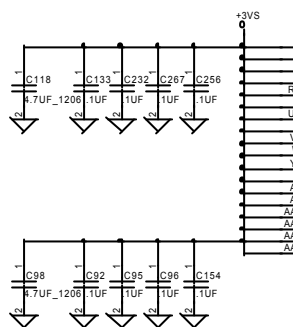
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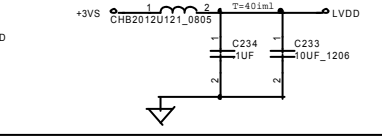
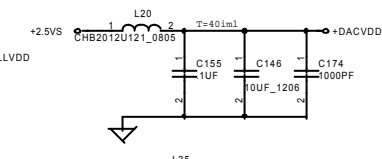
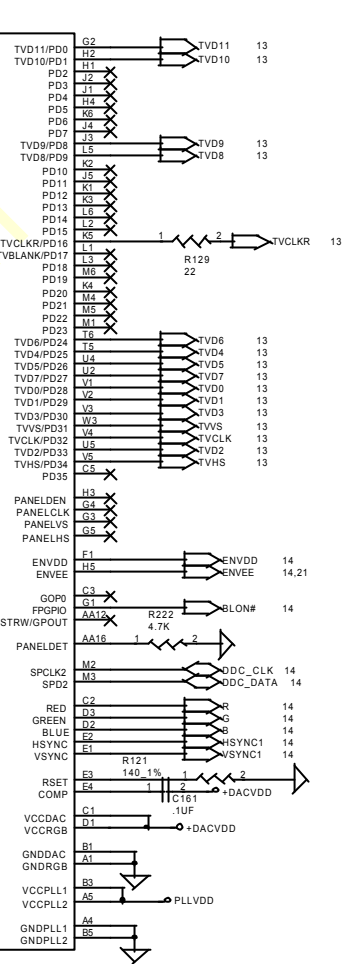
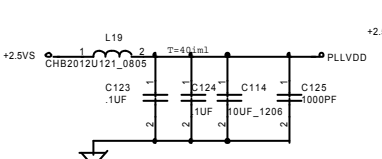
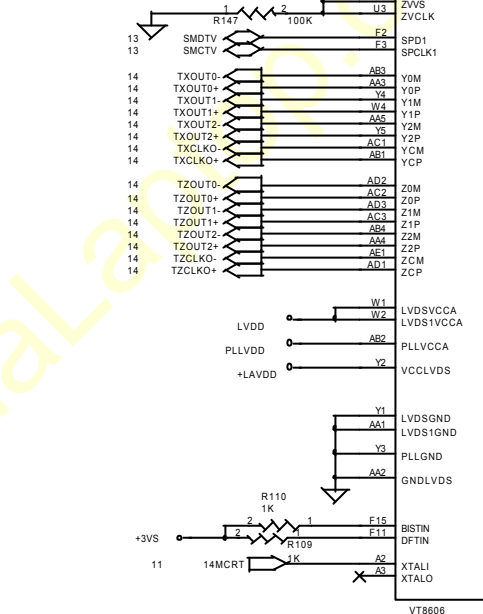
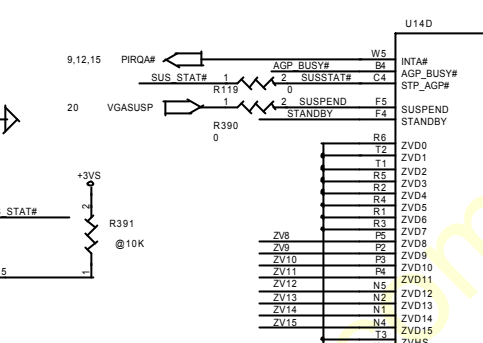
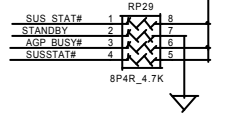


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PCI REQASSIGNMENT	
REQ#0	MiniPCI(Compal)
REQ#1	MINIPCI
REQ#2	1394
REQ#3	PCMCIA CONTROLLER
REQ#4	NO USED



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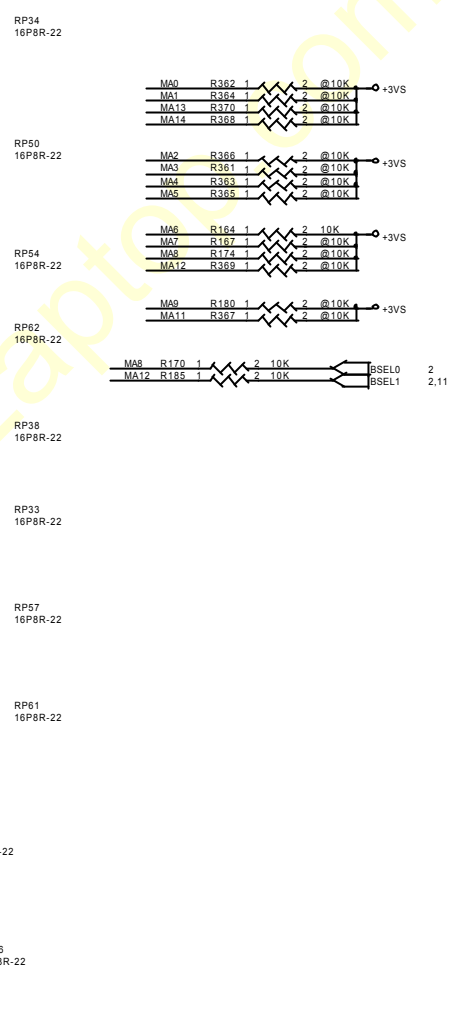
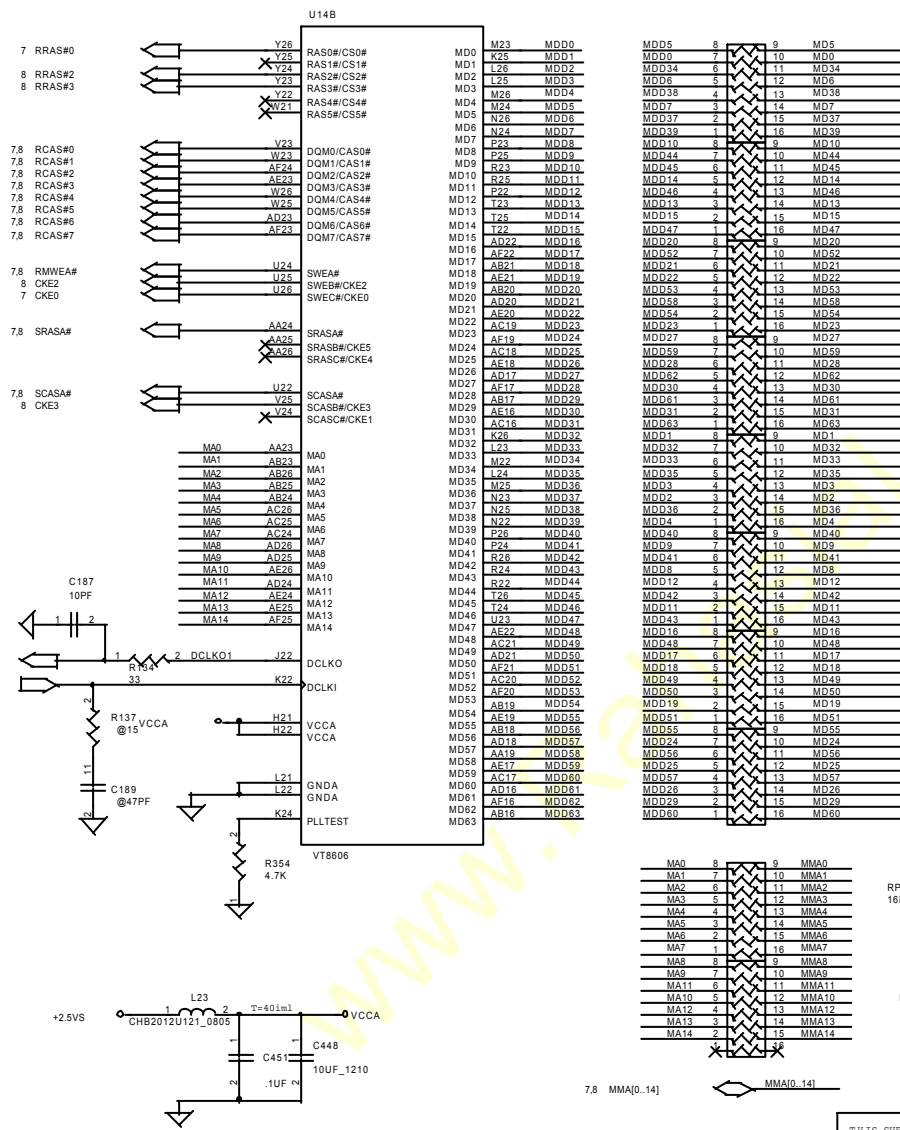
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MD[0..63]  $\diamond$  MD[0..63] 7,8



Strap	Description	Setting
MA12,8	CPU Clock Frequency	01=100MHz 11=133MHz 00=66MHz
MA2	PCI Base Address Mapping	0=Map0 1=Map1
MA3	Graphic IO Enable/Disable	0=Enable 1=Disable
MA4	PCI Interrupt	0=Enable 1=Disable
MA7	Graphic Test Mode	0=Normal 1=Test
MA9	VGA Clock Select	0=PLL 1=External
MA11	IOQ Level	0=4Level 1=1Level
MA0,1,13,14	Panel Type	

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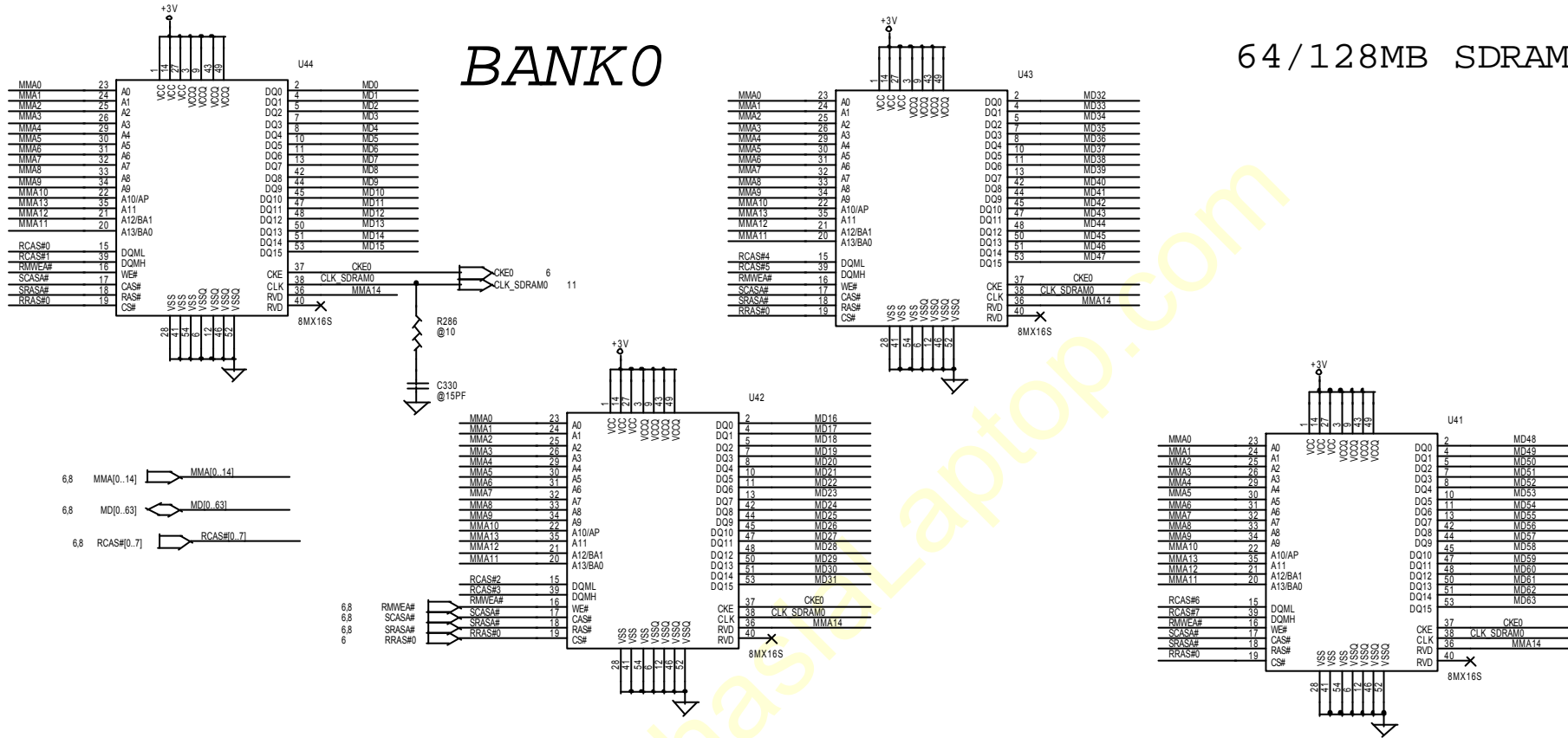
Rev: 2A

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# BANK 0

## 64/128MB SDRAM



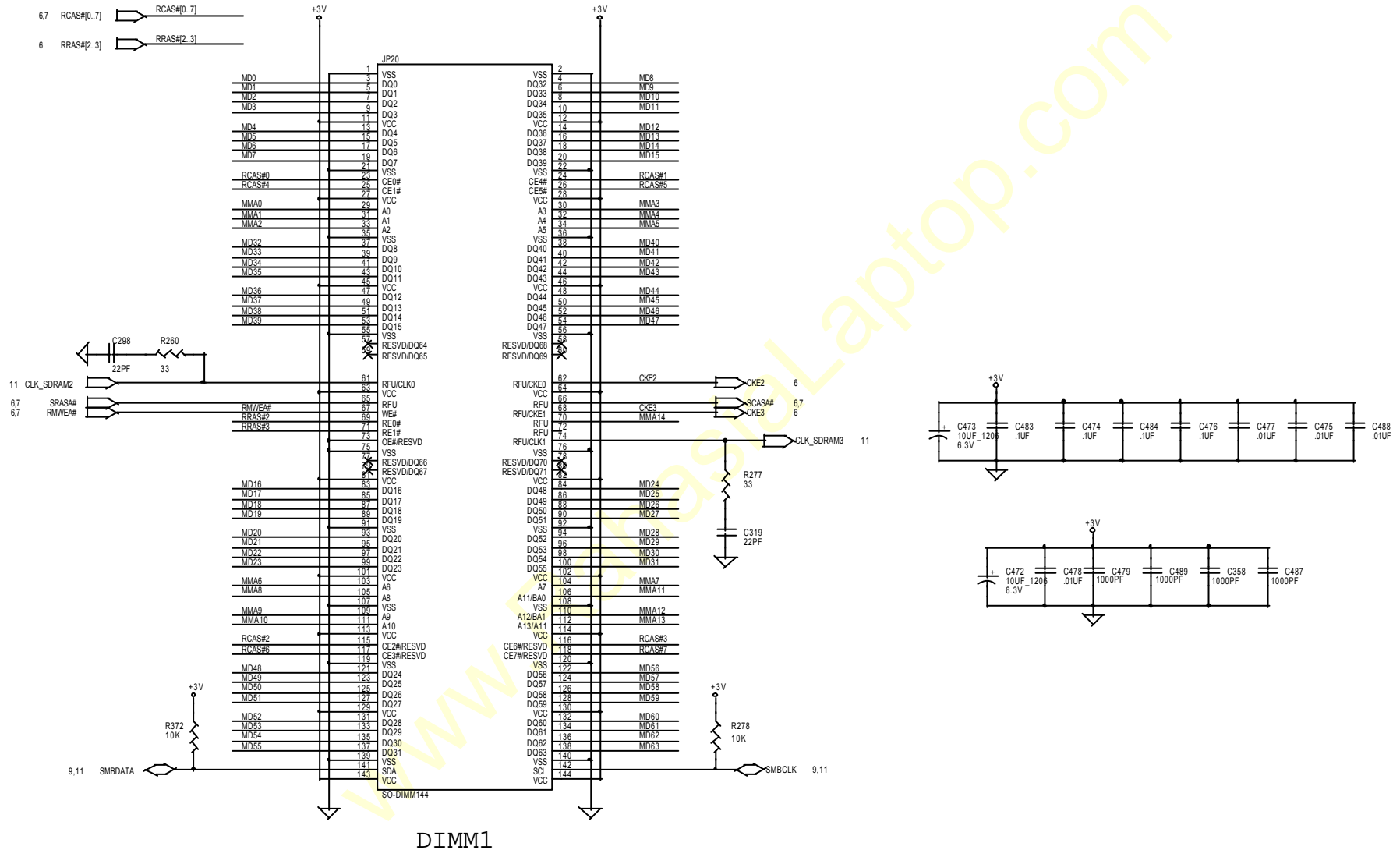
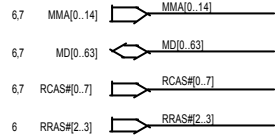
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SO-DIM 144 PINS  
RAM MODULE CONN.

# BANK 2 / 3



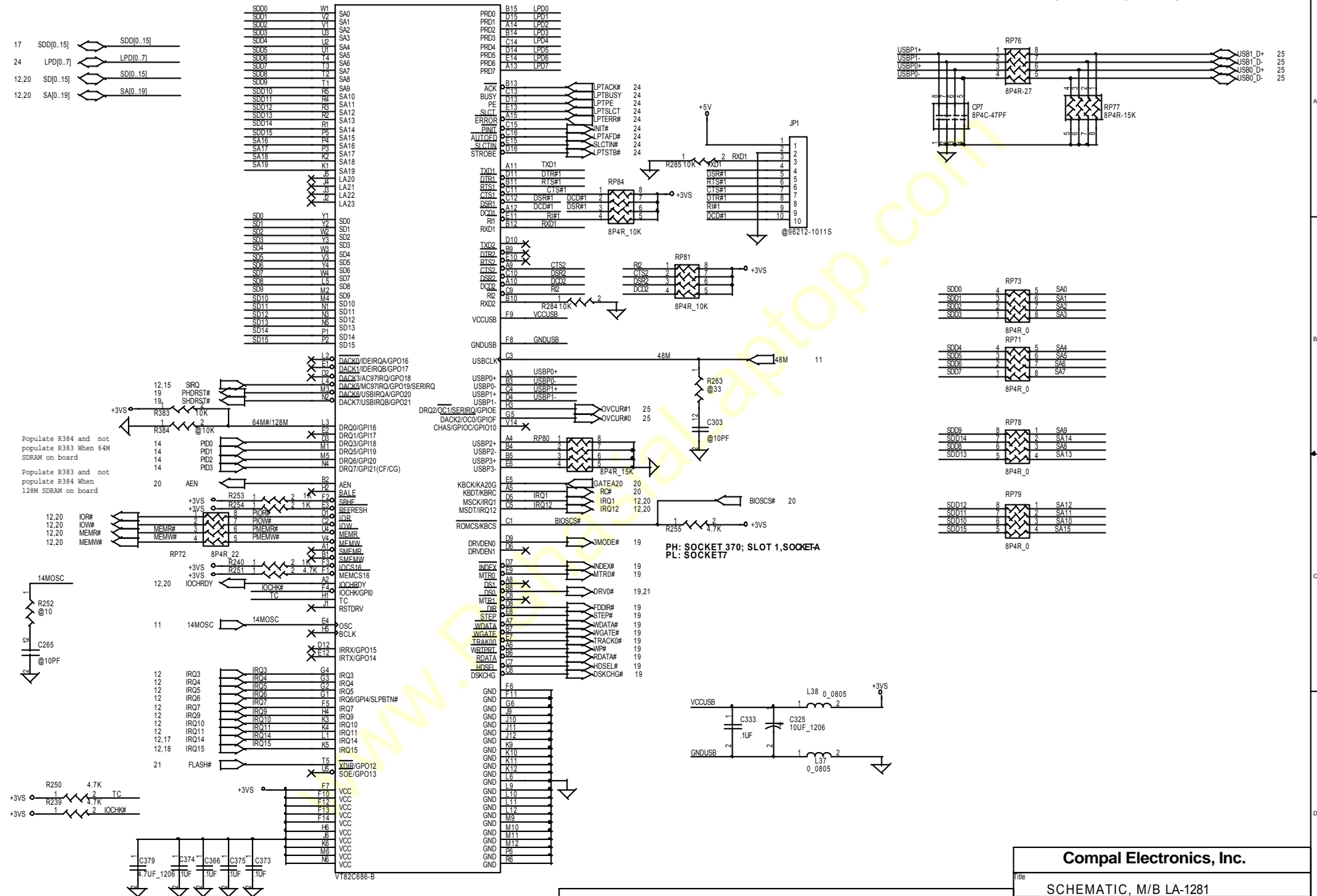
DIMM1

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Populate R384 and not populate R383 When 64M SDRAM on board

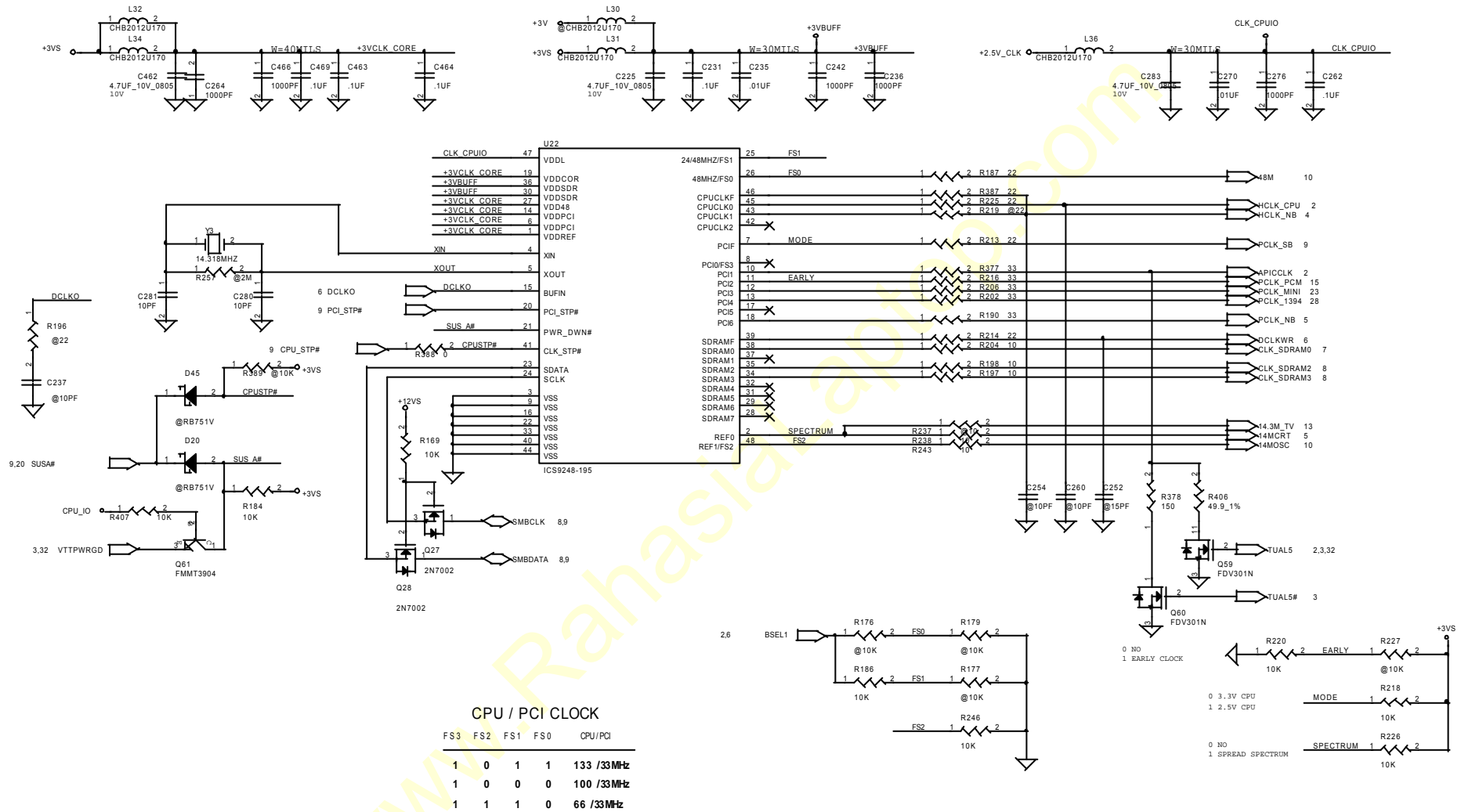
Populate R383 and not populate R384 When 128M SDRAM on board

PH: SOCKET 370; SLOT 1, SOCKET A PL: SOCKET 17

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# CLOCK GENERATOR & BUFFER

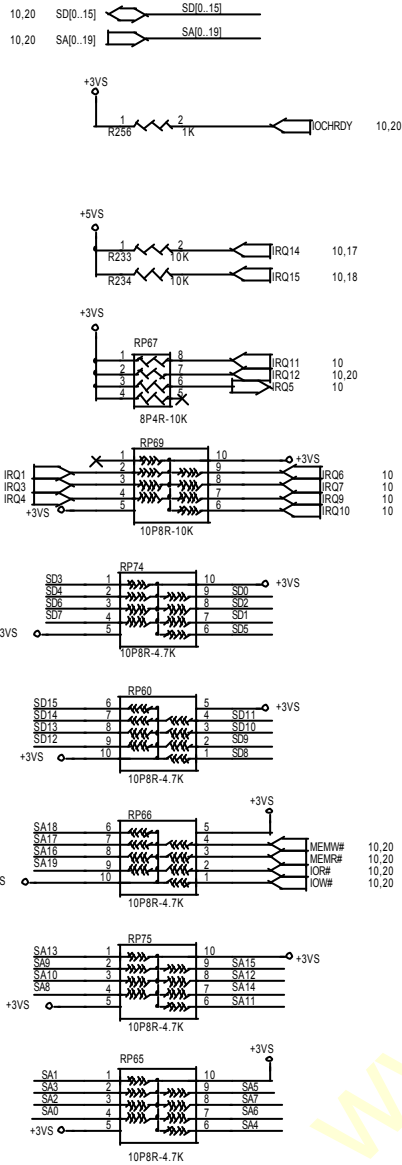


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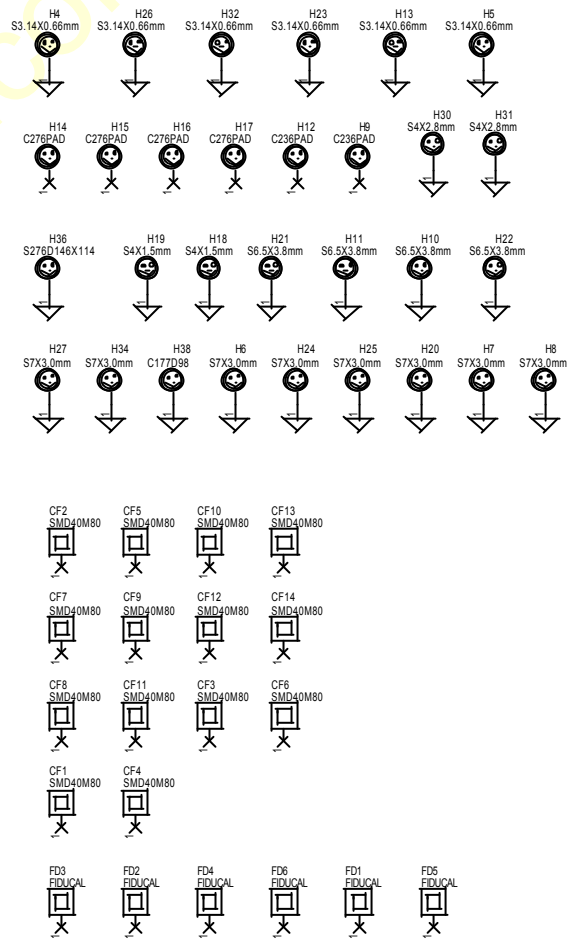
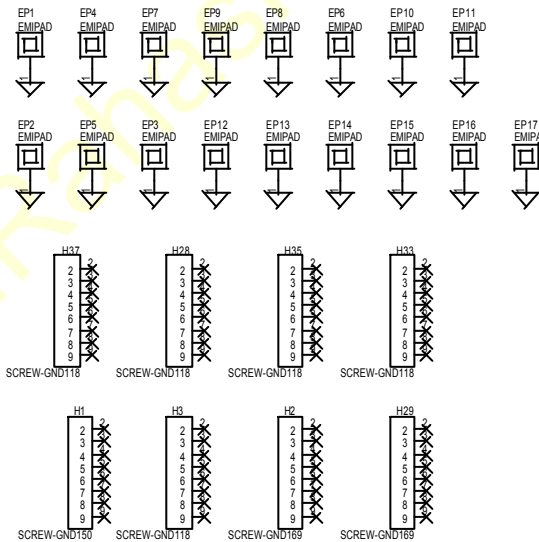
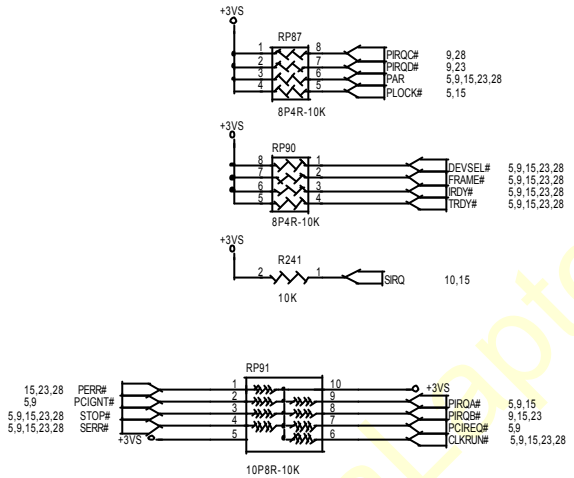
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# ISA BUS Pullup



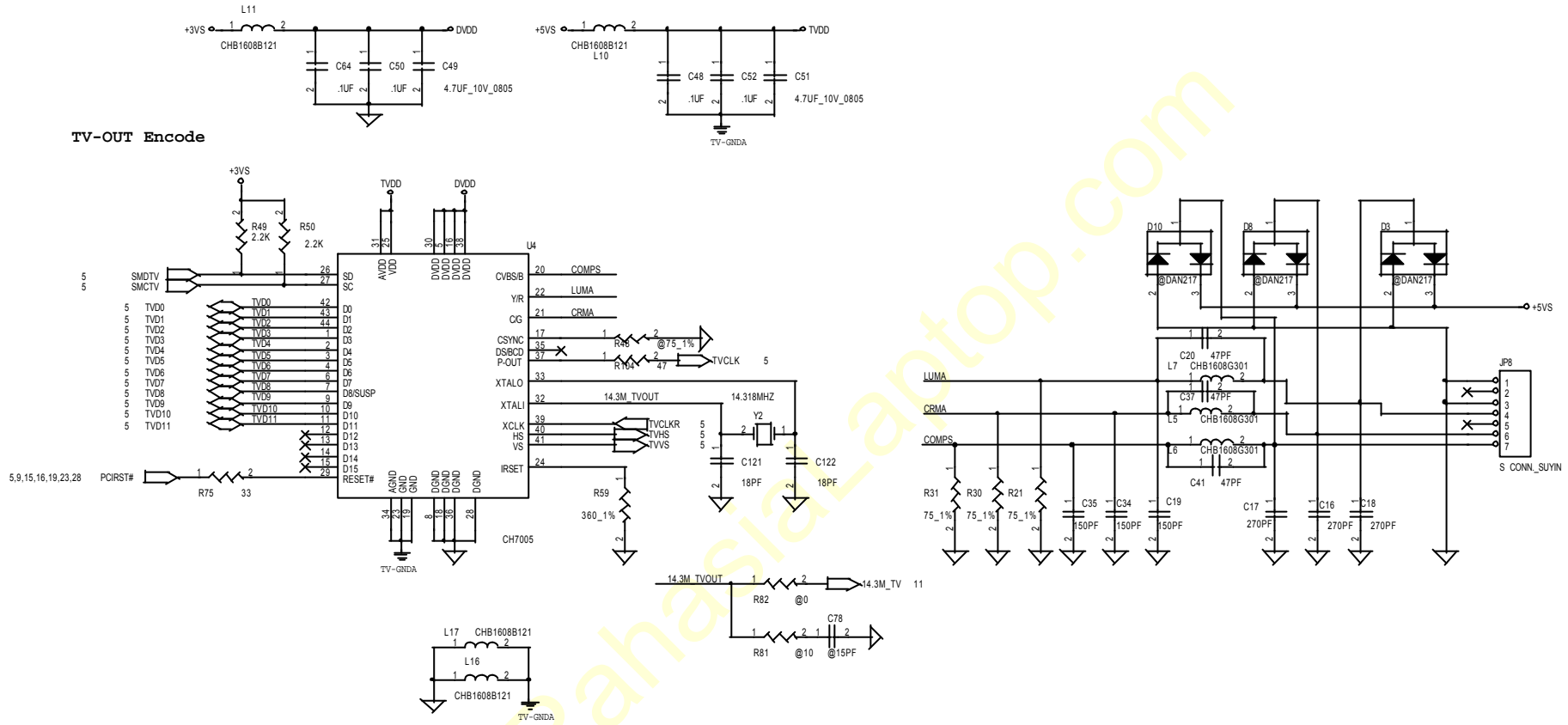
# PCI BUS Pullup



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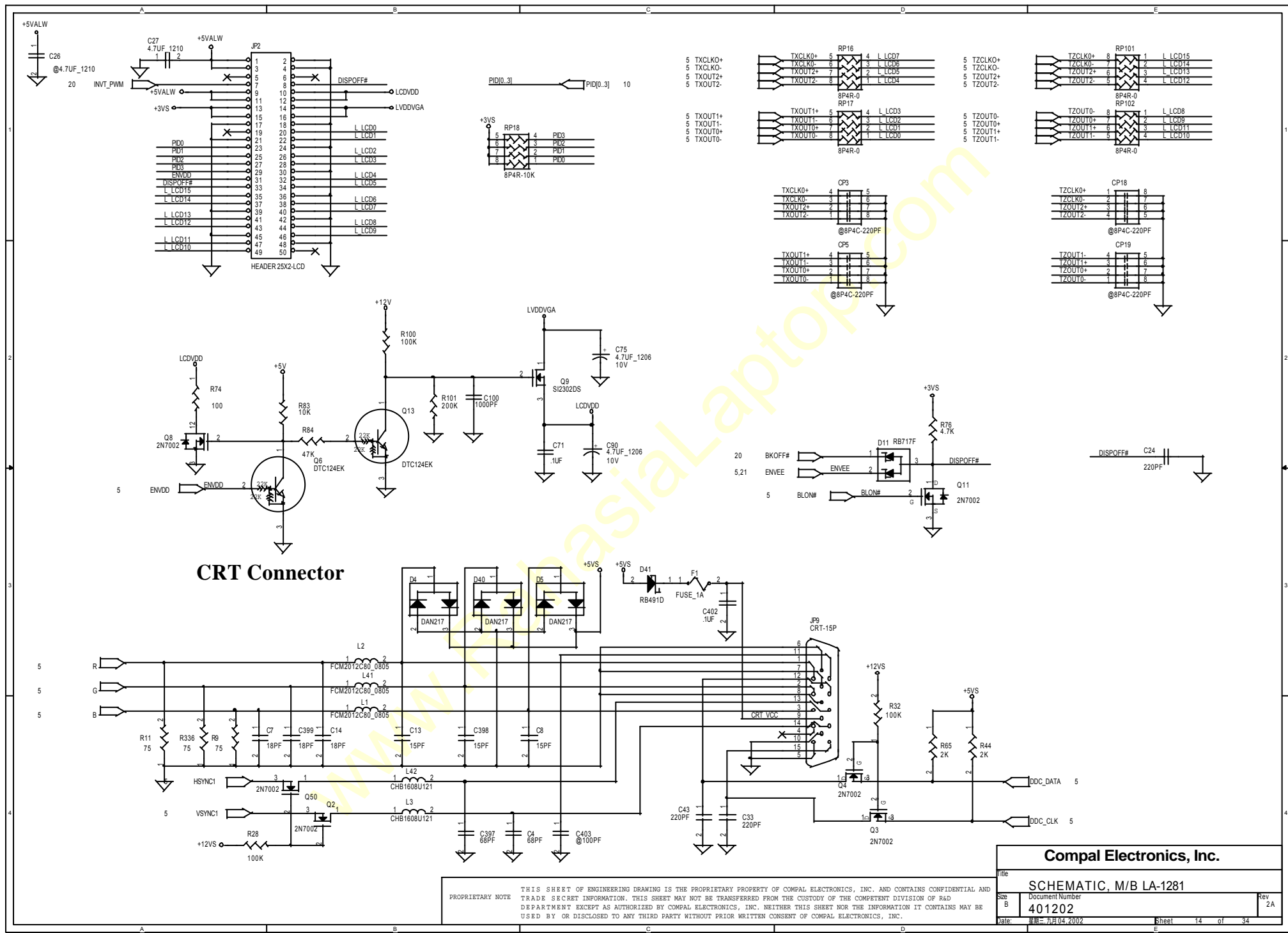
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TV-OUT Encode



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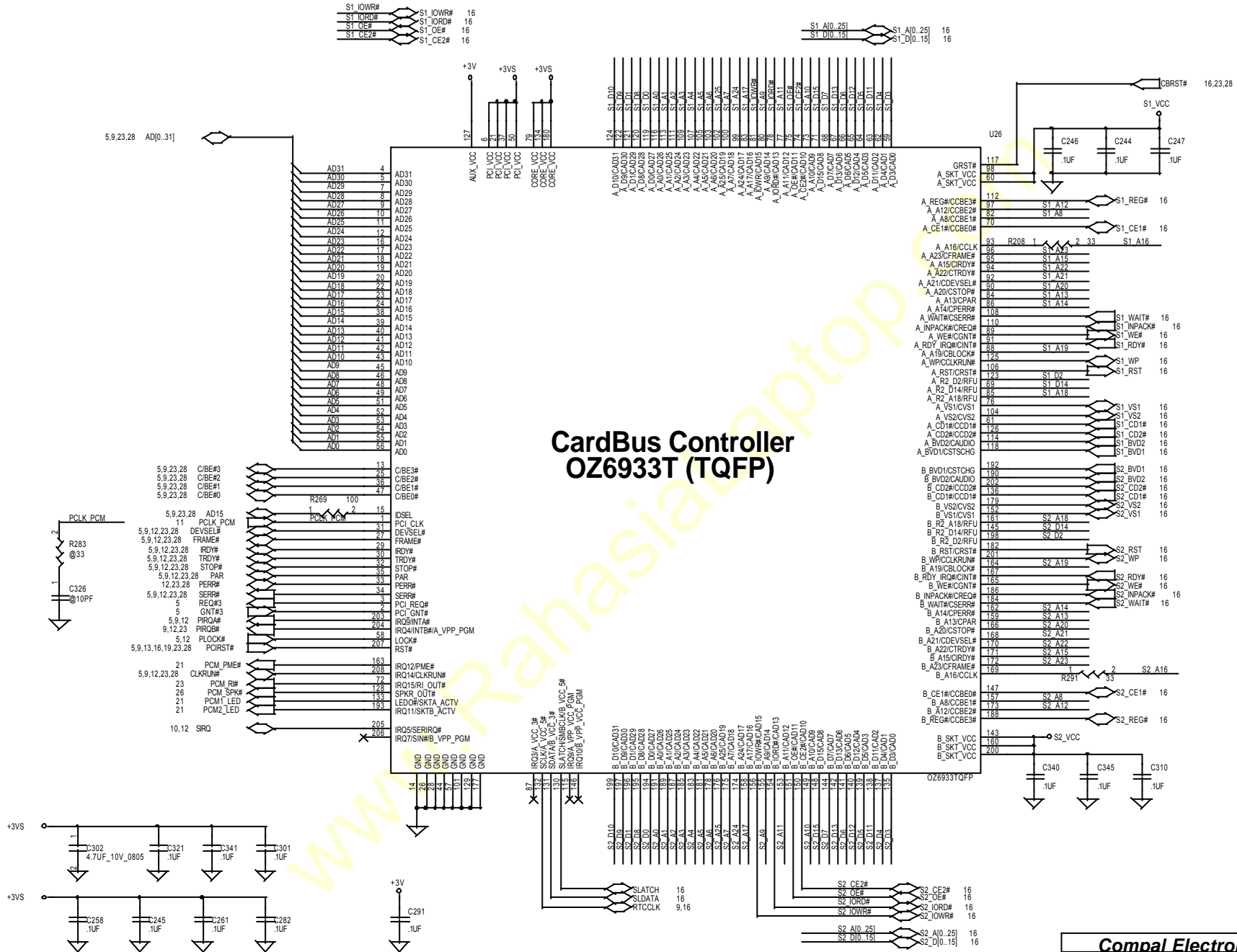


**CRT Connector**

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# CardBus Controller OZ6933T (TQFP)

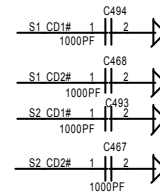
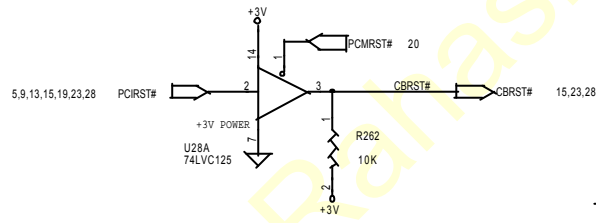
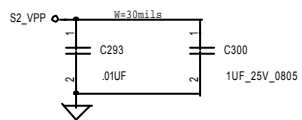
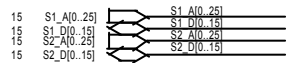
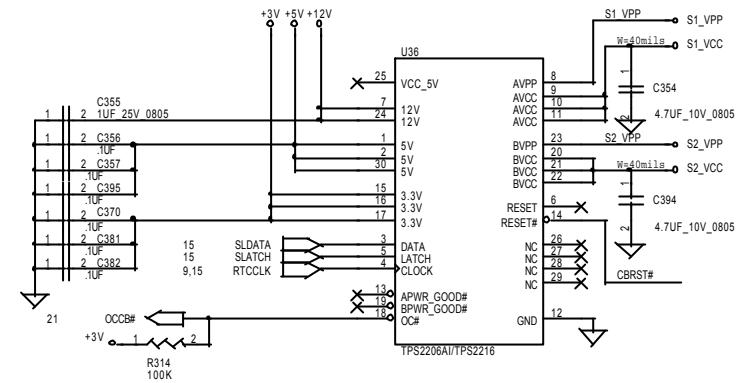


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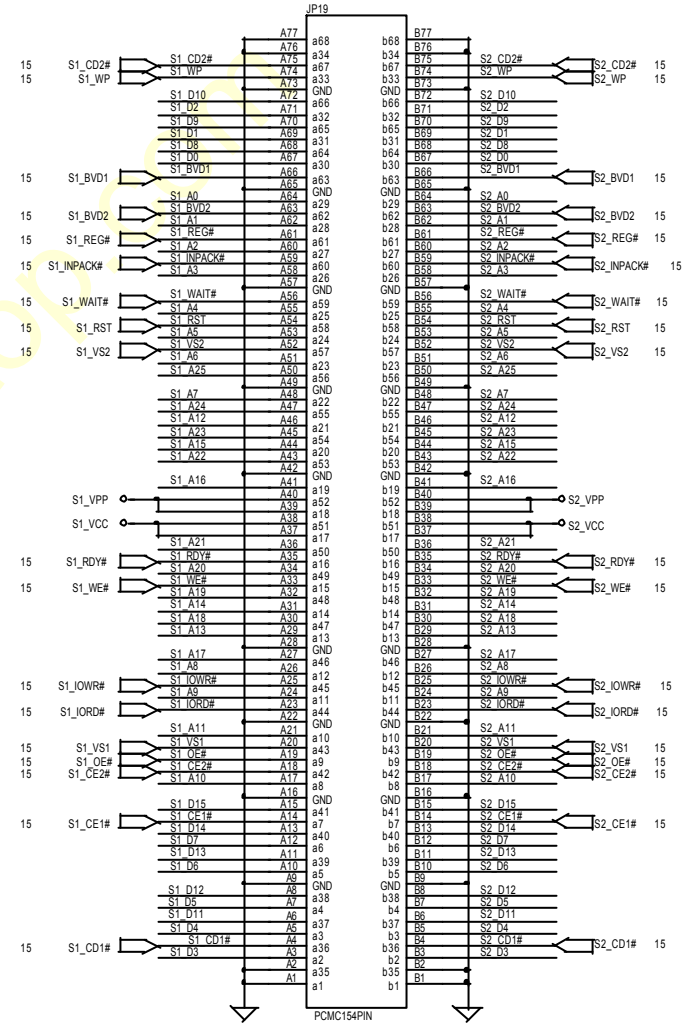
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PCMCIA POWER CTRL. Wire ZV PORT to Slot A



CARDBUS SOCKET



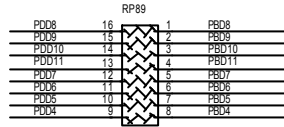
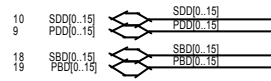
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SCHEMATIC, M/B LA-1281

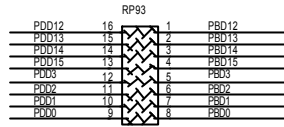
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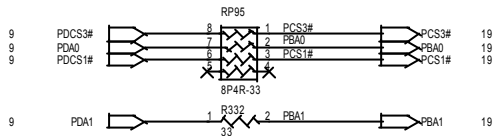
**IDE Series Resistor**  
Place them close SB



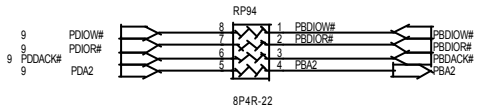
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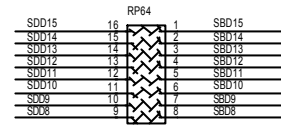
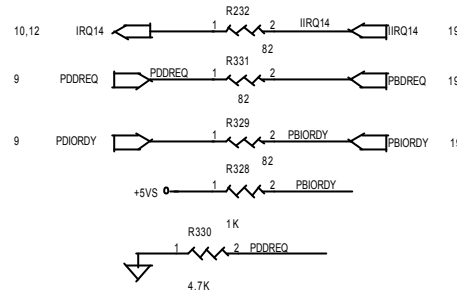
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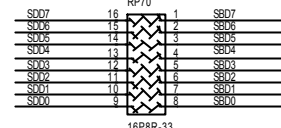
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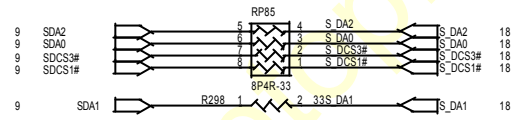
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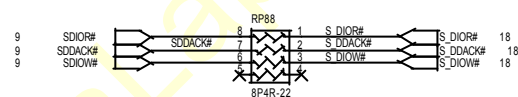
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16P8R-33



8P4R-33



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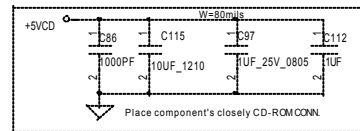
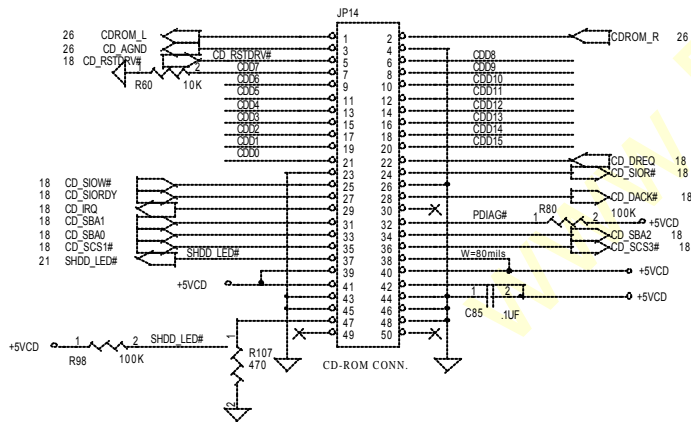
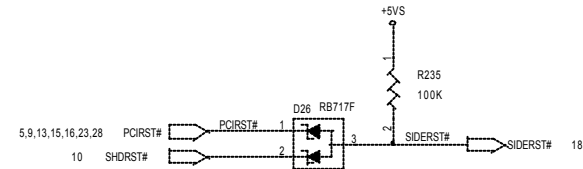
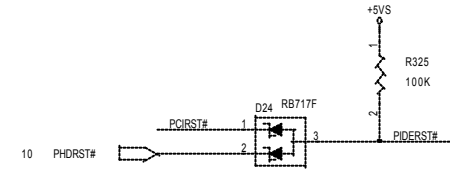
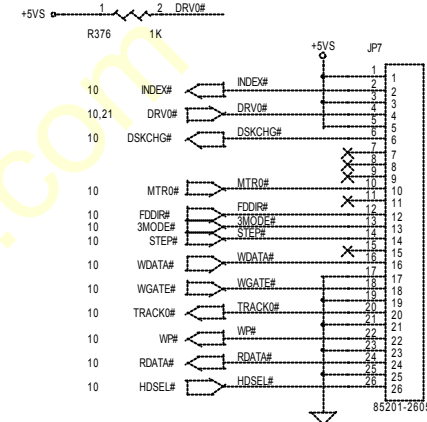
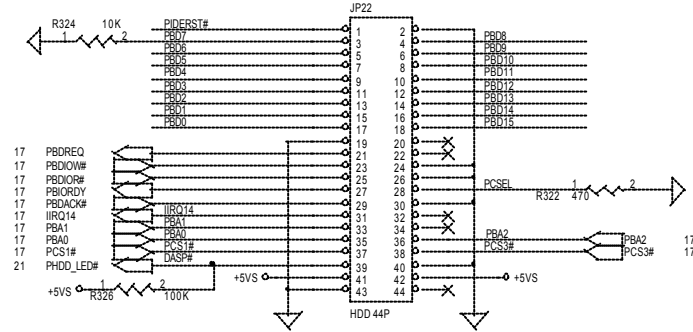
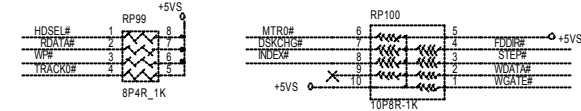
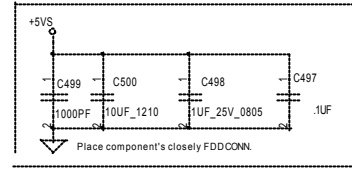
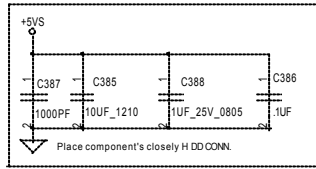
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# IDE, CD-ROM & FDD Module CONN.

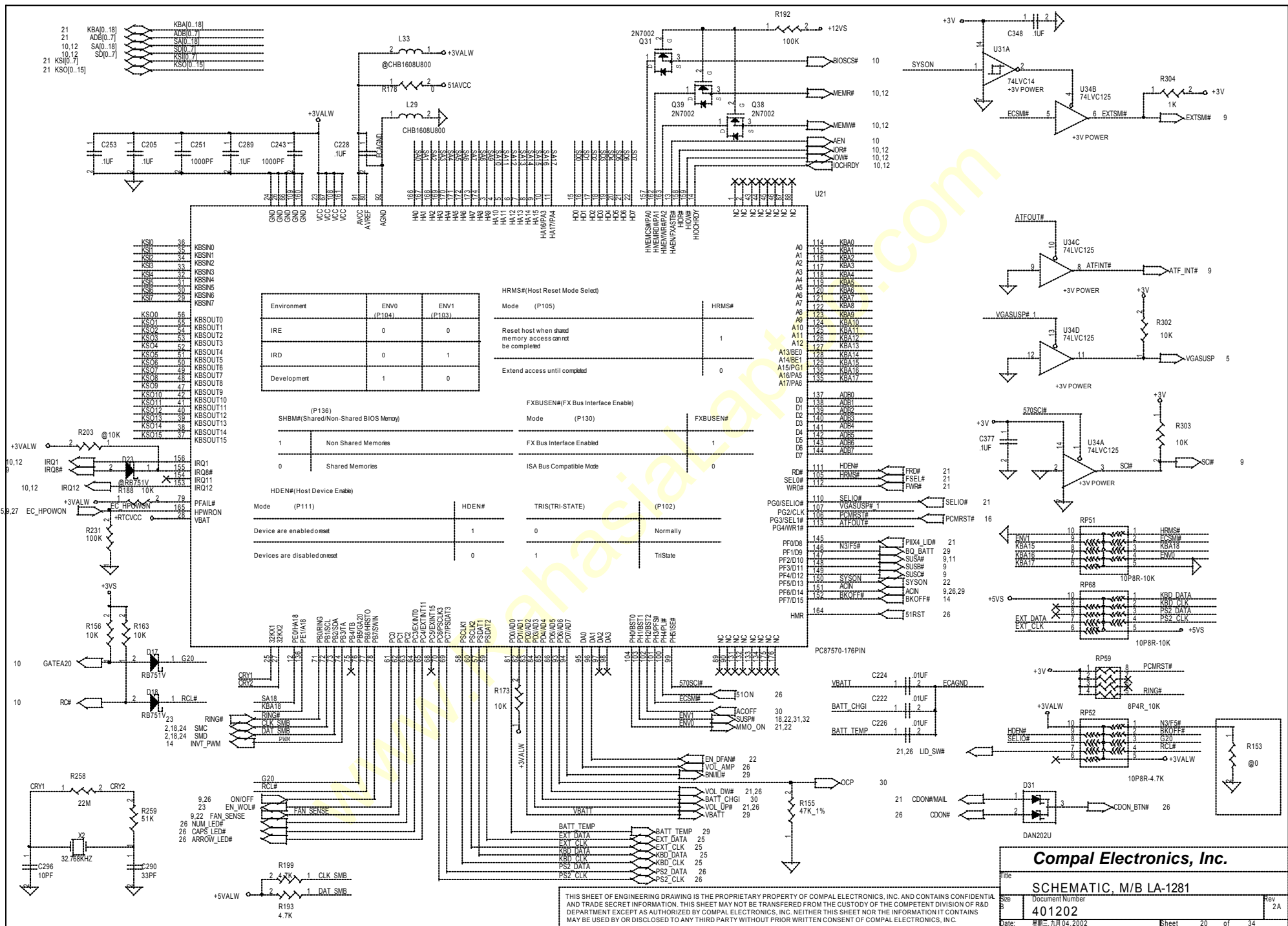


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Environment	ENV0 (P104)	ENV1 (P103)
IRE	0	0
IRD	0	1
Development	1	0

Mode (P105)	HRMS#
Reset host when shared memory access cannot be completed	1
Extend access until completed	0

SHBM# (P136)	Mode (P130)	FXBUSEN#
1   Non Shared Memories	FX Bus Interface Enabled	1
0   Shared Memories	ISA Bus Compatible Mode	0

Mode (P111)	HDEN#	TRIS(TRI-STATE) (P102)
Devices are enabled on reset	1	Normally
Devices are disabled on reset	0	TriState

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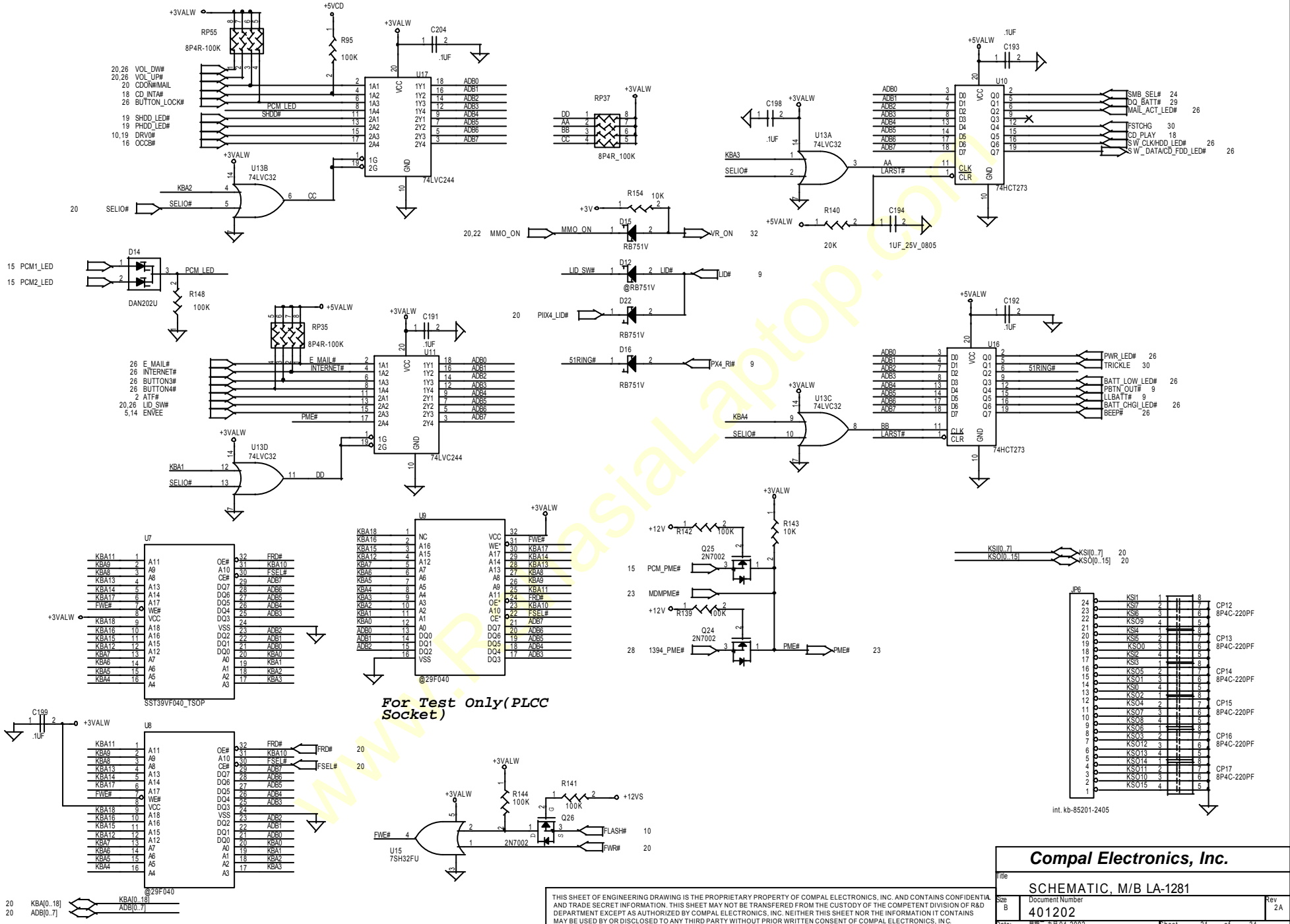
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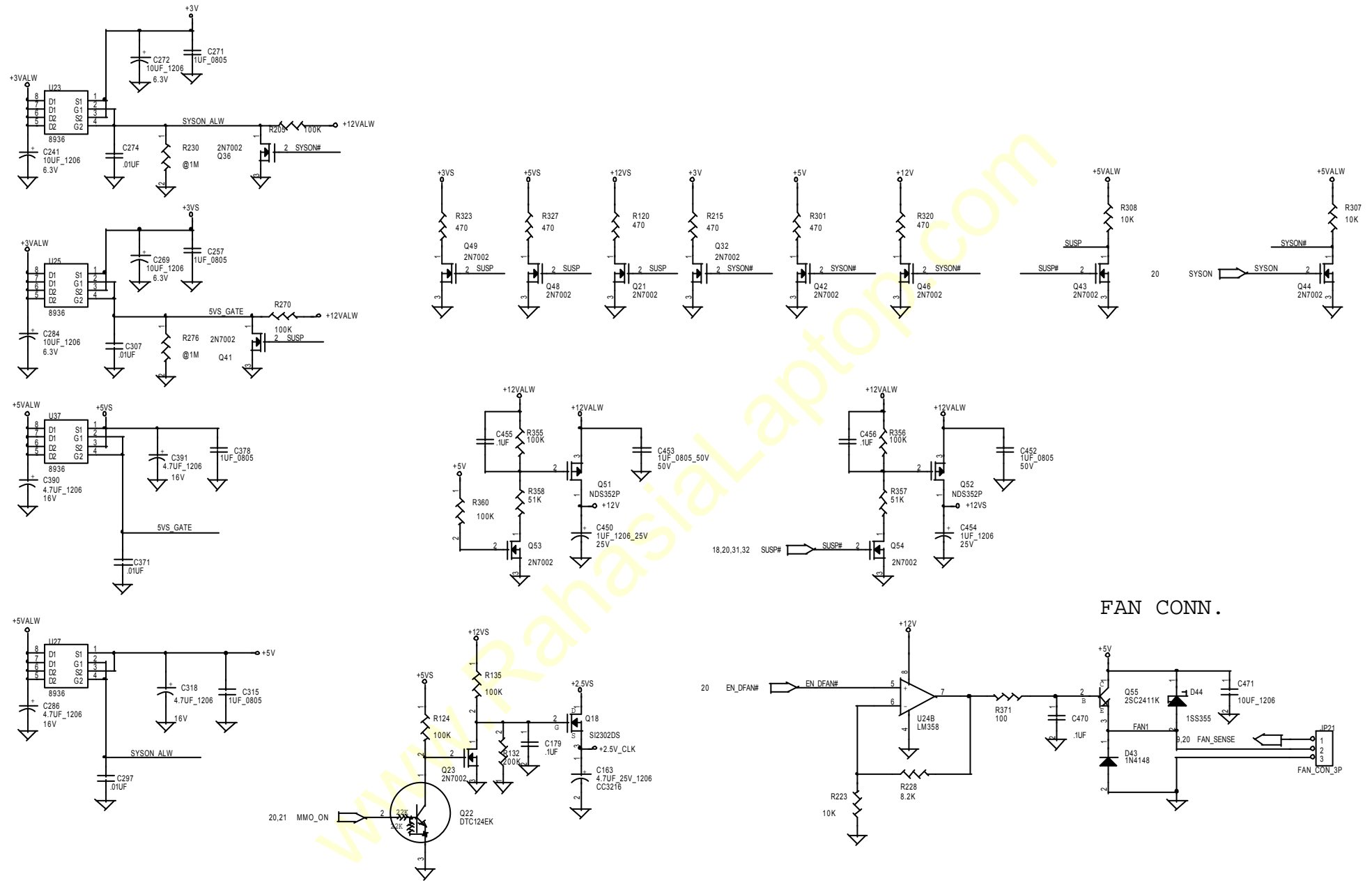
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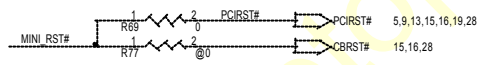
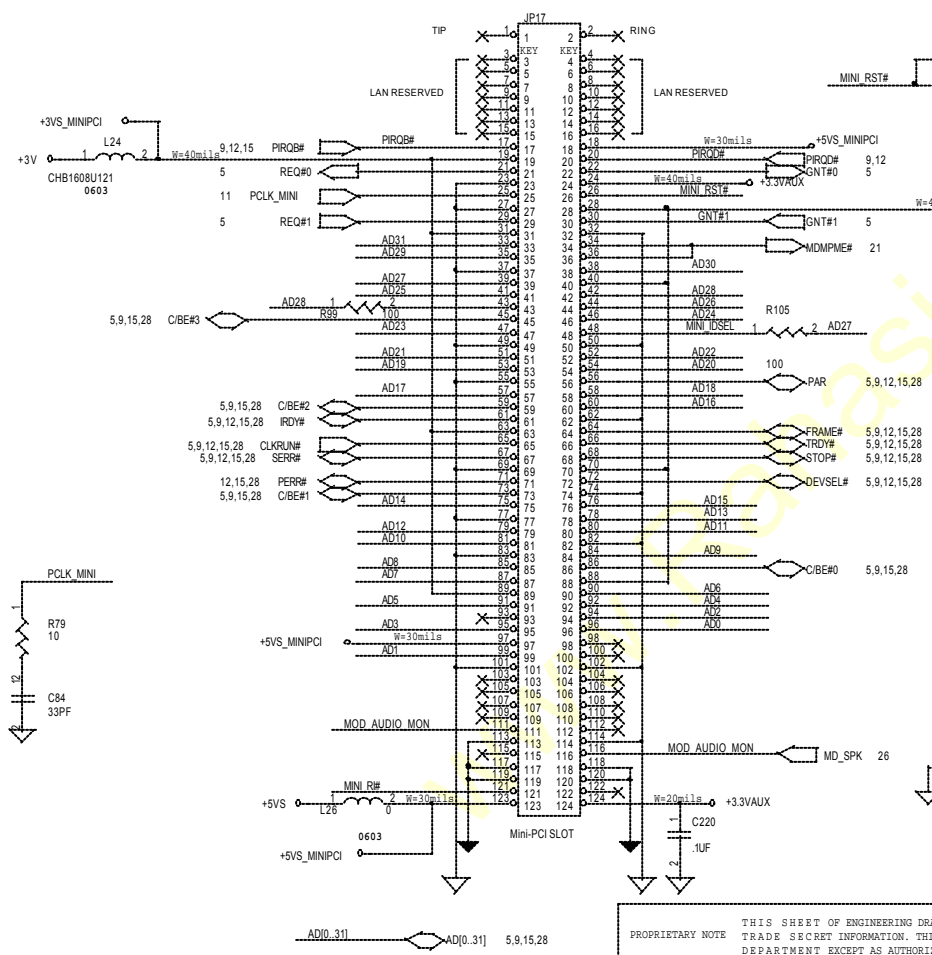
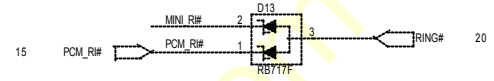
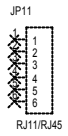
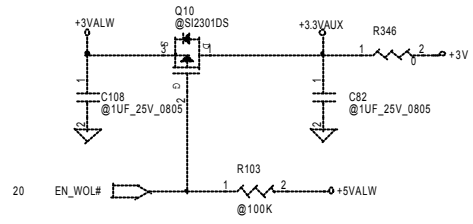


FAN CONN.

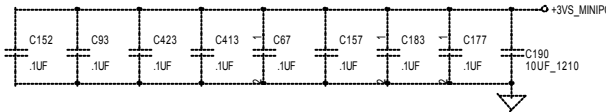
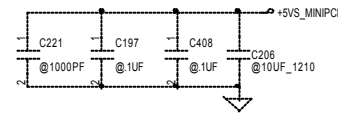
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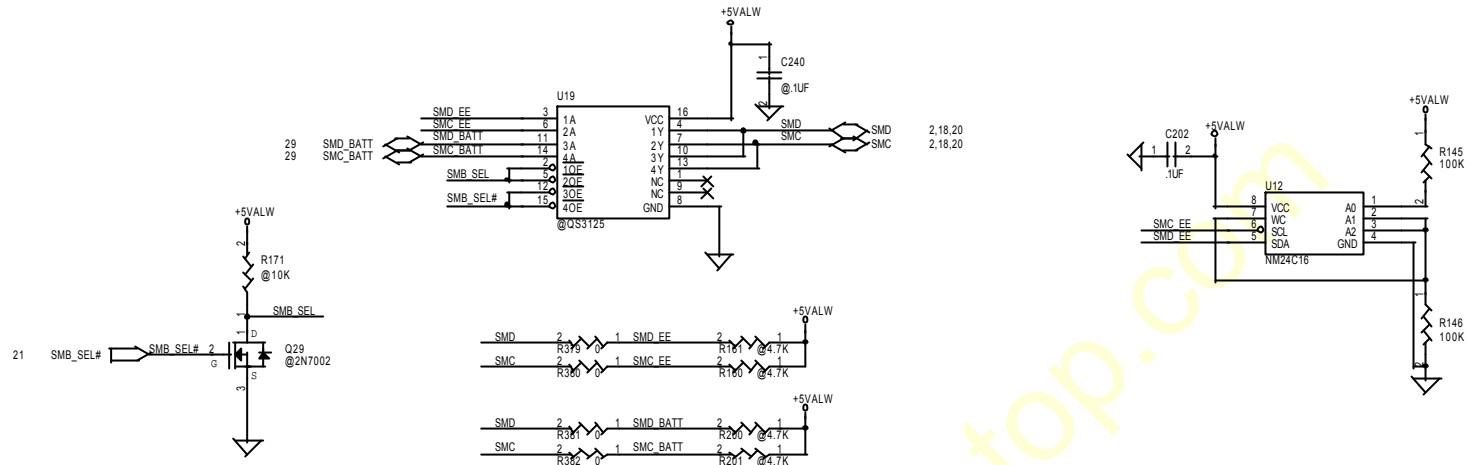


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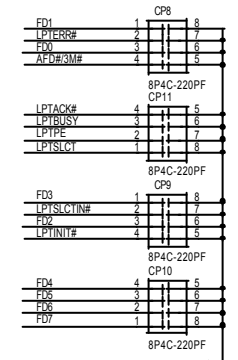
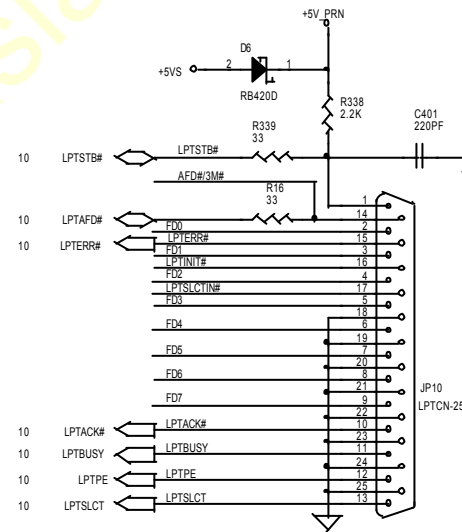
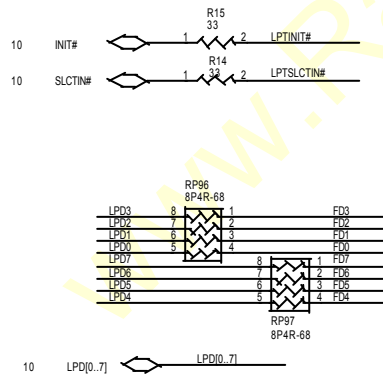
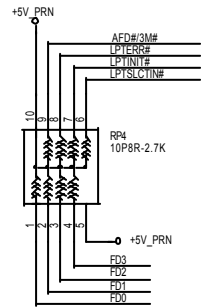
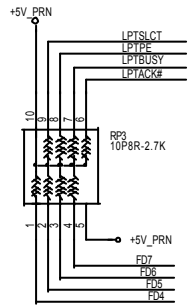
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PARALLEL PORT

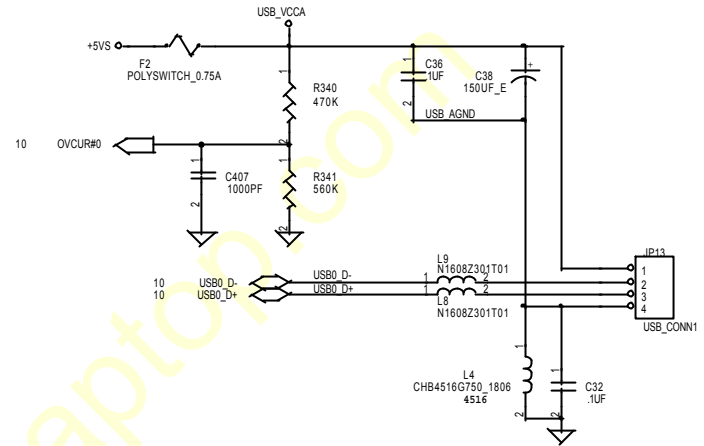
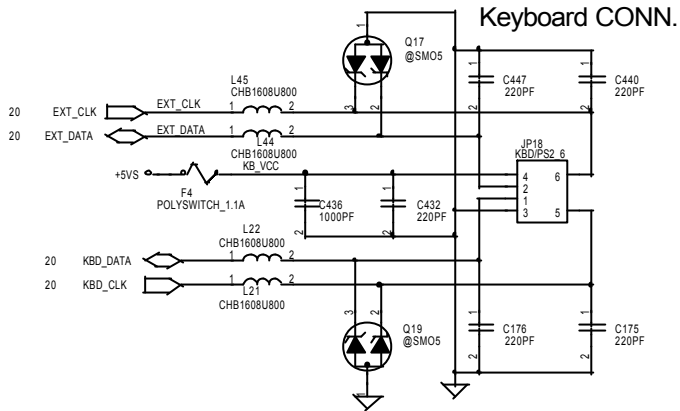


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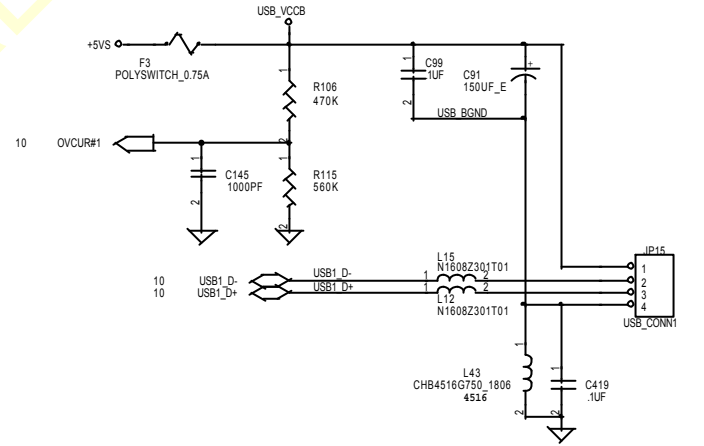
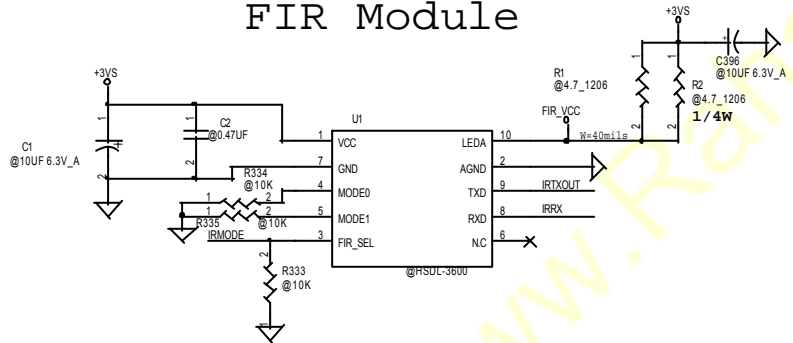
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### FIR Module

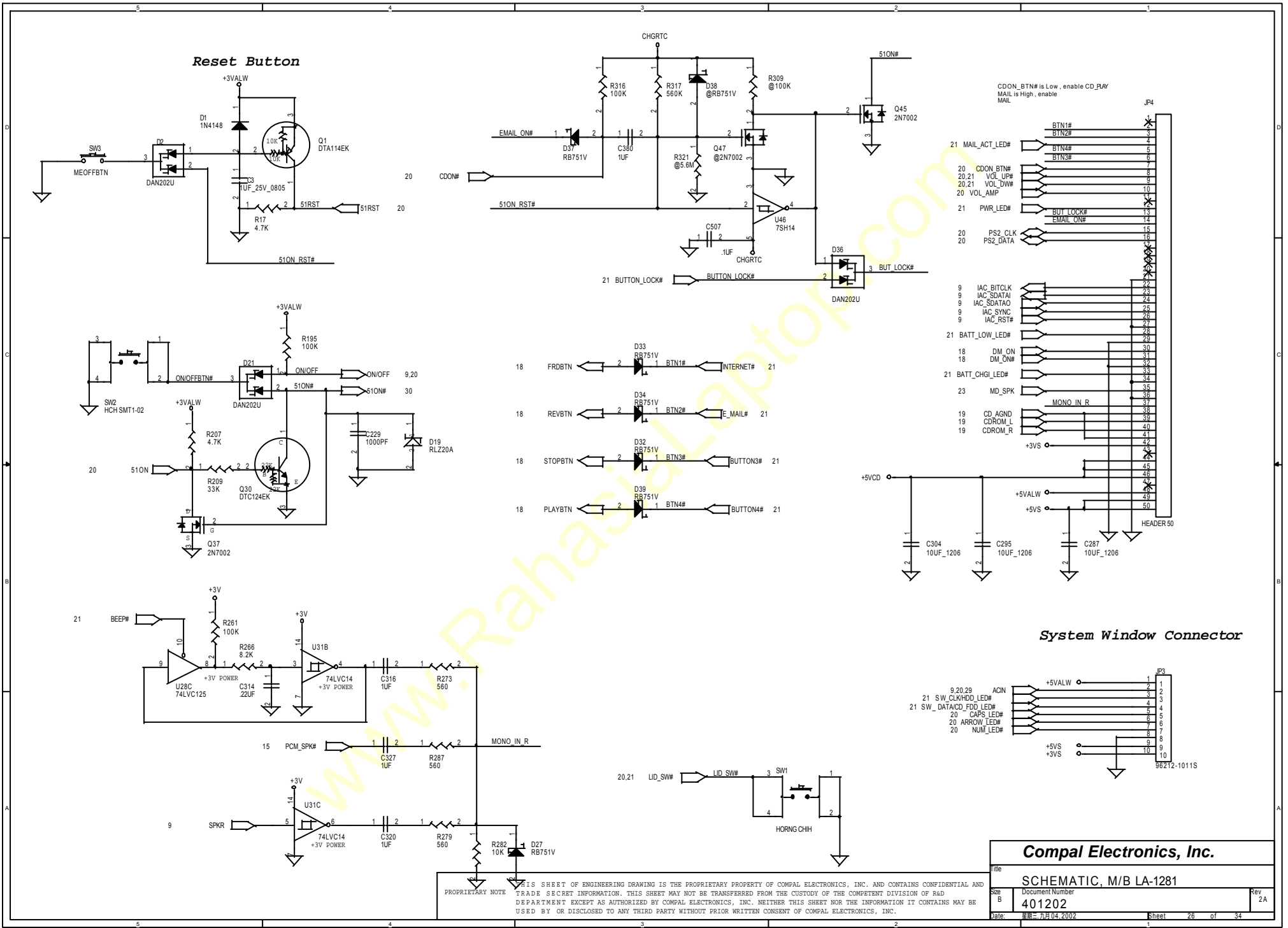


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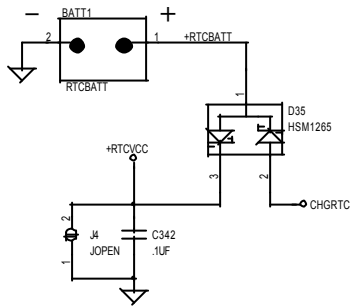
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MAIL is High, enable MAIL

System Window Connector

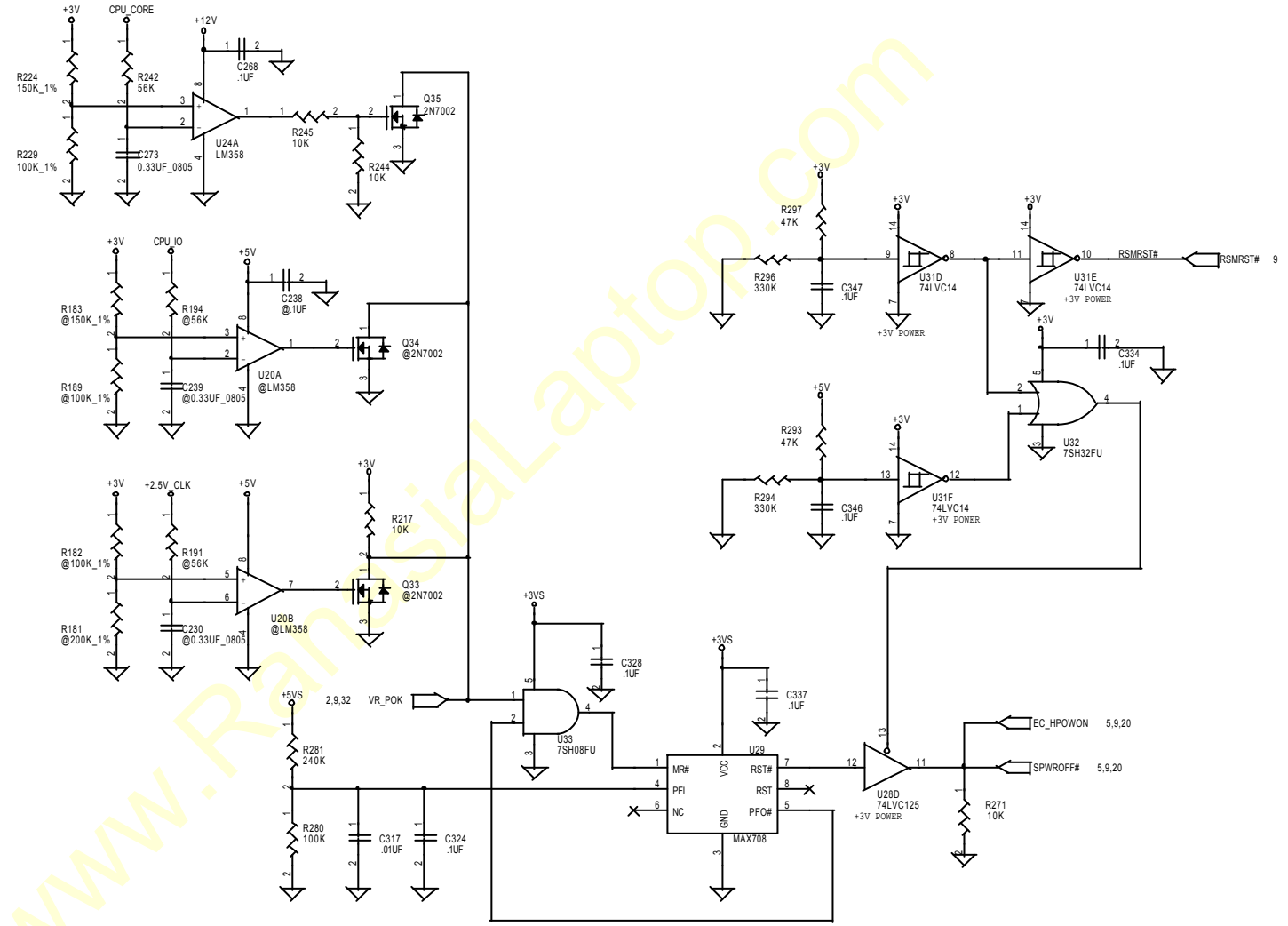
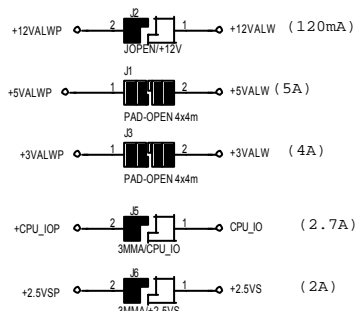
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### RTC BATT

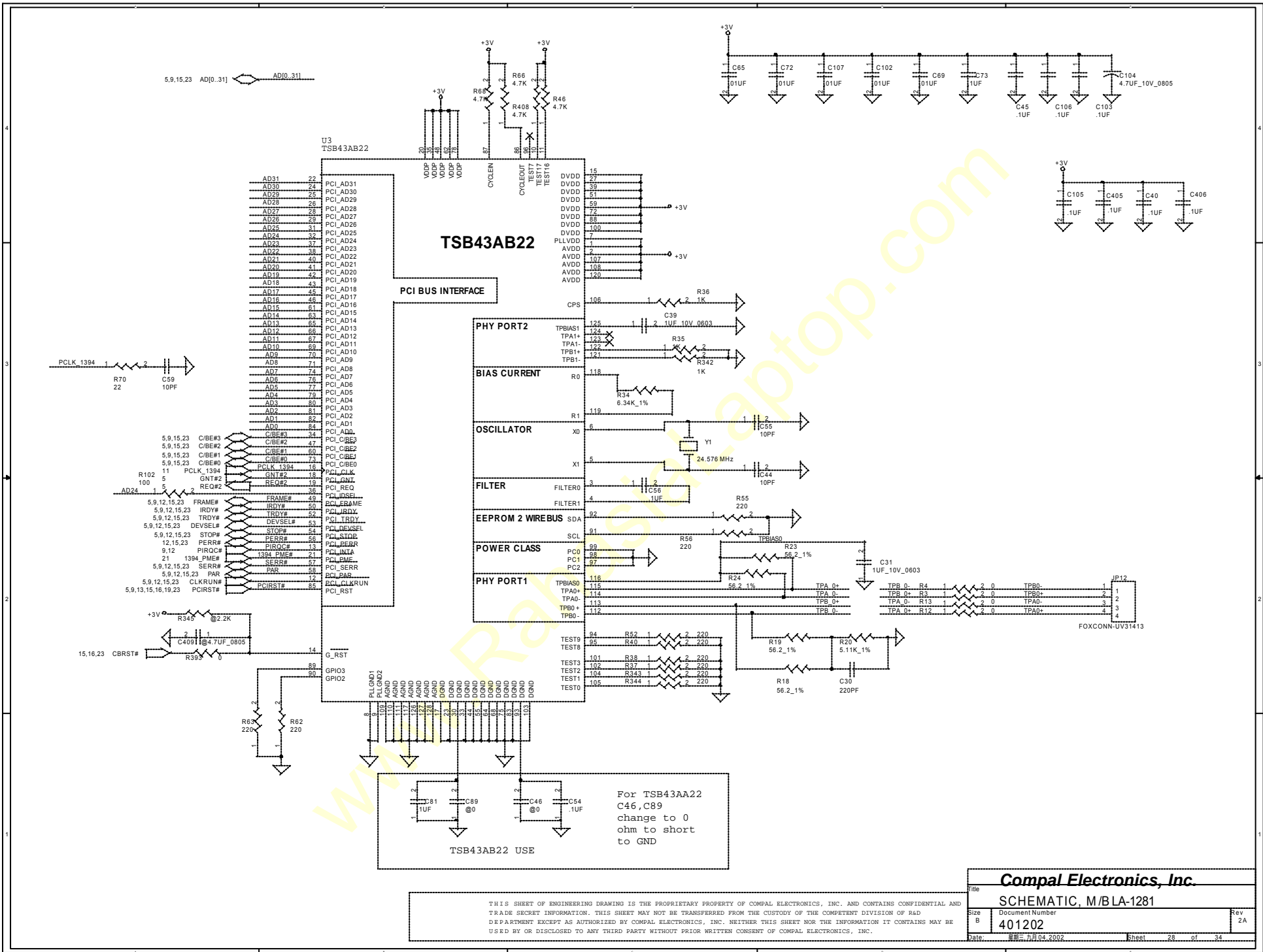


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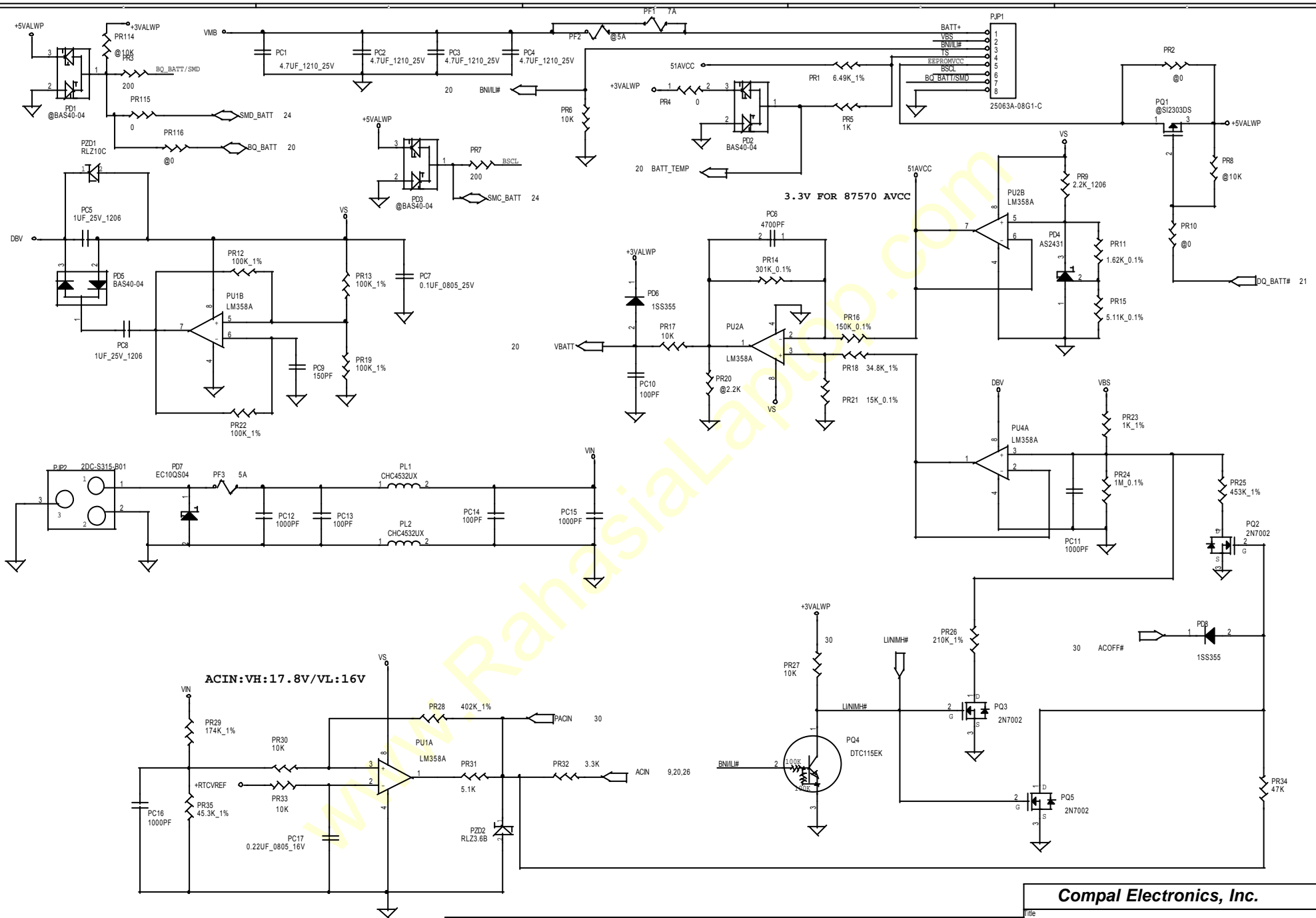


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ACIN: VH: 1.7.8V / VL: 1.6V

3.3V FOR 87570 AVCC

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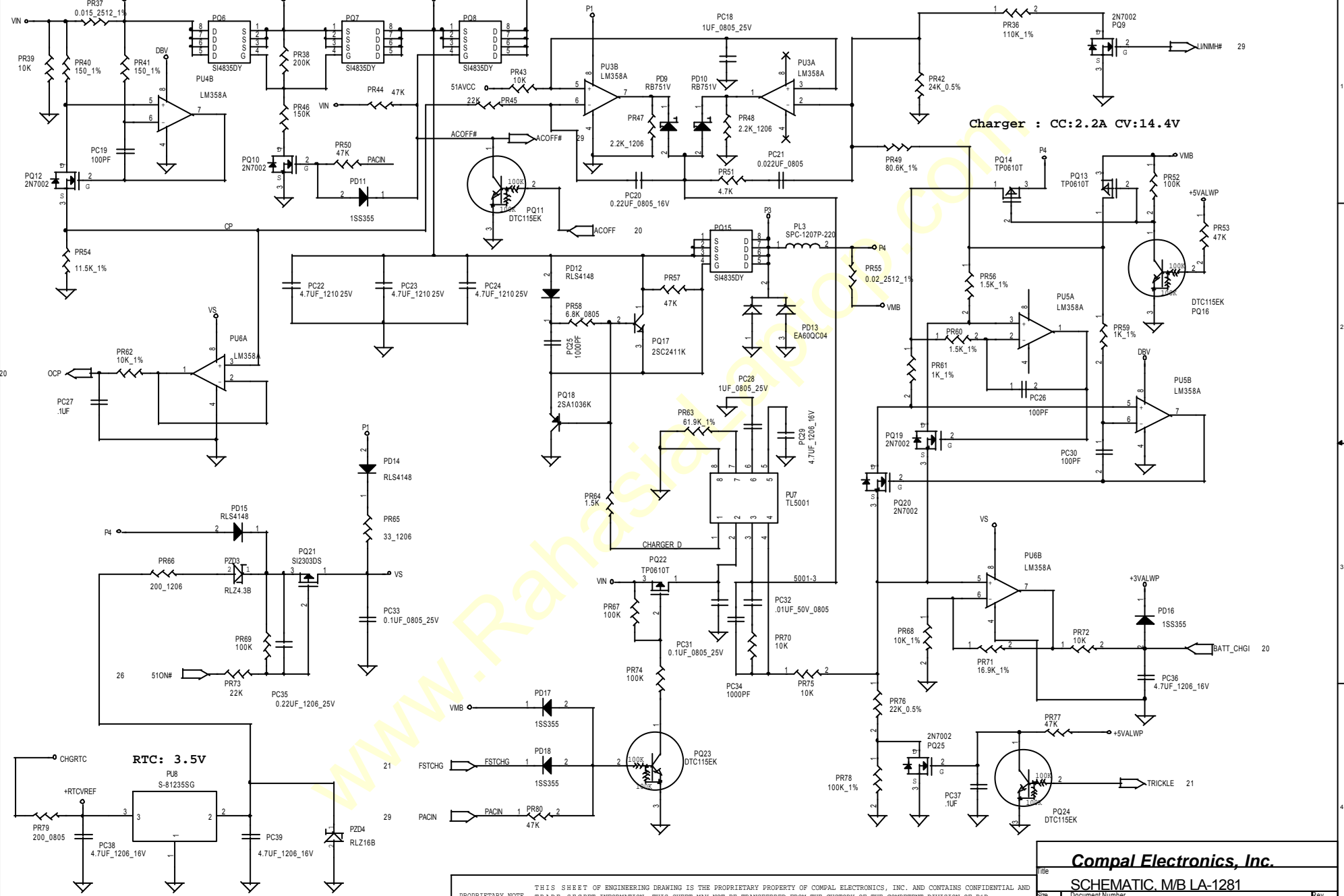
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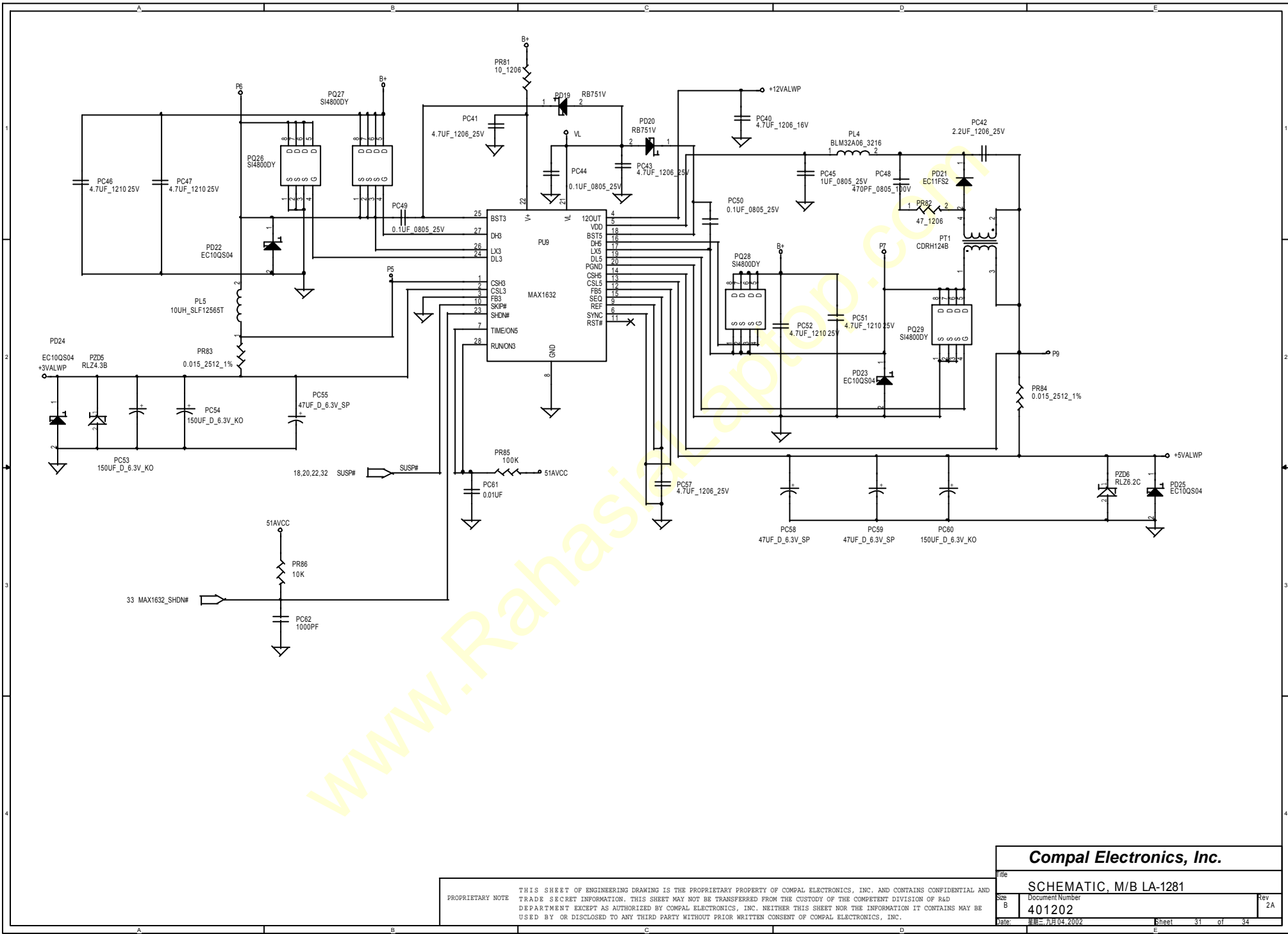
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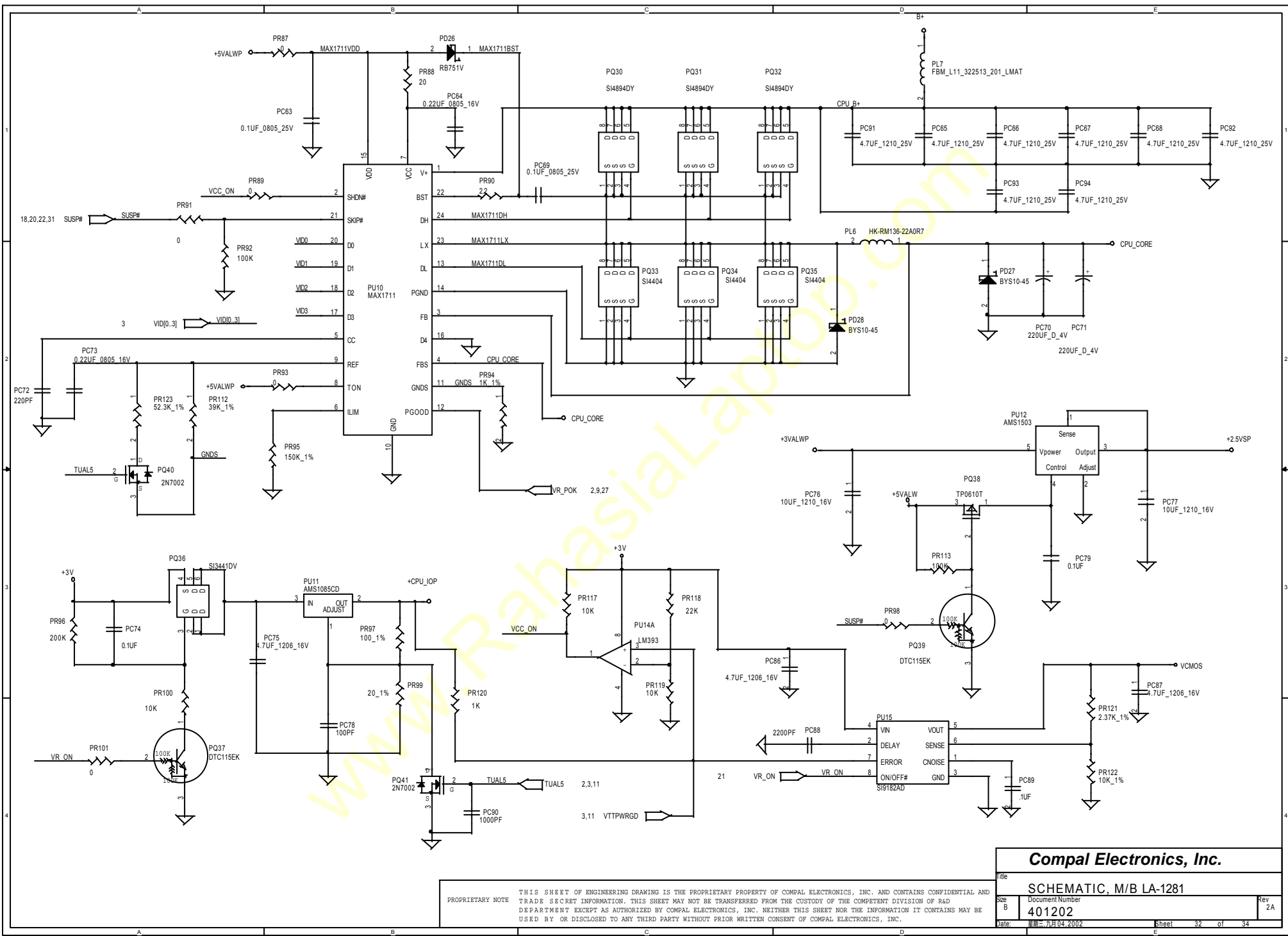
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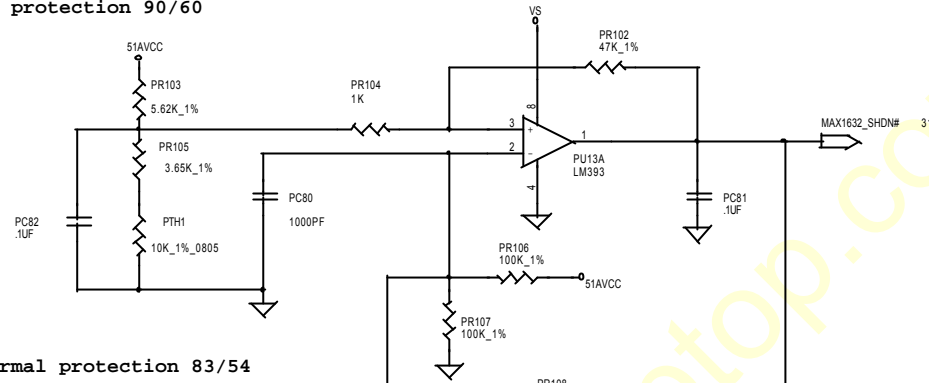
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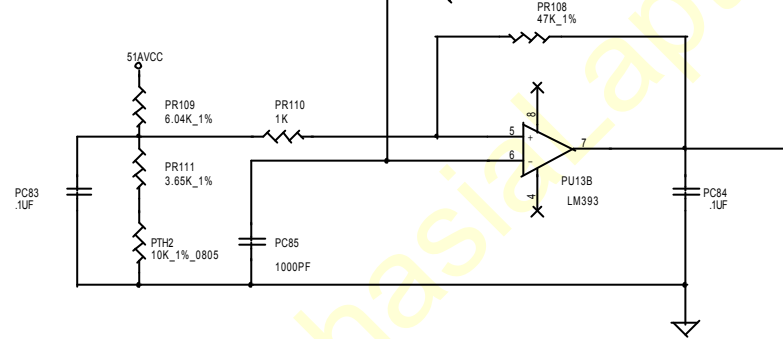
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度C



For Battery thermal protection 83/54  
度C



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# CY23 PIR LIST

08/28/01 Written by Jerry

P11: Add Q61 and R407 for VTTPWRGD

\*\*\*\*\* Rev1.0 PIR List \*\*\*\*\*

09/10/01 Written by Jerry

P26: Add @ at R309 and Q47

Add C507 and U46

Change value of R317 to 510K

P27: Remove @ at R224, R229, R242, R245, R244, C273, and Q35

P32: Add PC91, PC92, PC93, and PC94.

09/12/01 Written by Jerry

P06: Change value of RP34, RP50, RP54, RP62, RP38, RP33, RP57,

RP61, RP53, and RP56 to 16P8R-22

P26: Change value of R317 to 560K

09/19/01 Written by Jerry

P29: Change value of PR29 to 174K\_1%

P32: Change value of PR123 to 52.3K\_1%

\*\*\*\*\* Rev2.0 PIR List \*\*\*\*\*

10/03/01 Written by Jerry

P02: Change value of R27 to 180

Delete R395

R395's Pin 1 tie to RP98's pin5

P03: Change value of R353 to 56.2 1%

P28: Add R408 between +3V and pin 87 of U3

10/08/01 Written by Jerry

P11, P13, P28: Change footprint of Y1, Y2, and Y3

P23: Change footprint of JP11

P28: Change footprint of JP12

P31: Change footprint of PL5

P26: Change footprint of SW1

10/17/01 Written by Jerry

P02: Add @ at RP25, RP24, RP28, RP27, RP31, RP30, RP 42, RP41,

RP40, RP43, RP44, RP45, RP46, RP47, RP48, RP49, RP7, RP1, RP6,

RP14, RP20, RP19, RP22, RP9, RP10, RP11, RP8, RP2, and R7

P06: Remove @ at R164

P11: Add @ at R176

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