Compal Confidential

NIWE2

Schematics Document

Arrandale

with Intel IBEX PEAK-M core logic

REV:0.3

Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

Compal Electronics,Ltd.

Title: **Cover Sheet**

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Compal confidential
File Name :

zzz

15.6W_PCB_LA5752P

POWER BD: LS-5754P
POWER BT
NOVO BT
POWER MANAGE BT

CAP SENSOR BD:LS-5752P
VOLUME UP
VOLUME DOWN
MUTE
AUDIO ENHANCE
BUTTON & LED

CARD READER BD:
LS-5753P
RTS5138
HP JACK
MIC JACK

VRAM 64*16
DDR3*4
page20

NVidia N11M-GE1
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PCI-E X16

intel
Arrandale
(UMA/DIS)
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37.5mm*37.5mm
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Clock Generator
ICS9LRS3199AKLFT
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DDR3-SO-DIMM X2
BANK 0, 1, 2, 3
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UP TO 8G

Dual Channel
DDR3-800(1.5V)
DDR3-1067(1.5V)

HDMI
CONN
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level shift IC
ASM1442
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100MHz
2.7GT/s
FDI *8
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CRT Connector
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FCBGA 951
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AZALIA

Audio Codec
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14*USB2.0

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PCI Express
Mini card Slot 2
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6*SATA serial

BlueTooth CONN
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USB CONN X1(Right)
page37

SPI ROM
BIOS page13

USB PORT X1(Left)
page37

SIM Card
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USB(WWAN)

LPC BUS

New Card X1
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WWAN
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Card Reader/Audio Jack SB
CONN
Realtek 5138
MS/MS
pro/SD/SD
pro/mmc/XD
HP X 1+
MIC_Ext X1
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EC
ENE KB926D
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Title: MB Block Diagram

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DDR3 Voltage Rails

power plane / State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +1.8VS +0.75VS +1.05VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

SMBUS Control Table

	SOURCE	RAM M2	BATT	KE926	SODIMM	CLK CHIP	WLAN WWAN	N10x Thermal Sensor	N10x	Cap sensor board	NEW CARD	PCH
SMB_EC_CK1 SMB_EC_DA1	KB926 +3VALW	X	V +3VALW	X	X	X	X	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926 +3VALW	X	X	X	X	X	X	X	X	X	X	V +3VALW
SMBCLK SMBDATA	PCH +3VALW	V +3VALW	X	X	V +3VS	V +3VS	X	X	X	X	V +3VS	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	X	X	V +3VALW	X	X	X	V +3VS	X	V +3VS	X	X

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

@ FUNCTION

	EVT	NON-USE
45@	(45 BOM)	
100@	10/100 LAN	
GIGA@	GIGA LAN	
UMA_HDMI@	FOR UMA HDMI components	
HDMI@	FOR HDMI components	
3G@	3G(WWAN) function	
X76@	(X76 BOM)	
ESATA@	ESATA function	
CMOS@	Camera function	
BT@	Blue Tooth	
~~10M@~~	~~FOR 10M CHIP~~	
~~11M@~~	~~FOR 11M CHIP~~	
UMA@	UMA only (Arranddale)	
DIS@	DIS only (Arranddale)	
~~VGA@~~	~~FOR NVIDIA PART~~	
~~HYBRID@~~	~~FOR SWITCHABLE~~	
~~HU@~~	~~SWITCHABLE or UMA only~~	
~~HD@~~	~~SWITCHABLE or DIS only~~	

SKU

Arrandale(dGPU) DIS only	DIS@ / 100@ for EVT
Arrandale(iGPU) UMA only	UMA@ / 100@ for EVT
~~Arrandale(iGPU+dGPU)~~ ~~SWITCHABLE~~	~~VGA@+HD@+HU@+HYBRID@~~

PCIE PORT LIST

PORT	DEVICE
1	
2	WLAN
3	LAN
4	3G
5	NEW CARD
6	
7	
8	

USB PORT LIST

PORT	DEVICE
0	RIGHT SIDE
1	LEFT SIDE
2	CMOS
3	LEFT SIDE
4	RIGHT SIDE
5	CARD READER
6	
7	
8	WIRELESS
9	
10	NEW CARD
11	BT
12	
13	3G

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Title	MB Notes List
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VGA and DDR3 Voltage Rails (N10x GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	N/A	N/A	
GPIO1	IN	-	Hot plug detect for IFP link C
GPIO2	OUT	H	Panel Back-Light brightness(PWM capable)
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light On/Off (PWM)
GPIO5	OUT	-	GPU VID0
GPIO6	OUT	-	GPU VID1
GPIO7	OUT	-	GPU VID2
GPIO8	I/O	L	Thermal Catastrophic Overtemp
GPIO9	OUT	L	Thermal Alert
GPIO10	OUT		Memory VREF switch
GPIO11	I/O	L	SLI raster sync
GPIO12	IN	-	AC power detect pin
GPIO13	OUT	-	MEM_VID orPower supply control
GPIO14	OUT	-	Power supply control
GPIO15	IN	-	Hot plug detect for IFP Link E
GPIO16	OUT	-	Programmable Fan Control
GPIO17	IN	-	
GPIO18	IN	-	
GPIO19	IN	-	Hot plug detect for IFP Link D
GPIO20	IN	-	
GPIO21	IN	-	Hot plug detect for IFP link F
GPIO22	IN	-	SLI swap ready signal
GPIO23	I/O		

GPIO6 GPIO5 N10M-GS N10P-GS

GPU_VID1	GPU_VID0	VGA_CORE	P-State
0	0	0.8V	12
0	1	0.85V	12
1	0	0.9V	0,10
1	1	1.0V (N10M-GS) 0.925V (N10P-GS)	

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

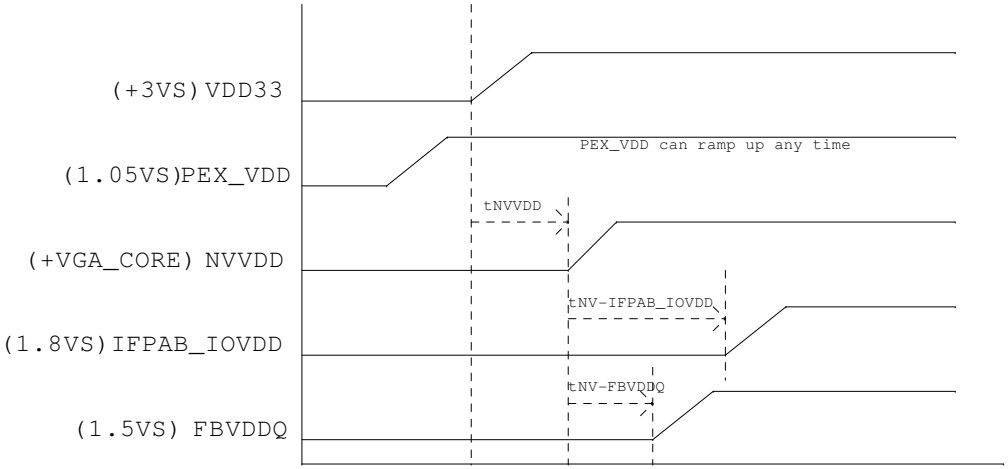
Products	GPU (4) (W)	Mem (1,5) (W)	NVCLK /MCLK (MHz)	NVVDD (V)	NVVDD (A)	NVVDD (W)	FBVDD (1.5V) (A)	FBVDD (1.5V) (W)	FBVDDQ (GPU+Mem) (1.5V) (A)	FBVDDQ (GPU+Mem) (1.5V) (W)	PCI Express (1.05V) (6) (mA)	PCI Express (1.05V) (6) (W)	I/O and PLLVDD (1.8V) (mA)	I/O and PLLVDD (1.8V) (W)	I/O and PLLVDD (1.05V) (mA)	I/O and PLLVDD (1.05V) (W)	Other (3.3V) (mA)	Other (3.3V) (W)
N10P-GS 128bit 1024MB DDR3	21.07	6.67	TBD	TBD	18.25	17.34	2.06	3.09	4.09	6.14	850	0.89	75	0.14	63	0.07	55	0.18
N10P-GE 128bit 1024MB DDR3	20.97	6.73	TBD	TBD	19.17	17.25	2.03	3.05	4.09	6.14	840	0.88	75	0.14	63	0.07	55	0.18
N10P-LP 128bit 1024MB DDR3	15.48	6.44	TBD	TBD	13.95	11.86	1.90	2.85	3.99	5.99	810	0.85	75	0.14	63	0.07	55	0.18

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

Products	GPU (4) (W)	Mem (1,5) (W)	NVCLK /MCLK (MHz)	NVVDD (V)	NVVDD (A)	NVVDD (W)	FBVDD (1.5V) (A)	FBVDD (1.5V) (W)	FBVDDQ (GPU+Mem) (1.5V) (A)	FBVDDQ (GPU+Mem) (1.5V) (W)	PCI Express (1.05V) (6) (mA)	PCI Express (1.05V) (6) (W)	I/O and PLLVDD (1.8V) (mA)	I/O and PLLVDD (1.8V) (W)	I/O and PLLVDD (1.05V) (mA)	I/O and PLLVDD (1.05V) (W)	Other (3.3V) (mA)	Other (3.3V) (W)
N10M-GE 64bit 512MB DDR3	13.36	2.93	TBD	TBD	11.89	10.70	0.66	0.99	2.16	3.24	792	0.83	75	0.14	63	0.07	100	0.33
N10M-GS 64bit 512MB DDR3	14.29	3.10	TBD	TBD	11.53	11.53	0.70	1.05	2.28	3.42	817	0.86	75	0.14	63	0.07	100	0.33
N10M-LP 64bit 512MB DDR3	8.28	2.91	TBD	TBD	6.60	5.61	0.62	0.93	2.20	3.3	782	0.82	75	0.14	63	0.07	100	0.33

Power Sequence

The ramp time for any rail must be more than 40us



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Title: VGA Notes List

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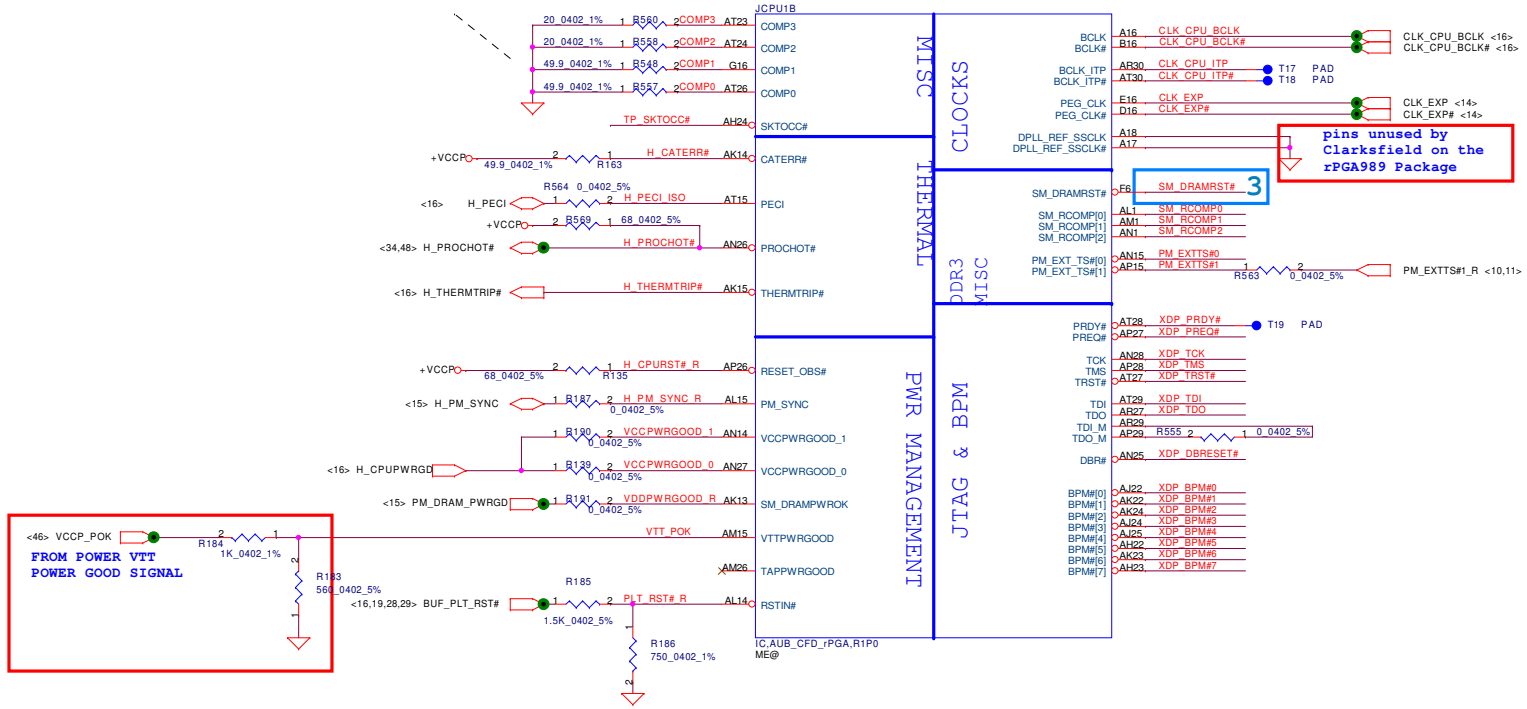
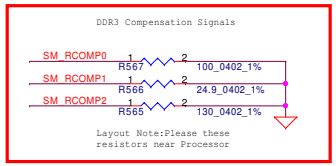
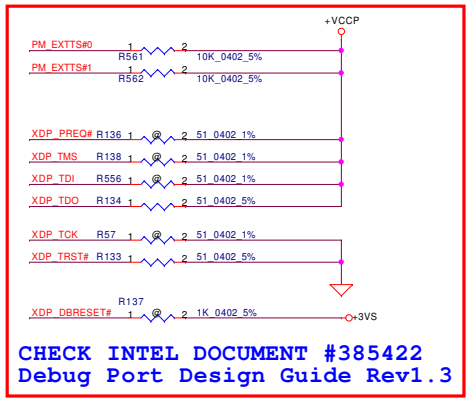
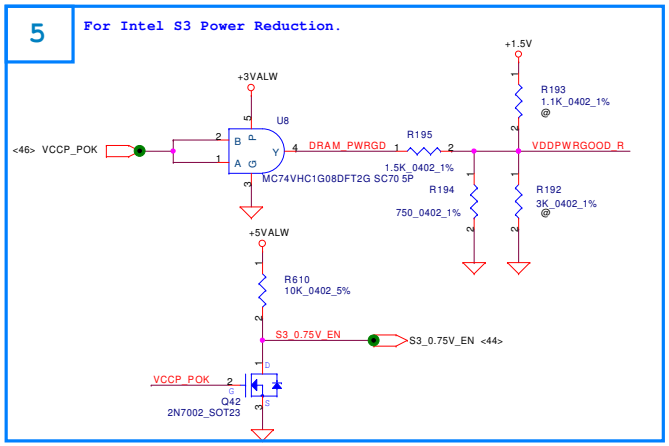
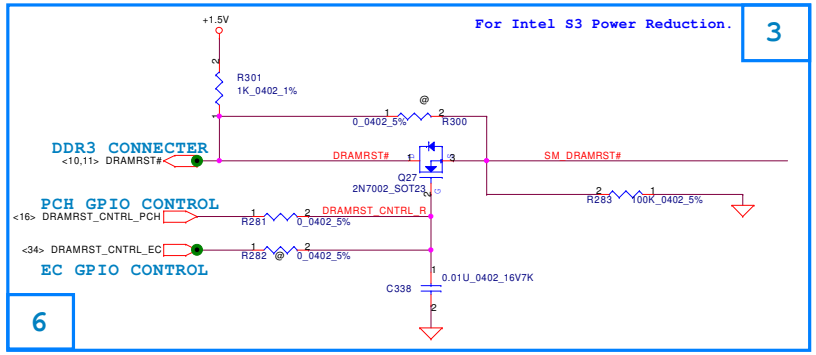
Layout rule：10mil width trace
length < 0.5", spacing 20mil











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Title: Arrandale(1/5)-Thermal/XDP

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Layout rule：trace length < 0.5"

JCPU1A

DMI

PCI EXPRESS -- GRAPHICS

Intel(R) FDI

IC,AUB_CFD_rPGA,R1P0
ME@

PCIE Lane Numbers Reversed

CFG3-PCI Express Static Lane Reversal

VGA@

FOR ES1 SAMPLE ONLY

JCPU1E

RESERVED

IC,AUB_CFD_rPGA,R1P0
ME@

CFG Straps for PROCESSOR

CFG0 — R58 3.01K_0402_1%

PCI-Express Configuration Select	
CFG0	1: Single PEG 0: Bifurcation enabled

Not applicable for Clarksfield Processor

CFG[1:0] 11=1*16 PEG
10=2*8 PEG

CFG3 — R61 3.01K_0402_1%

CFG3-PCI Express Static Lane Reversal	
CFG3	1: Normal Operation 0: Lane Numbers Reversed 15 -> 0, 14 ->1, ...

CFG4 — R60 3.01K_0402_1%

CFG4-Display Port Presence	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

Security Classification	Compal Secret Data		
Issued Date	2008/10/31	Deciphered Date	2009/10/31

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Title: Arrandale(2/5)-DMI/PEG/FDI

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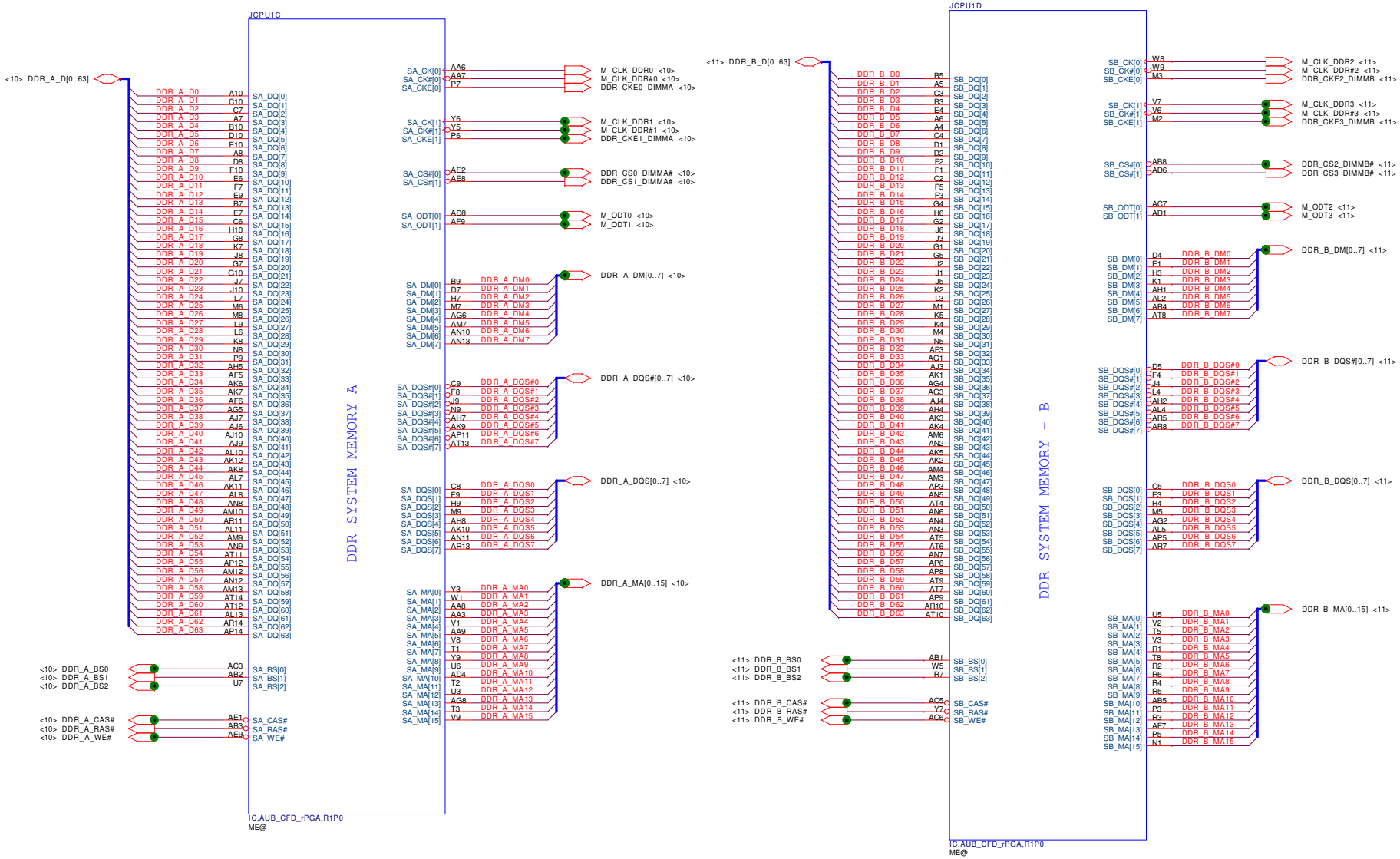

Security Classification	Compal Secret Data		
Issued Date	2008/10/31	Deciphered Date	2009/10/31

Compal Electronics, Inc.

Title: *Arrandale(3/5)-DDR III*

Size	Document Number	Rev
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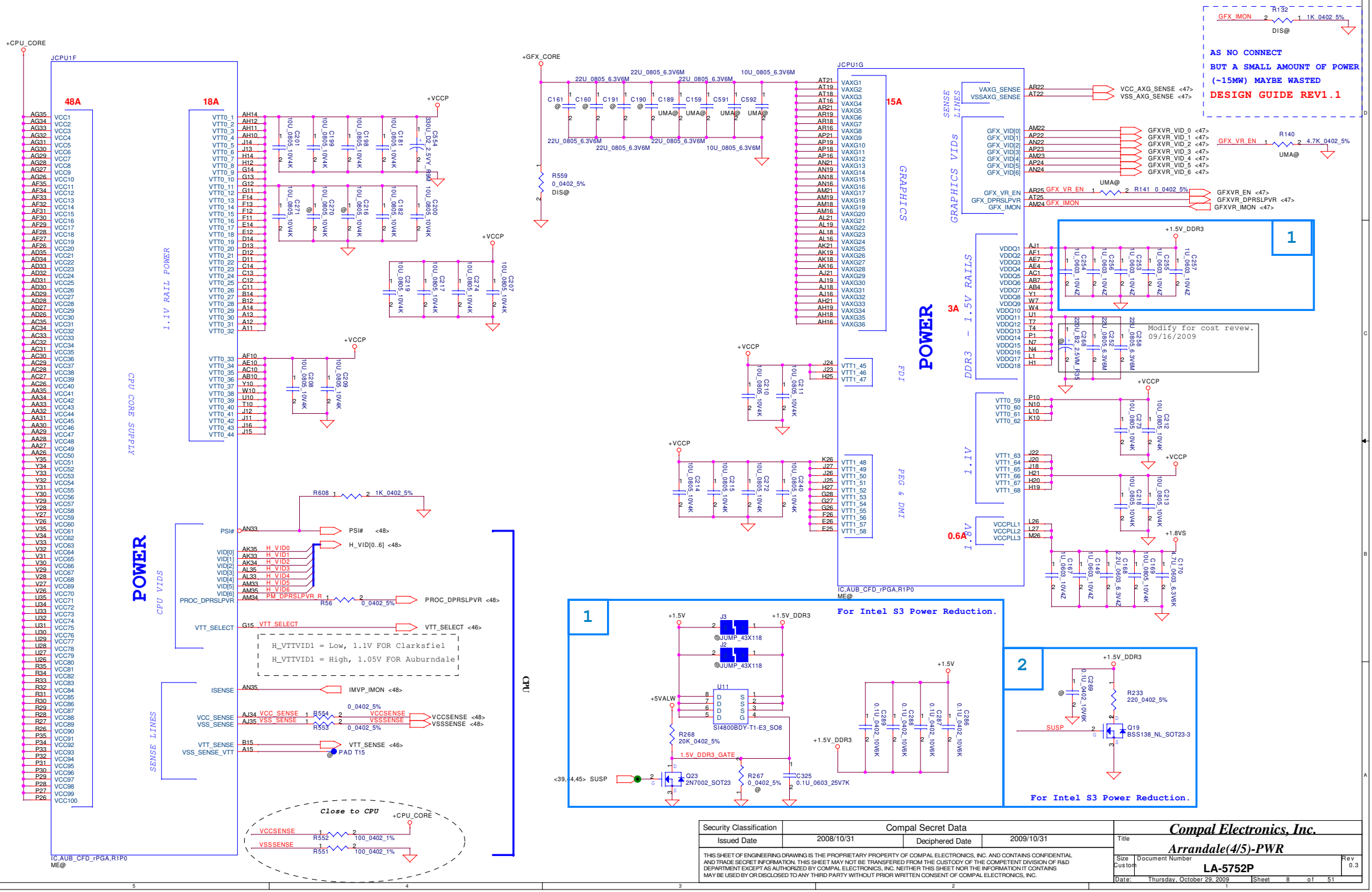

Security Classification	Compal Secret Data		
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Title: Arrandale(4/5)-PWR			
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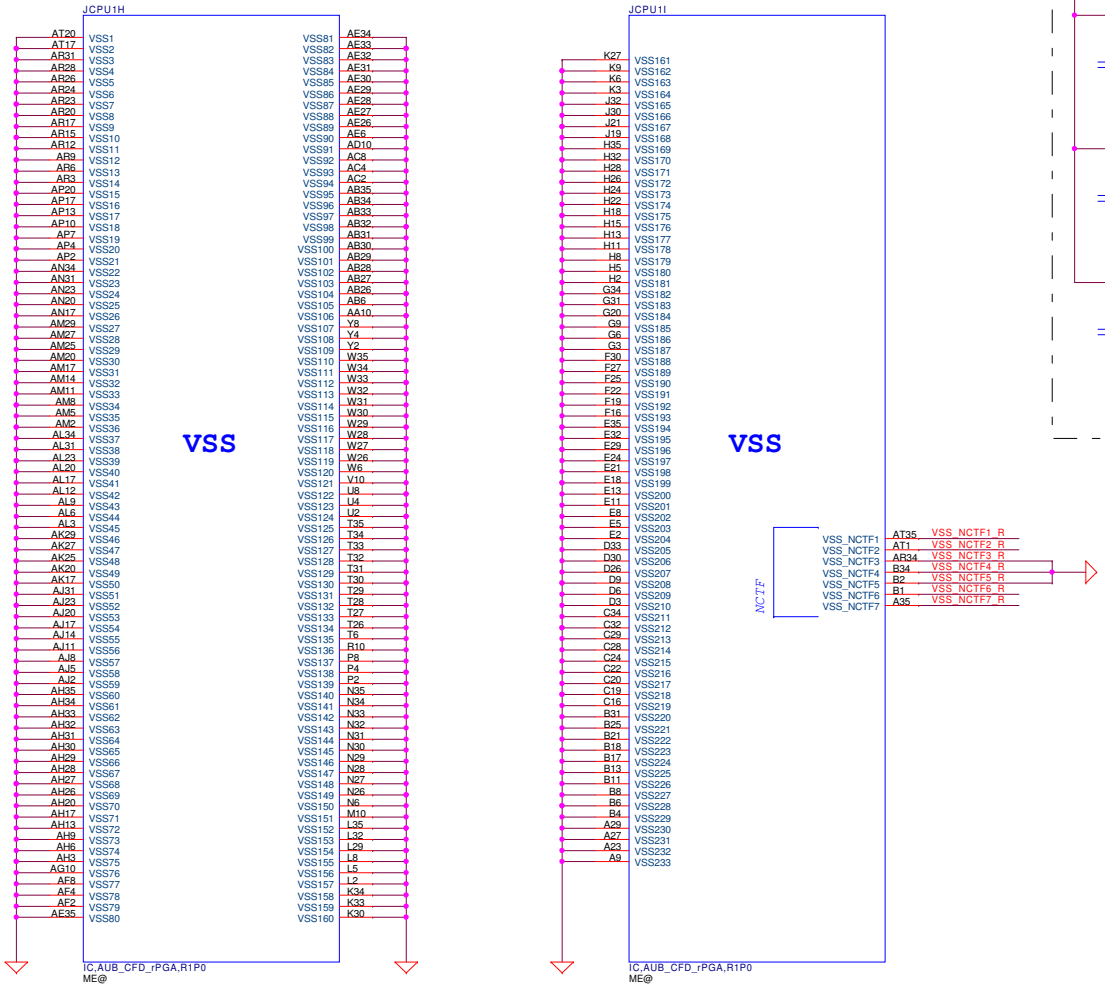

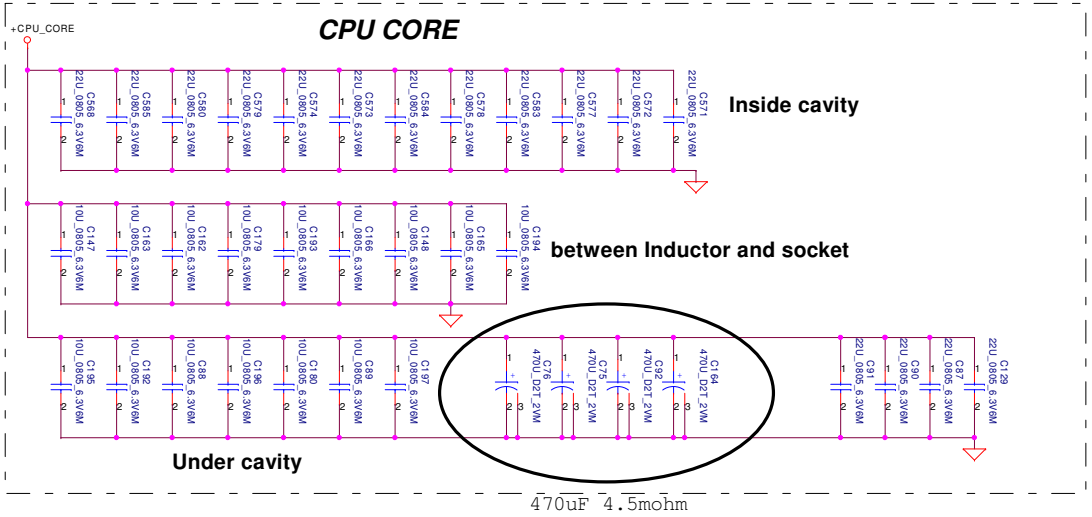

Security Classification	Compal Secret Data		
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Title: *Arrandale(5/5)-GND/Bypass*

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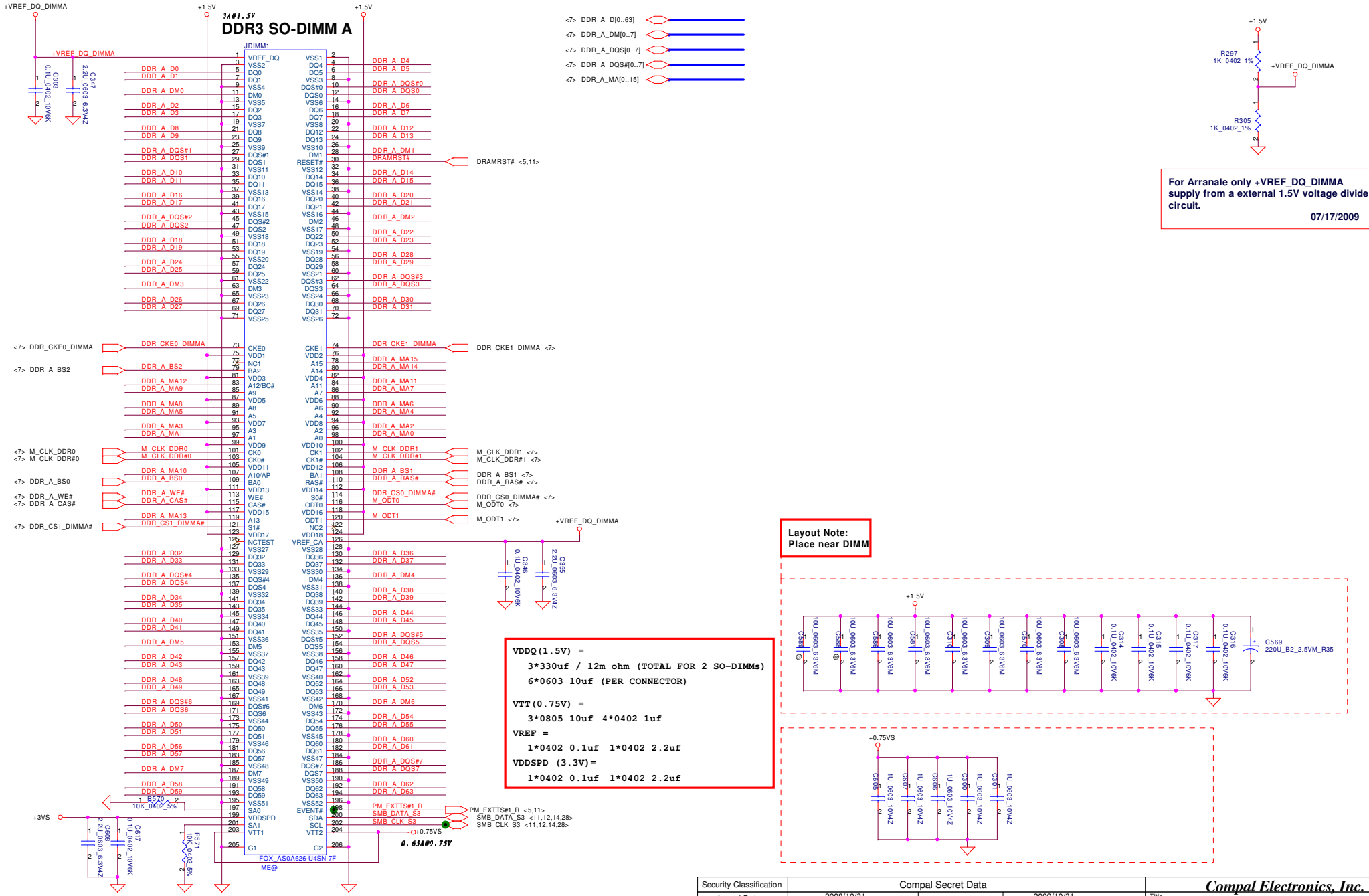
DDR3 SO-DIMM A

JDIMM1

FOX_AS0A626-U4SN-7F

ME@



<7> DDR_A_D[0..63]
<7> DDR_A_DM[0..7]
<7> DDR_A_DQS[0..7]
<7> DDR_A_DQS#[0..7]
<7> DDR_A_MA[0..15]

For Arranale only +VREF_DQ_DIMMA supply from a external 1.5V voltage divide circuit.

07/17/2009

Layout Note: Place near DIMM


```
VDDQ(1.5V) =
  3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)
  6*0603 10uf (PER CONNECTOR)

VTT(0.75V) =
  3*0805 10uf  4*0402 1uf
VREF =
  1*0402 0.1uf  1*0402 2.2uf
VDDSPD (3.3V)=
  1*0402 0.1uf  1*0402 2.2uf
```

Security Classification	Compal Secret Data		
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Title: **DDRIII-SODIMM SLOT1**

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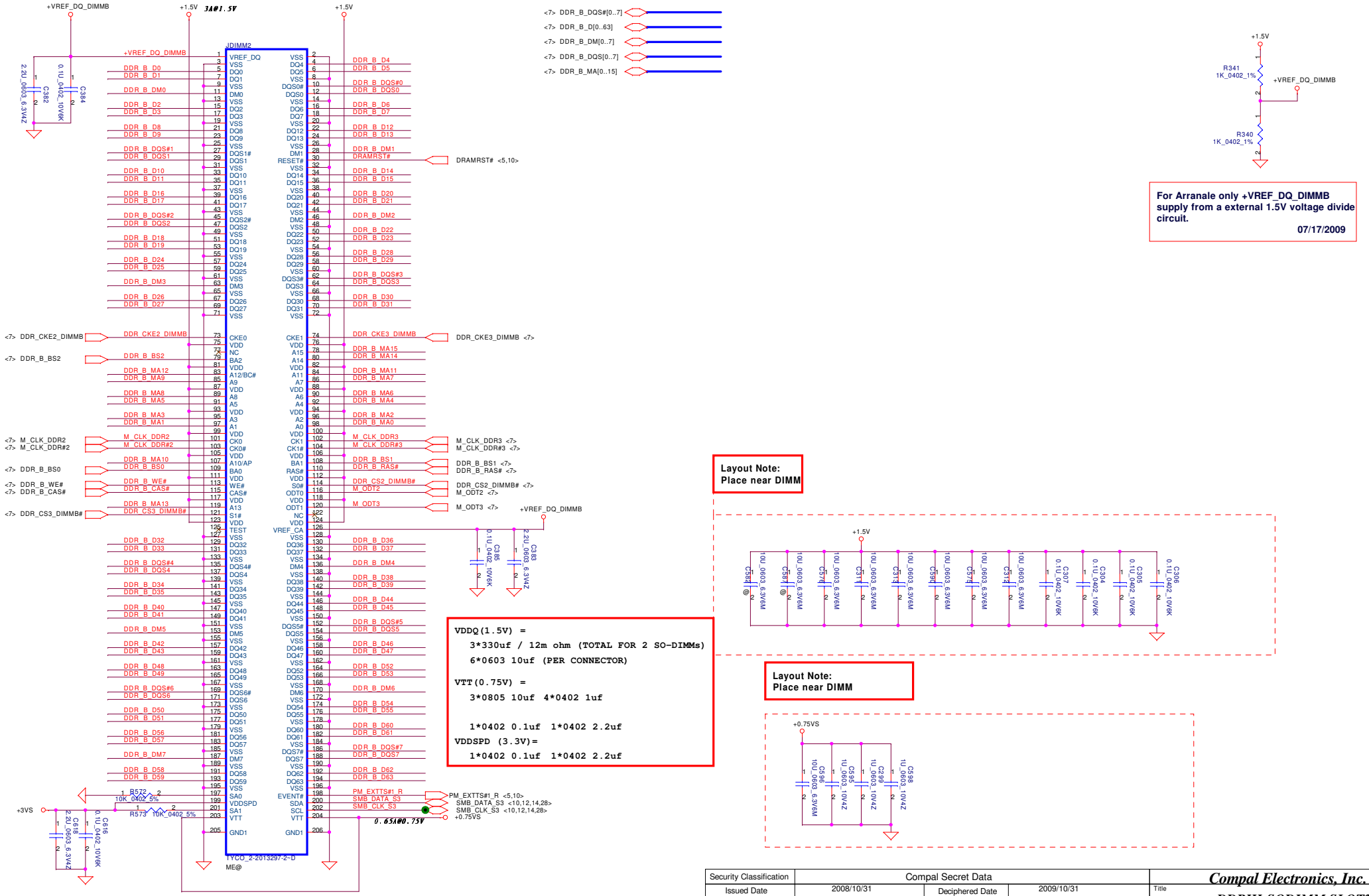

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Title: DDRIII-SODIMM SLOT2

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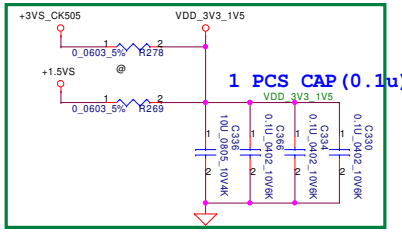
Reserve for Low Power CLK GEN.
RTM890N-632
SLG8LV597VTR

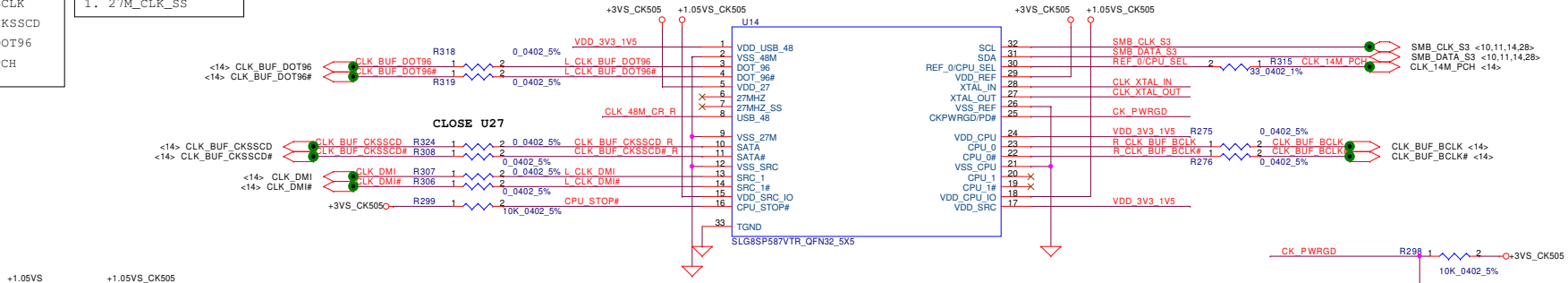


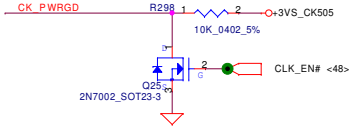
1 PCS CAP(0.1u) BY 1 INPUT PIN

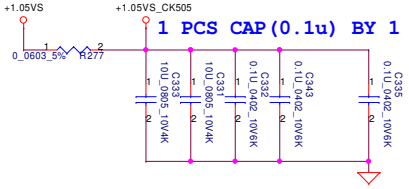
CLK GEN TO PCH
1. CLK_DMI
2. CLK_BUF_BCLK
3. CLK_BUF_CKSSCD
4. CLK_BUF_DOT96
5. CLK_14M_PCH

CLK GEN TO VGA
1. 27M_CLK
1. 27M_CLK_SS

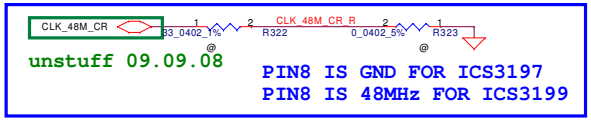
CLOSE U27





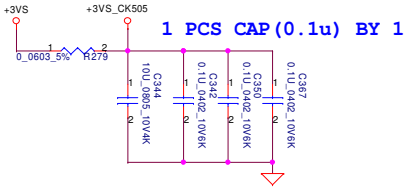


RTM890N-631-GRT QFN 32P CLK GEN (SA00003HQ00)
ICS9LVS3199AKLFT MLF 32P CLK GEN (SA00003HR00)

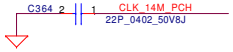


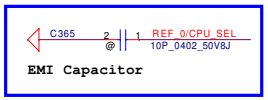
unstuff 09.09.08

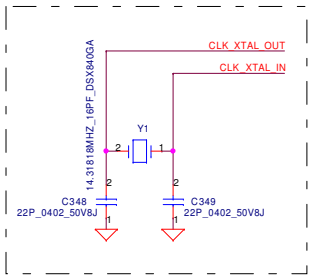
PIN8 IS GND FOR ICS3197
PIN8 IS 48MHz FOR ICS3199



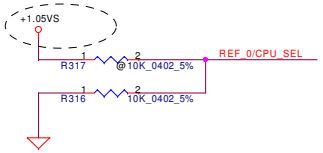
1 PCS CAP(0.1u) BY 1 INPUT PIN







PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz



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Title: CLOCK GENERATOR

Size: | Document Number: LA-5752P | Rev: 0.3

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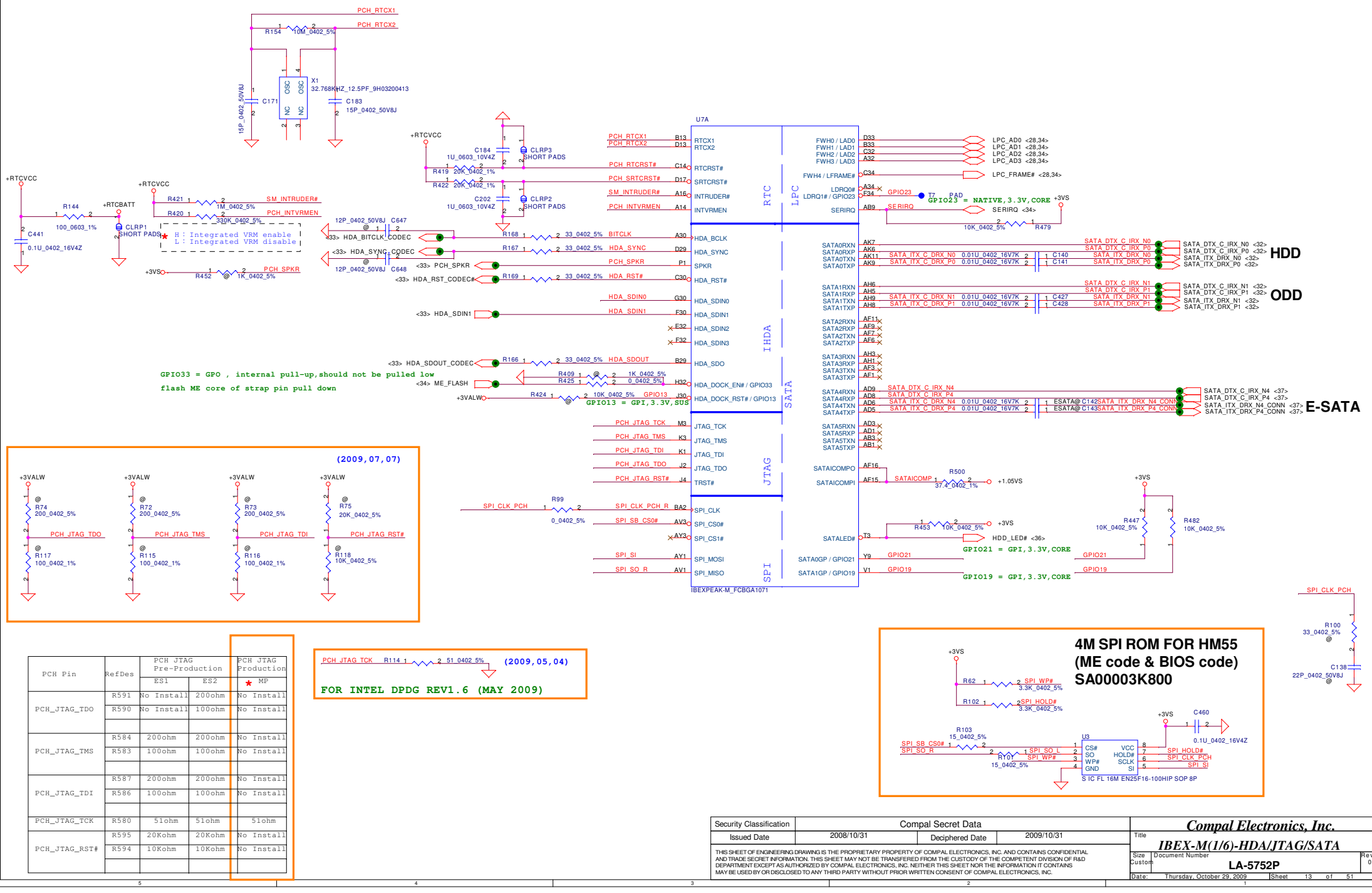


PCH Pin	RefDes	PCH JTAG Pre-Production ES1	PCH JTAG Pre-Production ES2	PCH JTAG Production * MP
PCH_JTAG_TDO	R591	No Install	200ohm	No Install
	R590	No Install	100ohm	No Install
PCH_JTAG_TMS	R584	200ohm	200ohm	No Install
	R583	100ohm	100ohm	No Install
PCH_JTAG_TDI	R587	200ohm	200ohm	No Install
	R586	100ohm	100ohm	No Install
PCH_JTAG_TCK	R580	51ohm	51ohm	51ohm
PCH_JTAG_RST#	R595	20Kohm	20Kohm	No Install
	R594	10Kohm	10Kohm	No Install

Security Classification	Compal Secret Data		
Issued Date	2008/10/31	Deciphered Date	2009/10/31

Compal Electronics, Inc.

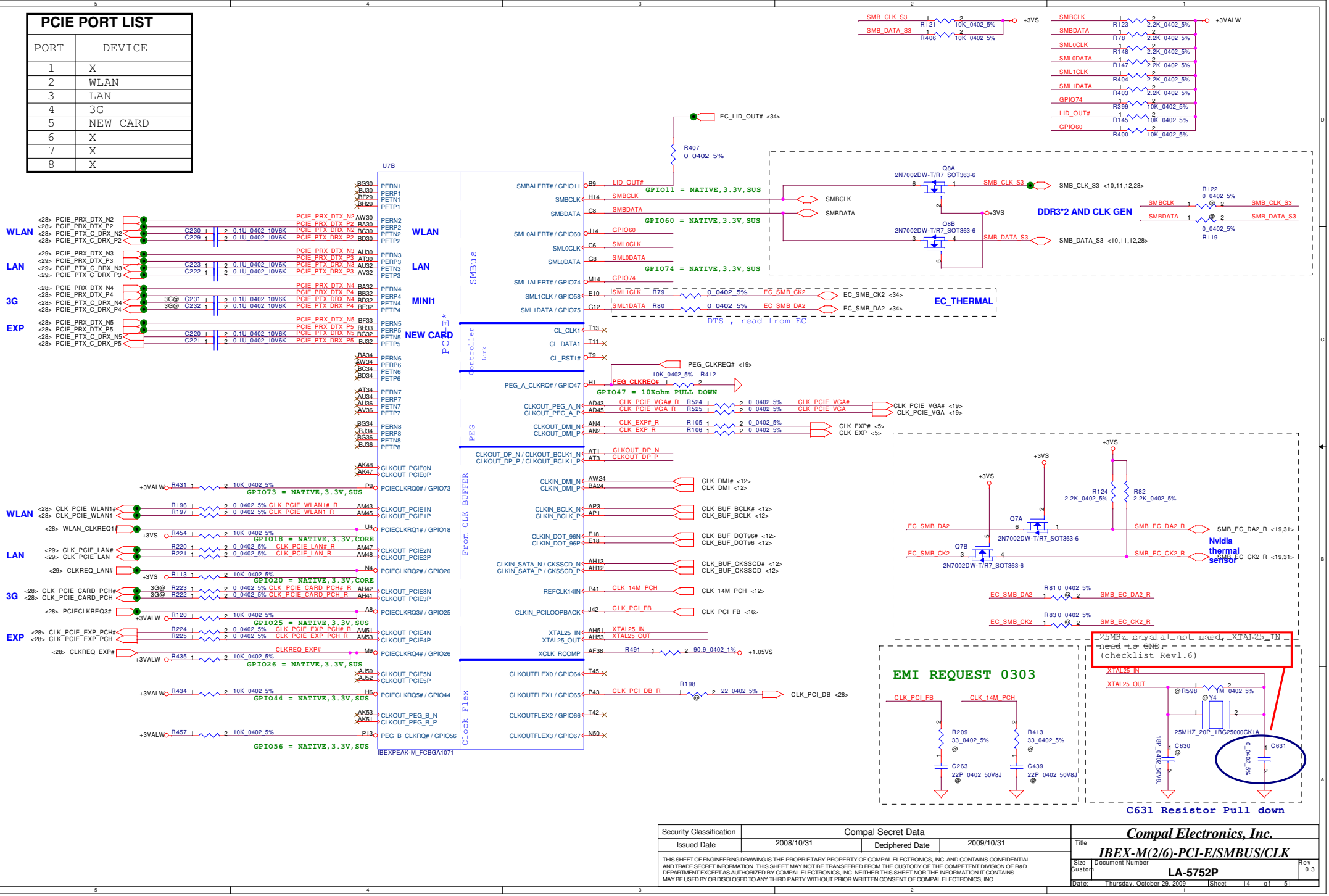
Title: IBEX-M(1/6)-HDA/JTAG/SATA

Size	Document Number	Rev
Custom	LA-5752P	0.3

Date: Thursday, October 29, 2009 Sheet 13 of 51

PCIE PORT LIST

PORT	DEVICE
1	X
2	WLAN
3	LAN
4	3G
5	NEW CARD
6	X
7	X
8	X



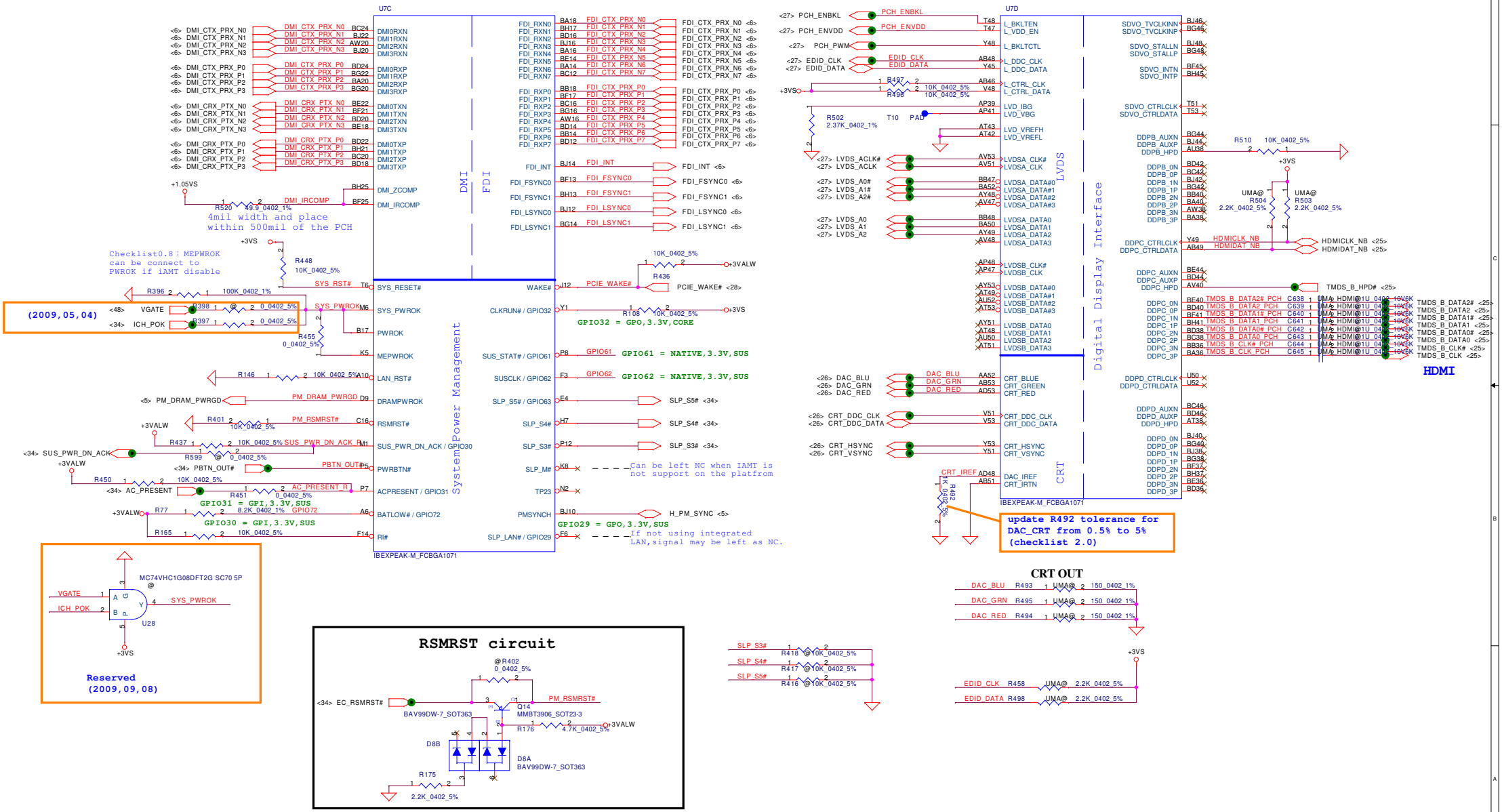
Security Classification	Compal Secret Data		
Issued Date	2008/10/31	Deciphered Date	2009/10/31

Compal Electronics, Inc.

Title: IBEX-M(2/6)-PCI-E/SMBUS/CLK

Size	Document Number	Rev
Custom	LA-5752P	0.3

Date: Thursday, October 29, 2009 | Sheet 14 of 51



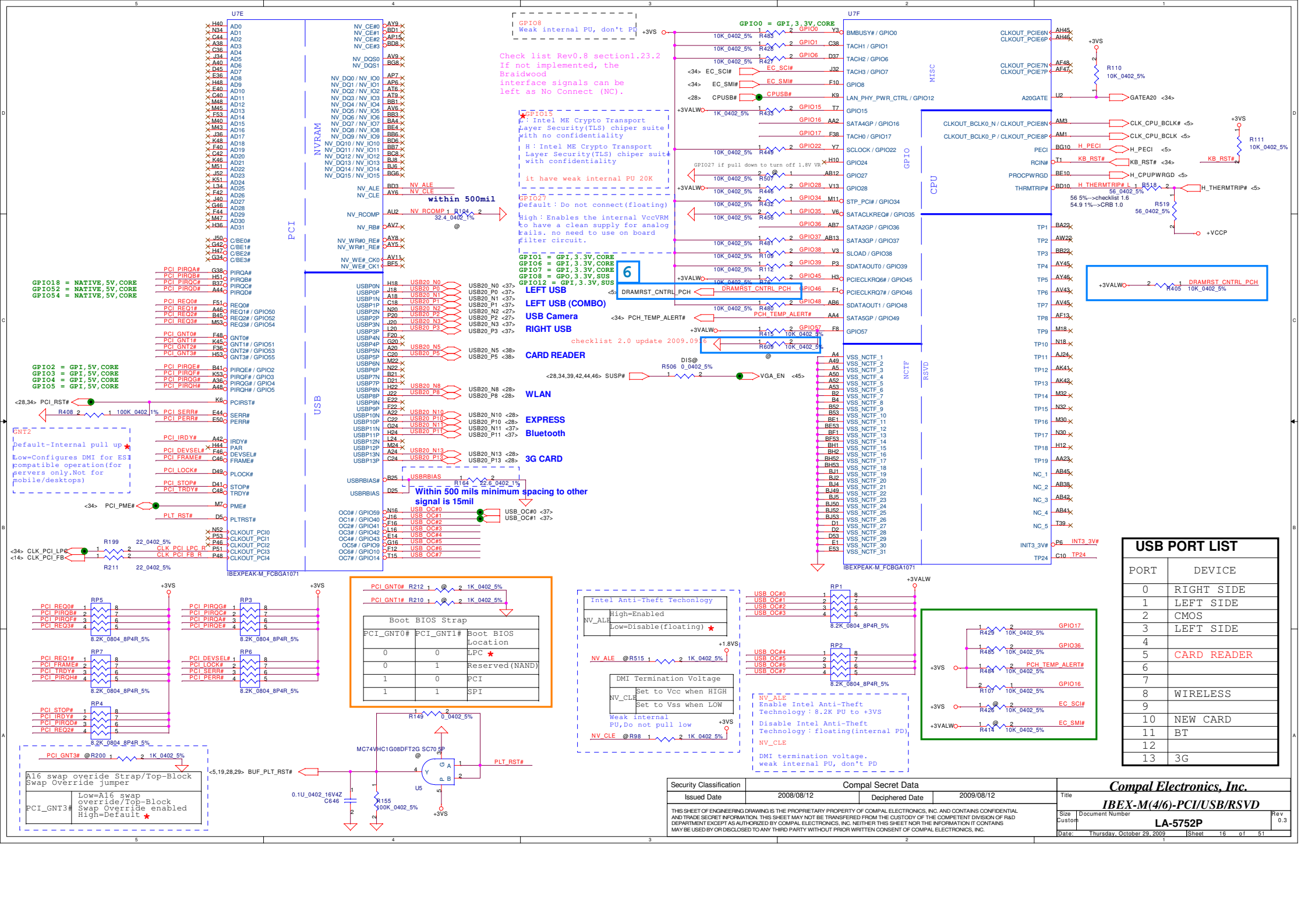
Security Classification	Compal Secret Data		
Issued Date	2008/10/31	Deciphered Date	2009/10/31

Compal Electronics, Inc.

Title: IBEX-M(3/6)-DMI/GPIO/LVDS

Size	Document Number	Rev
Custom	LA-5752P	0.3

Date: Thursday, October 29, 2009 | Sheet 15 of 51


U7E
PCI
NVRAM
USB
IBEXPEAK-M_FCBGA1071
U7F
MISC
GPIO
CPU
NCTF
RSVD
GPIO8
Weak internal PU, don't PD
GPIO0 = GPI,3.3V,CORE
Check list Rev0.8 section1.23.2
If not implemented, the
Braidwood
interface signals can be
left as No Connect (NC).
GPIO15
H : Intel ME Crypto Transport
Layer Security(TLS) chiper suite
with no confidentiality
L : Intel ME Crypto Transport
Layer Security(TLS) chiper suite
with confidentiality
it have weak internal PU 20K
GPIO27
Default : Do not connect(floating)
High : Enables the internal VccVRM
to have a clean supply for analog
rails. no need to use on board
filter circuit.
GPIO1 = GPI,3.3V,CORE
GPIO6 = GPI,3.3V,CORE
GPIO7 = GPI,3.3V,CORE
GPIO8 = GPO,3.3V,SUS
GPIO12 = GPI,3.3V,SUS
within 500mil
GPIO18 = NATIVE,5V,CORE
GPIO52 = NATIVE,5V,CORE
GPIO54 = NATIVE,5V,CORE
GPIO2 = GPI,5V,CORE
GPIO3 = GPI,5V,CORE
GPIO4 = GPI,5V,CORE
GPIO5 = GPI,5V,CORE
GNT2
Default-Internal pull up
Low=Configures DMI for ES1
compatible operation(for
servers only.Not for
mobile/desktops)
LEFT USB
LEFT USB (COMBO)
USB Camera
RIGHT USB
CARD READER
WLAN
EXPRESS
Bluetooth
3G CARD
checklist 2.0 update 2009.09.16
Within 500 mils minimum spacing to other
signal is 15mil
Boot BIOS Strap
PCI_GNT0#
PCI_GNT1#
Boot BIOS Location
0 0 LPC
0 1 Reserved(NAND)
1 0 PCI
1 1 SPI
Intel Anti-Theft Techonlogy
NV_ALE
High=Enabled
Low=Disable(floating)
DMI Termination Voltage
NV_CLE
Set to Vcc when HIGH
Set to Vss when LOW
Weak internal
PU,Do not pull low
NV_ALE
Enable Intel Anti-Theft
Technology : 8.2K PU to +3VS
Disable Intel Anti-Theft
Technology : floating(internal PD)
NV_CLE
DMI termination voltage.
weak internal PU, don't PD
A16 swap overide Strap/Top-Block
Swap Override jumper
PCI_GNT3#
Low=A16 swap override/Top-Block Swap Override enabled
High=Default
MC74VHC1G08DFT2G SC70_5P
USB PORT LIST
PORT DEVICE
0 RIGHT SIDE
1 LEFT SIDE
2 CMOS
3 LEFT SIDE
4
5 CARD READER
6
7
8 WIRELESS
9
10 NEW CARD
11 BT
12
13 3G
Security Classification
Compal Secret Data
Issued Date
2008/08/12
Deciphered Date
2009/08/12
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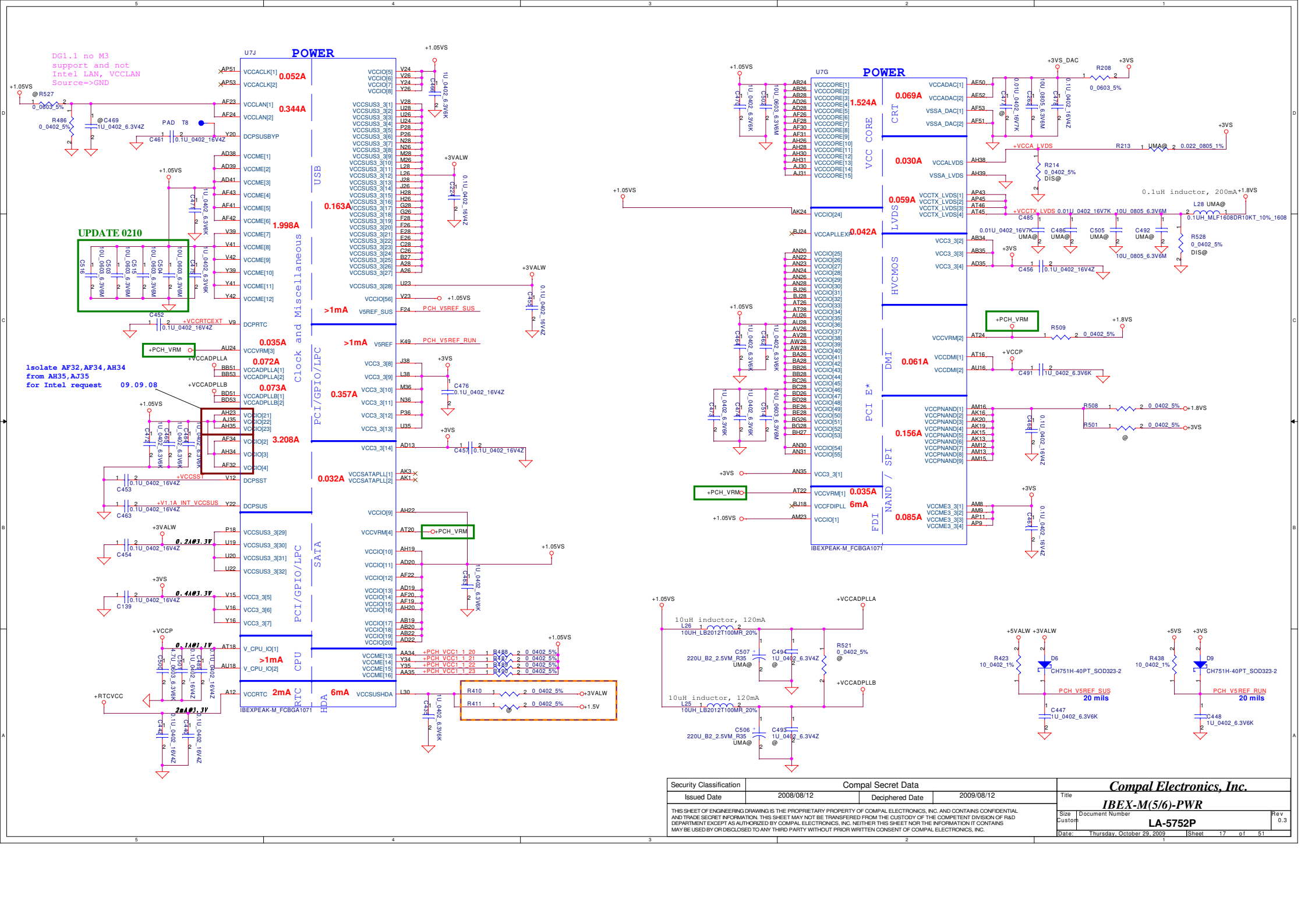
Compal Electronics, Inc.
Title
IBEX-M(4/6)-PCI/USB/RSVD
Size Custom
Document Number
LA-5752P
Rev 0.3
Date: Thursday, October 29, 2009
Sheet 16 of 51


DG1.1 no M3 support and not Intel LAN, VCCLAN Source=>GND
POWER
U7J
U7G
UPDATE 0210
lsolate AF32,AF34,AH34 from AH35,AJ35 for Intel request 09.09.08
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
CRT
VCC CORE
LVDS
HVCMOS
DMI
PCI E*
SPI
NAND / FDI
0.052A
0.344A
1.998A
0.163A
0.035A
0.072A
0.073A
3.208A
0.357A
0.032A
1.524A
0.069A
0.030A
0.059A
0.042A
0.061A
0.156A
0.085A
6mA
2mA
>1mA
IBEXPEAK-M_FCBGA1071
10uH inductor, 120mA
0.1uH inductor, 200mA
Security Classification
Compal Secret Data
Issued Date
2008/08/12
Deciphered Date
2009/08/12
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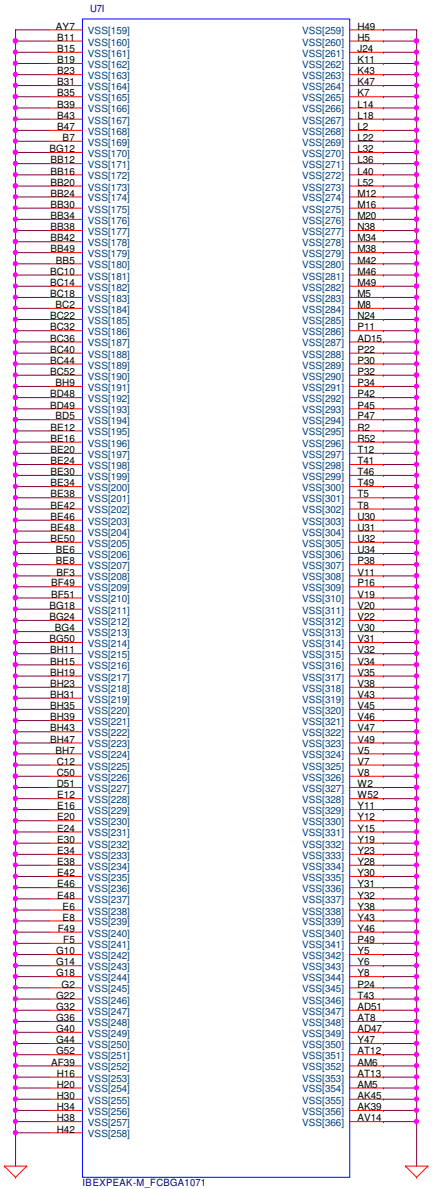
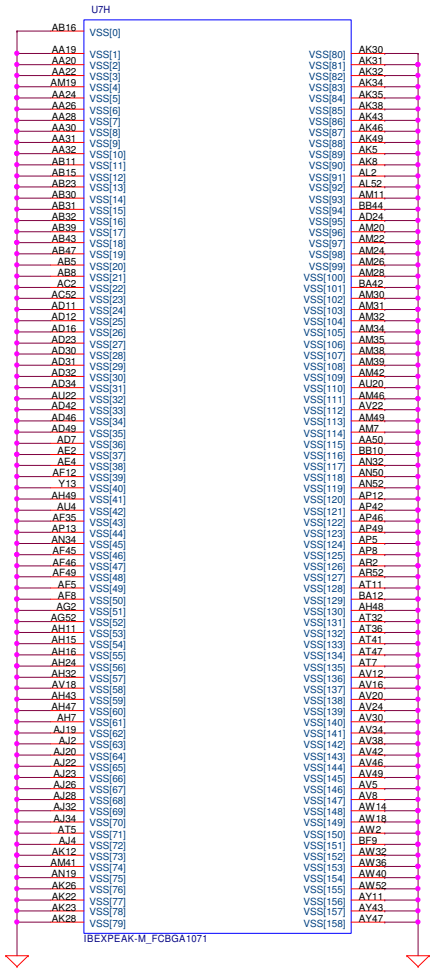
Compal Electronics, Inc.
Title
IBEX-M(5/6)-PWR
Size Custom
Document Number
LA-5752P
Rev 0.3
Date: Thursday, October 29, 2009
Sheet 17 of 51





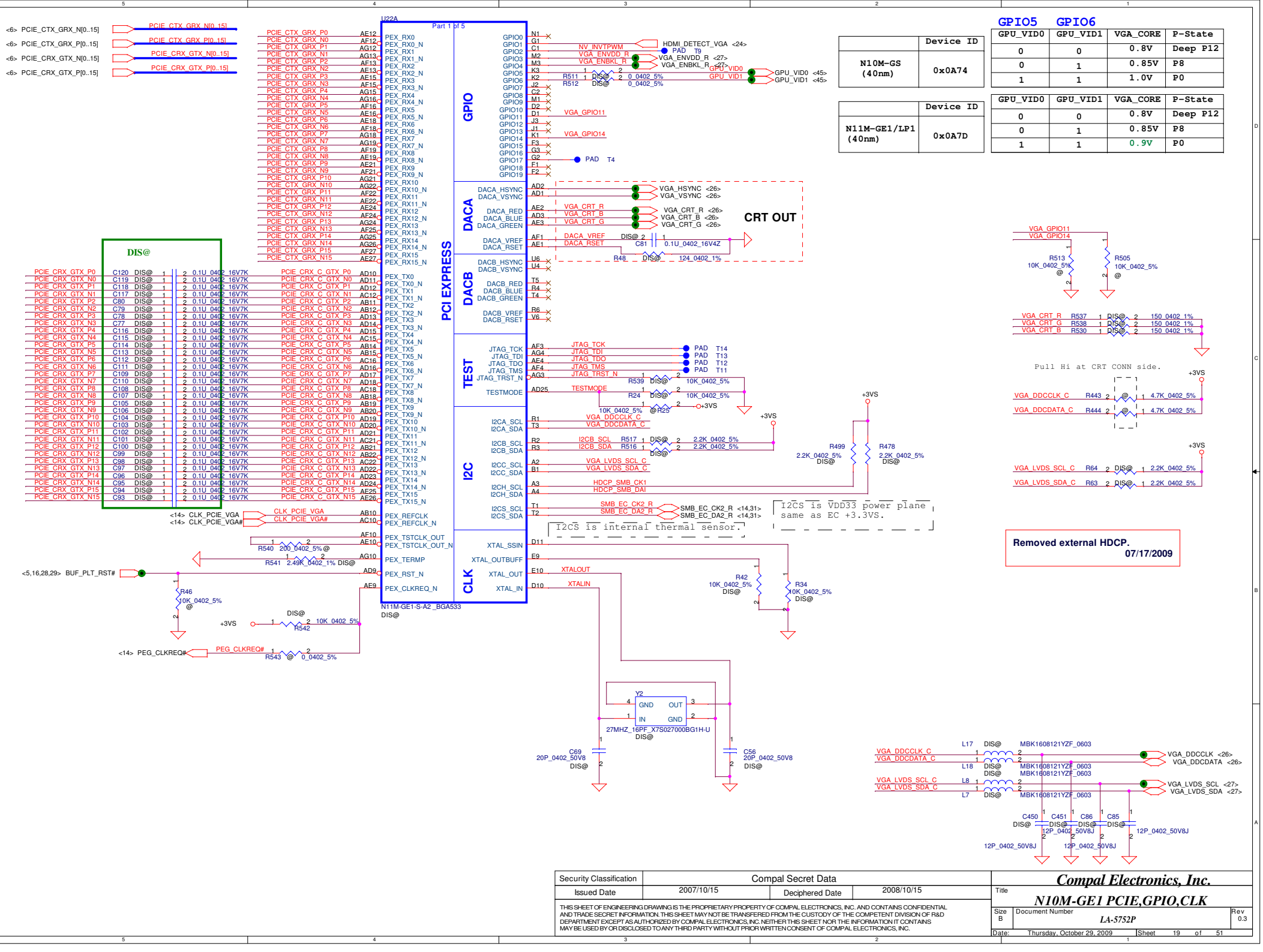
Security Classification	Compal Secret Data		
Issued Date	2008/10/31	Deciphered Date	2009/10/31

Compal Electronics, Inc.

Title: **IBEX-M(6/6)-GND**

Size	Document Number	Rev
Custom	LA-5752P	0.3

Date: Thursday, October 29, 2009 | Sheet 18 of 51


GPIO5 GPIO6
GPU_VID0 GPU_VID1 VGA_CORE P-State
0 0 0.8V Deep P12
0 1 0.85V P8
1 1 1.0V P0
Device ID
N10M-GS (40nm) 0x0A74
N11M-GE1/LP1 (40nm) 0x0A7D
GPU_VID0 GPU_VID1 VGA_CORE P-State
0 0 0.8V Deep P12
0 1 0.85V P8
1 1 0.9V P0
U22A
Part 1 of 5
PCI EXPRESS
GPIO
DACA
DACB
TEST
I2C
CLK
PEX_RX0 PEX_RX0_N PEX_RX1 PEX_RX1_N PEX_RX2 PEX_RX2_N PEX_RX3 PEX_RX3_N PEX_RX4 PEX_RX4_N PEX_RX5 PEX_RX5_N PEX_RX6 PEX_RX6_N PEX_RX7 PEX_RX7_N PEX_RX8 PEX_RX8_N PEX_RX9 PEX_RX9_N PEX_RX10 PEX_RX10_N PEX_RX11 PEX_RX11_N PEX_RX12 PEX_RX12_N PEX_RX13 PEX_RX13_N PEX_RX14 PEX_RX14_N PEX_RX15 PEX_RX15_N
PEX_TX0 PEX_TX0_N PEX_TX1 PEX_TX1_N PEX_TX2 PEX_TX2_N PEX_TX3 PEX_TX3_N PEX_TX4 PEX_TX4_N PEX_TX5 PEX_TX5_N PEX_TX6 PEX_TX6_N PEX_TX7 PEX_TX7_N PEX_TX8 PEX_TX8_N PEX_TX9 PEX_TX9_N PEX_TX10 PEX_TX10_N PEX_TX11 PEX_TX11_N PEX_TX12 PEX_TX12_N PEX_TX13 PEX_TX13_N PEX_TX14 PEX_TX14_N PEX_TX15 PEX_TX15_N
PEX_REFCLK PEX_REFCLK_N
PEX_TSTCLK_OUT PEX_TSTCLK_OUT_N
PEX_TERMP
PEX_RST_N
PEX_CLKREQ_N
N11M-GE1-S-A2_BGA533
DIS@
GPIO0 GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 GPIO6 GPIO7 GPIO8 GPIO9 GPIO10 GPIO11 GPIO12 GPIO13 GPIO14 GPIO15 GPIO16 GPIO17 GPIO18 GPIO19
DACA_HSYNC DACA_VSYNC DACA_RED DACA_BLUE DACA_GREEN DACA_VREF DACA_RSET
DACB_HSYNC DACB_VSYNC DACB_RED DACB_BLUE DACB_GREEN DACB_VREF DACB_RSET
JTAG_TCK JTAG_TDI JTAG_TDO JTAG_TMS JTAG_TRST_N TESTMODE
I2CA_SCL I2CA_SDA I2CB_SCL I2CB_SDA I2CC_SCL I2CC_SDA I2CH_SCL I2CH_SDA I2CS_SCL I2CS_SDA
XTAL_SSIN XTAL_OUTBUFF XTAL_OUT XTAL_IN
CRT OUT
VGA_HSYNC VGA_VSYNC VGA_CRT_R VGA_CRT_B VGA_CRT_G
DACA_VREF DACA_RSET C81 0.1U_0402_16V4Z R48 124_0402_1%
VGA_GPIO11 VGA_GPIO14 R513 10K_0402_5% R505 10K_0402_5%
VGA_CRT_R R537 150_0402_1%
VGA_CRT_G R538 150_0402_1%
VGA_CRT_B R530 150_0402_1%
Pull Hi at CRT CONN side.
VGA_DDCCLK_C R443 4.7K_0402_5%
VGA_DDCDATA_C R444 4.7K_0402_5%
VGA_LVDS_SCL_C R64 2.2K_0402_5%
VGA_LVDS_SDA_C R63 2.2K_0402_5%
I2CS is VDD33 power plane same as EC +3.3VS.
I2CS is internal thermal sensor.
Removed external HDCP.
07/17/2009
DIS@
PCIE_CRX_GTX_P0 C120 DIS@ 0.1U_0402_16V7K PCIE_CRX_C_GTX_P0
PCIE_CRX_GTX_N0 C119 DIS@ 0.1U_0402_16V7K PCIE_CRX_C_GTX_N0
PCIE_CRX_GTX_P1 C118 DIS@ 0.1U_0402_16V7K PCIE_CRX_C_GTX_P1
PCIE_CRX_GTX_N1 C117 DIS@ 0.1U_0402_16V7K PCIE_CRX_C_GTX_N1
PCIE_CRX_GTX_P2 C80 DIS@ 0.1U_0402_16V7K PCIE_CRX_C_GTX_P2
PCIE_CRX_GTX_N2 C79 DIS@ 0.1U_0402_16V7K PCIE_CRX_C_GTX_N2
PCIE_CRX_GTX_P3 C78 DIS@ 0.1U_0402_16V7K PCIE_CRX_C_GTX_P3
PCIE_CRX_GTX_N3 C77 DIS@ 0.1U_0402_16V7K PCIE_CRX_C_GTX_N3
PCIE_CRX_GTX_P4 C116 DIS@ 0.1U_0402_16V7K PCIE_CRX_C_GTX_P4
PCIE_CRX_GTX_N4 C115 DIS@ 0.1U_0402_16V7K PCIE_CRX_C_GTX_N4
PCIE_CRX_GTX_P5 C114 DIS@ 0.1U_0402_16V7K PCIE_CRX_C_GTX_P5
PCIE_CRX_GTX_N5 C113 DIS@ 0.1U_0402_16V7K PCIE_CRX_C_GTX_N5
PCIE_CRX_GTX_P6 C112 DIS@ 0.1U_0402_16V7K PCIE_CRX_C_GTX_P6
PCIE_CRX_GTX_N6 C111 DIS@ 0.1U_0402_16V7K PCIE_CRX_C_GTX_N6
PCIE_CRX_GTX_P7 C109 DIS@ 0.1U_0402_16V7K PCIE_CRX_C_GTX_P7
PCIE_CRX_GTX_N7 C110 DIS@ 0.1U_0402_16V7K PCIE_CRX_C_GTX_N7
PCIE_CRX_GTX_P8 C108 DIS@ 0.1U_0402_16V7K PCIE_CRX_C_GTX_P8
PCIE_CRX_GTX_N8 C107 DIS@ 0.1U_0402_16V7K PCIE_CRX_C_GTX_N8
PCIE_CRX_GTX_P9 C105 DIS@ 0.1U_0402_16V7K PCIE_CRX_C_GTX_P9
PCIE_CRX_GTX_N9 C106 DIS@ 0.1U_0402_16V7K PCIE_CRX_C_GTX_N9
PCIE_CRX_GTX_P10 C104 DIS@ 0.1U_0402_16V7K PCIE_CRX_C_GTX_P10
PCIE_CRX_GTX_N10 C103 DIS@ 0.1U_0402_16V7K PCIE_CRX_C_GTX_N10
PCIE_CRX_GTX_P11 C102 DIS@ 0.1U_0402_16V7K PCIE_CRX_C_GTX_P11
PCIE_CRX_GTX_N11 C101 DIS@ 0.1U_0402_16V7K PCIE_CRX_C_GTX_N11
PCIE_CRX_GTX_P12 C100 DIS@ 0.1U_0402_16V7K PCIE_CRX_C_GTX_P12
PCIE_CRX_GTX_N12 C99 DIS@ 0.1U_0402_16V7K PCIE_CRX_C_GTX_N12
PCIE_CRX_GTX_P13 C98 DIS@ 0.1U_0402_16V7K PCIE_CRX_C_GTX_P13
PCIE_CRX_GTX_N13 C97 DIS@ 0.1U_0402_16V7K PCIE_CRX_C_GTX_N13
PCIE_CRX_GTX_P14 C96 DIS@ 0.1U_0402_16V7K PCIE_CRX_C_GTX_P14
PCIE_CRX_GTX_N14 C95 DIS@ 0.1U_0402_16V7K PCIE_CRX_C_GTX_N14
PCIE_CRX_GTX_P15 C94 DIS@ 0.1U_0402_16V7K PCIE_CRX_C_GTX_P15
PCIE_CRX_GTX_N15 C93 DIS@ 0.1U_0402_16V7K PCIE_CRX_C_GTX_N15
<6> PCIE_CTX_GRX_N[0..15]
<6> PCIE_CTX_GRX_P[0..15]
<6> PCIE_CRX_GTX_N[0..15]
<6> PCIE_CRX_GTX_P[0..15]
<14> CLK_PCIE_VGA
<14> CLK_PCIE_VGA#
R540 200_0402_5%@
R541 2.49K_0402_1% DIS@
<5,16,28,29> BUF_PLT_RST#
R46 10K_0402_5% @
+3VS
R542 10K_0402_5%
<14> PEG_CLKREQ#
R543 @ 0_0402_5%
R539 10K_0402_5%
R24 10K_0402_5%
R25 @
R499 2.2K_0402_5% DIS@
R478 2.2K_0402_5% DIS@
R42 10K_0402_5% DIS@
R34 10K_0402_5% DIS@
Y2 GND OUT IN GND
27MHZ_16PF_X7S027000BG1H-U DIS@
C69 20P_0402_50V8 DIS@
C56 20P_0402_50V8 DIS@
L17 L18 L8 L7 MBK1608121YZF_0603
VGA_DDCCLK <26>
VGA_DDCDATA <26>
VGA_LVDS_SCL <27>
VGA_LVDS_SDA <27>
C450 C451 C86 C85 12P_0402_50V8J
Security Classification
Compal Secret Data
Issued Date 2007/10/15
Deciphered Date 2008/10/15
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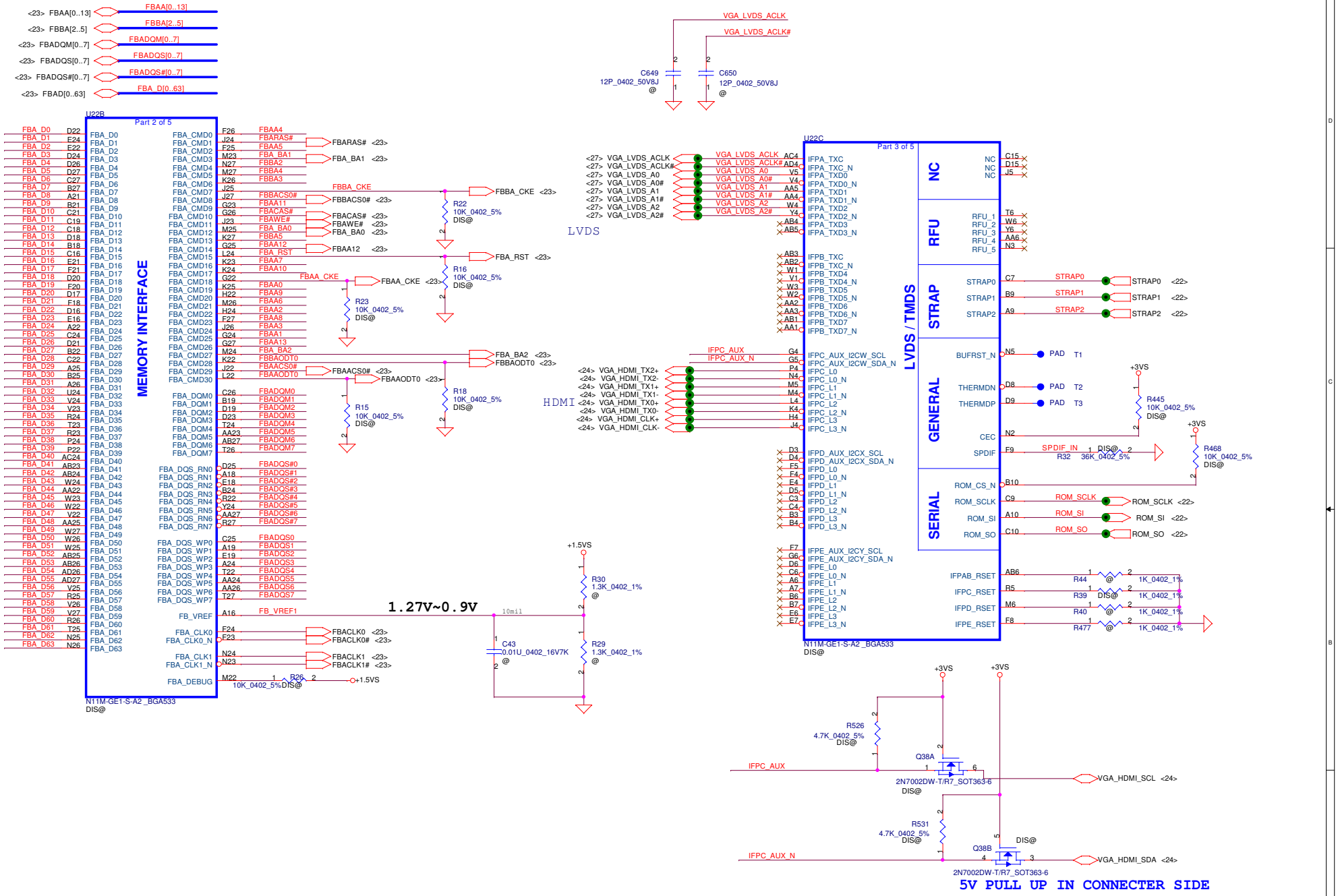
Compal Electronics, Inc.
Title
N10M-GE1 PCIE,GPIO,CLK
Size B
Document Number LA-5752P
Rev 0.3
Date: Thursday, October 29, 2009
Sheet 19 of 51



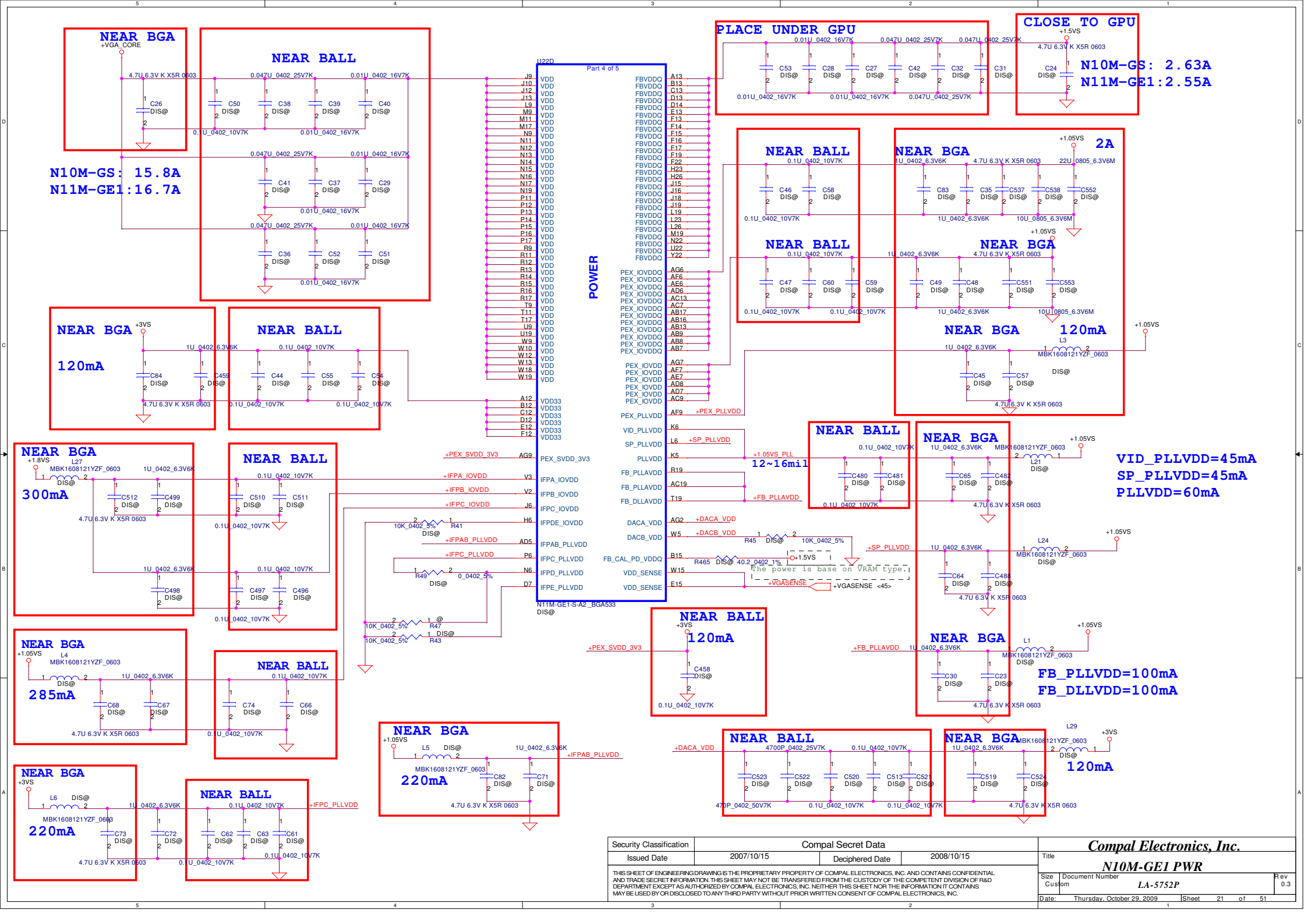
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **N10M-GE1 LVDS,Memory Bus**

Size	Document Number	Rev
B	LA-5752P	0.3

Date: Thursday, October 29, 2009 Sheet 20 of 51



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

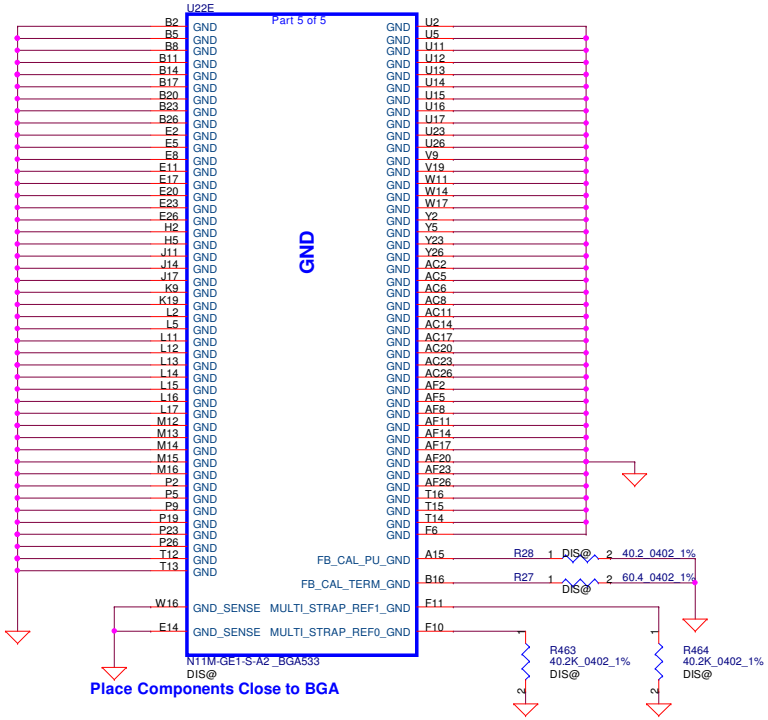
Compal Electronics, Inc.

Title: **N10M-GE1 PWR**

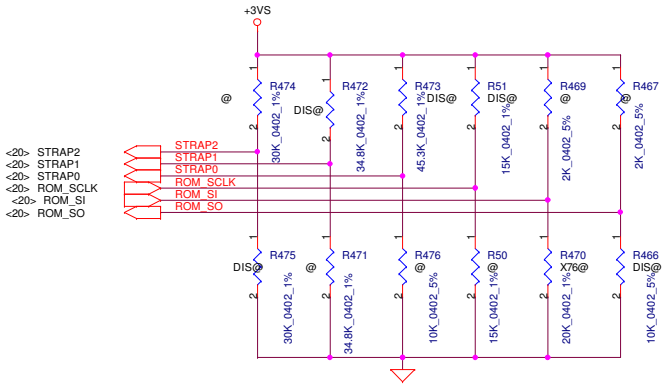
Size	Document Number	Rev
Custom	LA-5752P	0.3

Date: Thursday, October 29, 2009 Sheet 21 of 51

A total of 8 signals are required for GB1 strapping this includes
2 reference signals
6 physical strapping pins
4 logical strapping bits
A total of 24 logical strapping bits are available



Place Components Close to BGA



STRAP1 use for 3GIO_PADCFG to set 35K pull up.
(PUN-04335-001_V10 HW9 update)

GPU	FB Memory (DDR3)		ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N11M-GE1 LP1 (0x0A7D) 40nm	Samsung 800MHz (defaul)	K4W1G1646E-HC12						
		64Mx16	PD 10K	PD 15K	PD 20K	PU 30K	PU 35K	PU 45K
	Hynix 800MHz	H5TQ1G63BFR-12C						
		64Mx16	PD 10K	PD 15K	PD 15K	PU 30K	PU 35K	PU 45K
					X76			

N11M-GE1 LP1	Memory/PKG	FBVDDQ	FB_CAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
	DDR3	+1.5VS	40.2 ohm	40.2 ohm	40.2/60.4 ohm

Must be used 1% resister for driver calibration

DG-04642-001-V01(May 22, 2009)

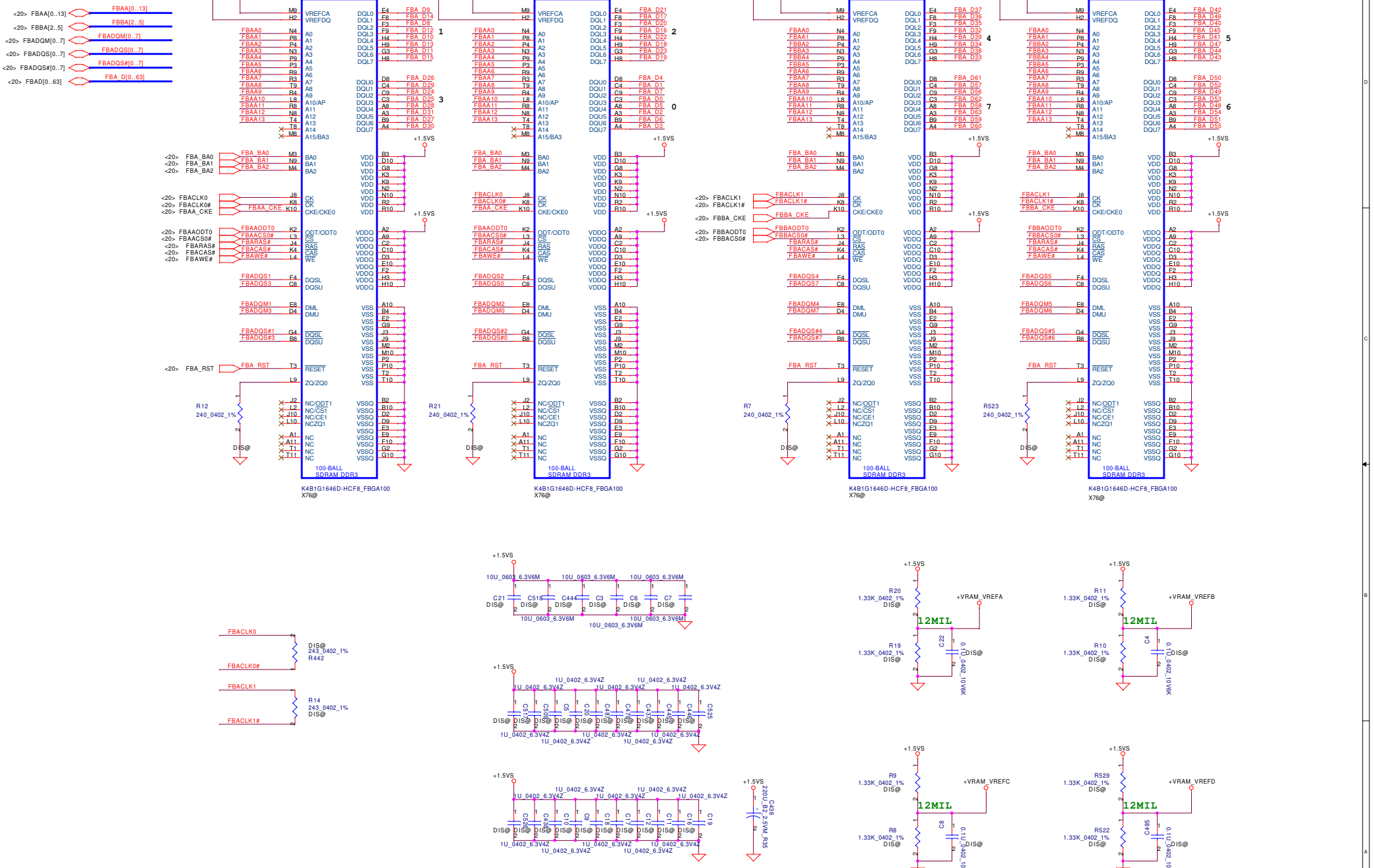
Compal Electronics, Inc.

Title: N10M-GE1 GND & STRAP

Size: B | Document Number: LA-5752P | Rev: 0.3

Date: Thursday, October 29, 2009 | Sheet 22 of 51

N10x 40nm DDR3 MAPPING
NVIDIA COCUMENT FOR DA-3978-001



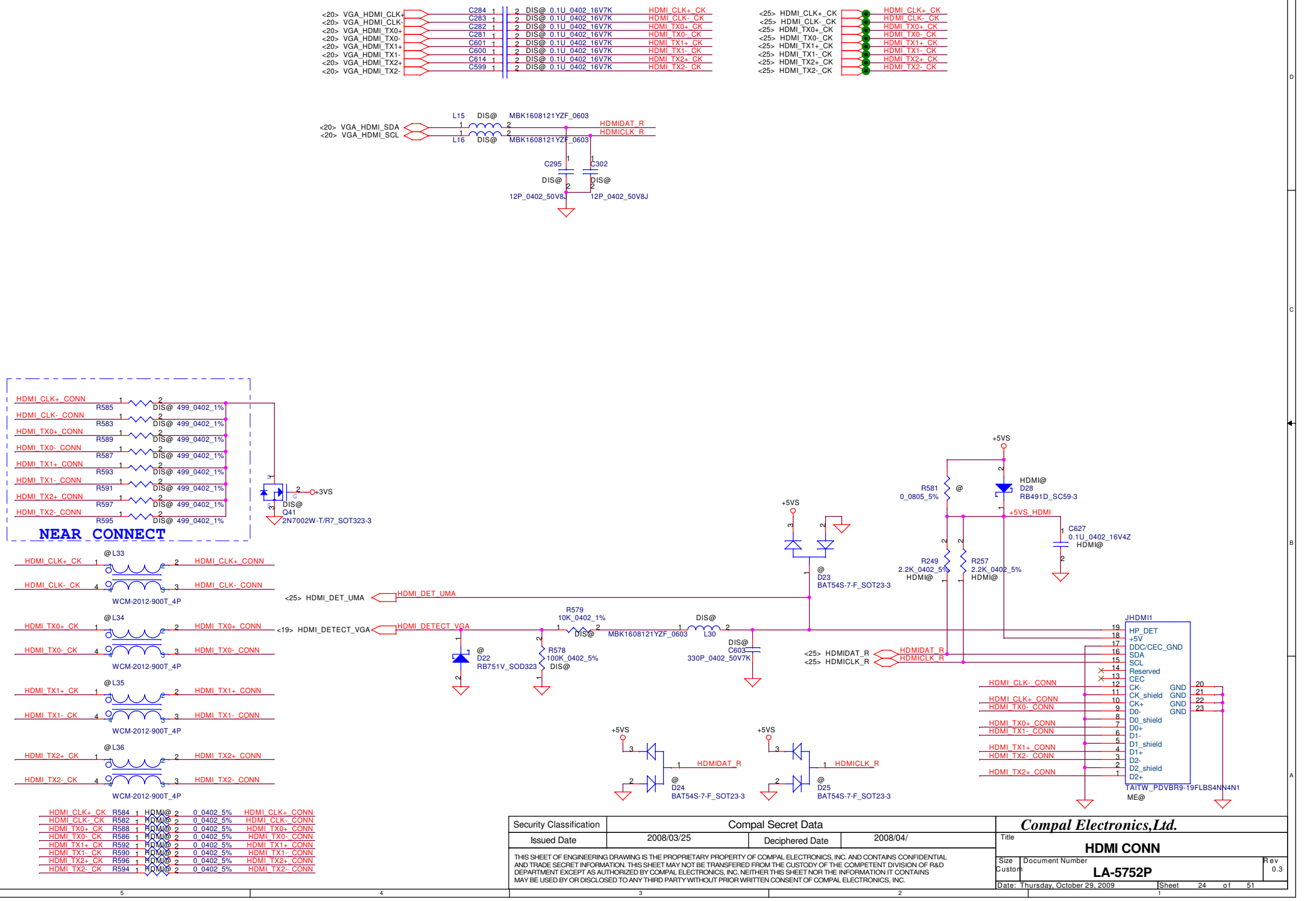
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **VRAM DDR3**

Size	Document Number	Rev
C	LA-5752P	0.3

Date: Thursday, October 29, 2009 Sheet 23 of 51



Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

Compal Electronics,Ltd.

Title: HDMI CONN

Size: Custom | Document Number: LA-5752P | Rev: 0.3

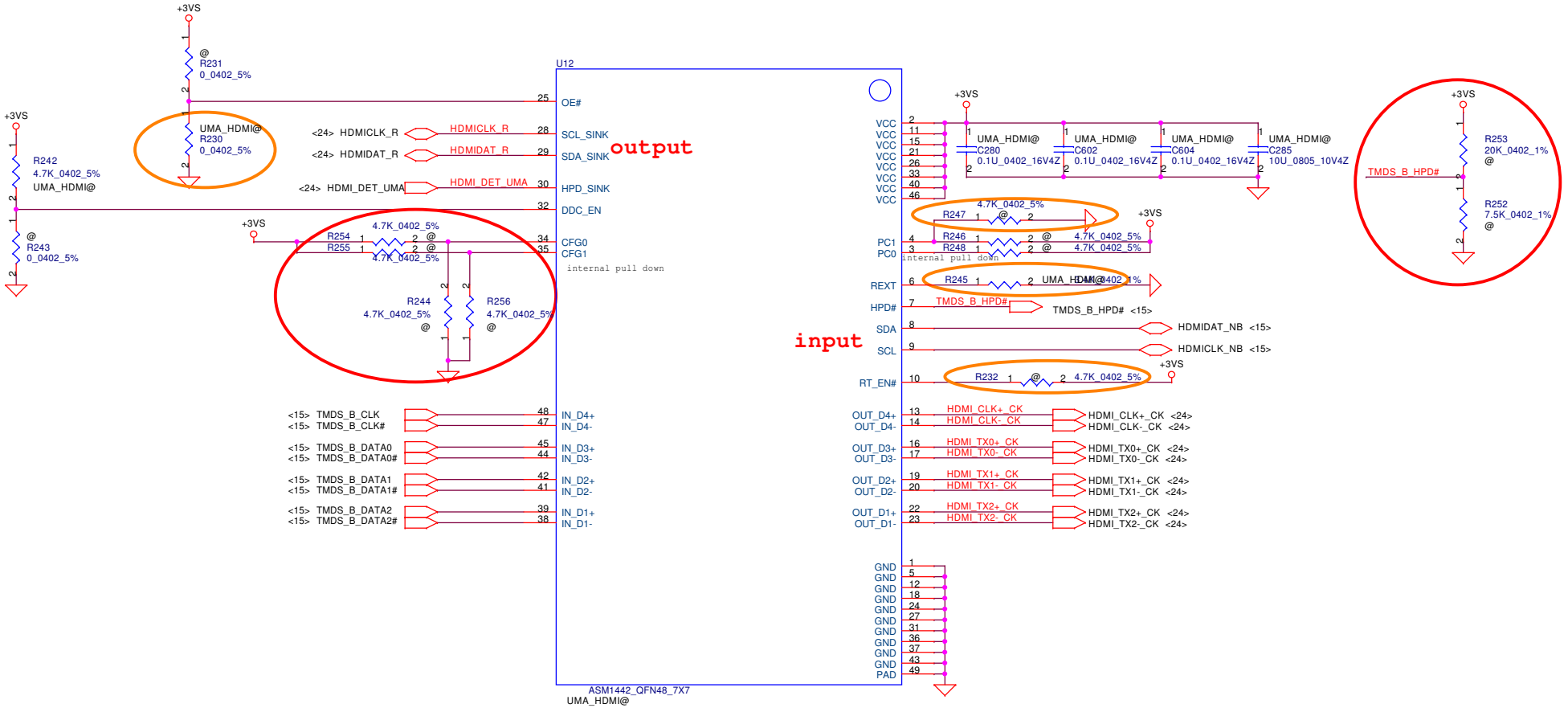
Date: Thursday, October 29, 2009 | Sheet 24 of 51

P/N:SA00003GT00 (ASM1442)

FOR asmedia R428 STUFF
RESERVE THE R668 PULL UP TO 3VS
RESERVE THE R670 PULL DOWN TO GND
CHANGE R483 FROM 499 TO 3.4K OHM

P/N:SA00002D700 (8101T)
P/N:SA00001U900 (CH7318A)

FOR 7318C PIN6 PULL DOWN 1.2Kohm
PIN7 PULL DOWN 7.5Kohm
PIN7 PULL UP 20Kohm



Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

Compal Electronics,Ltd.

Title: Level Shiftter_ASM1442

Size: Custom | Document Number: LA-5752P | Rev: 0.3

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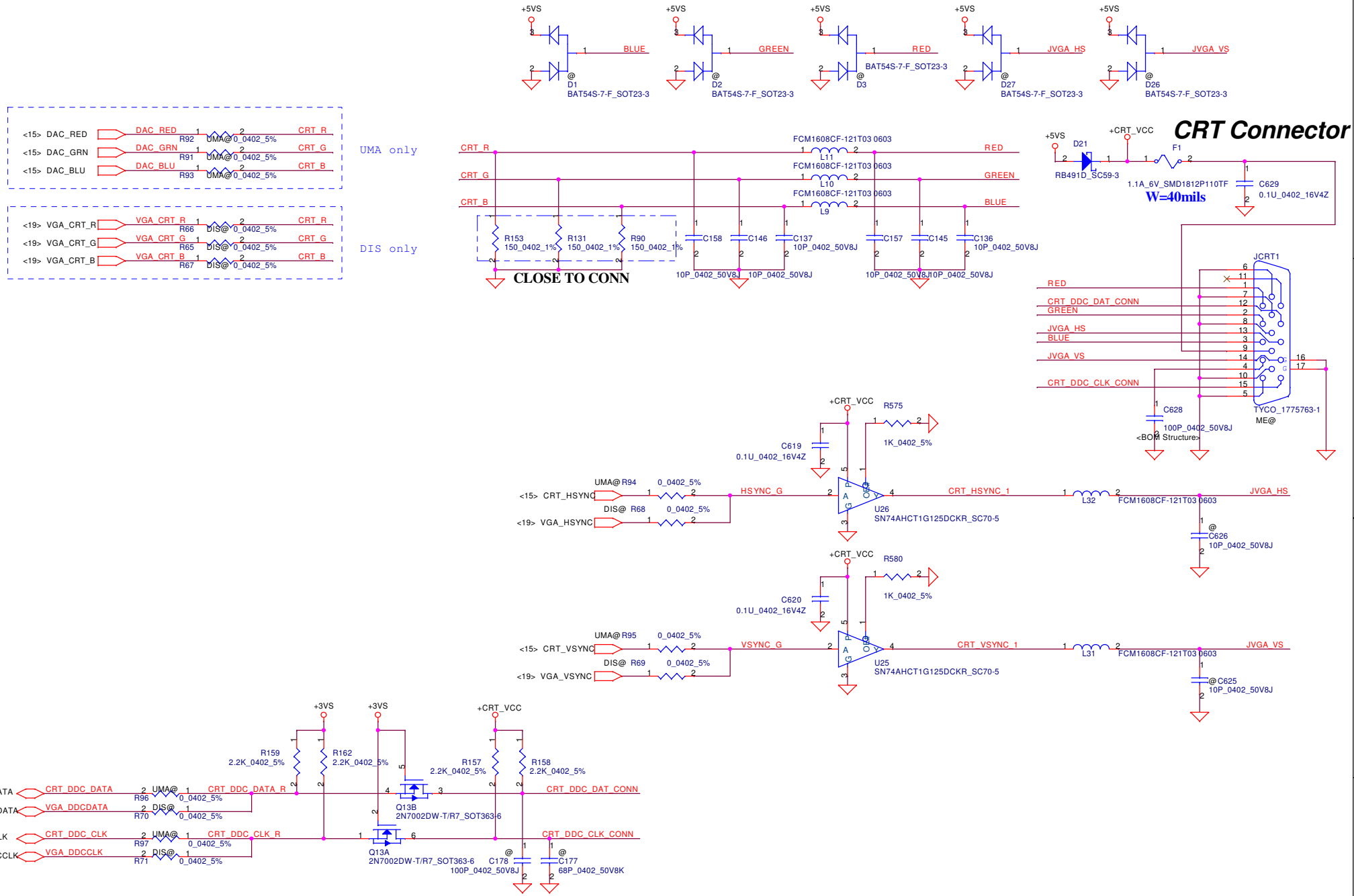
CRT Connector



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.			
Title: CRT Connector			
Size: Custom	Document Number: LA-5752P		Rev: 0.3
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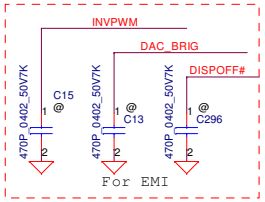
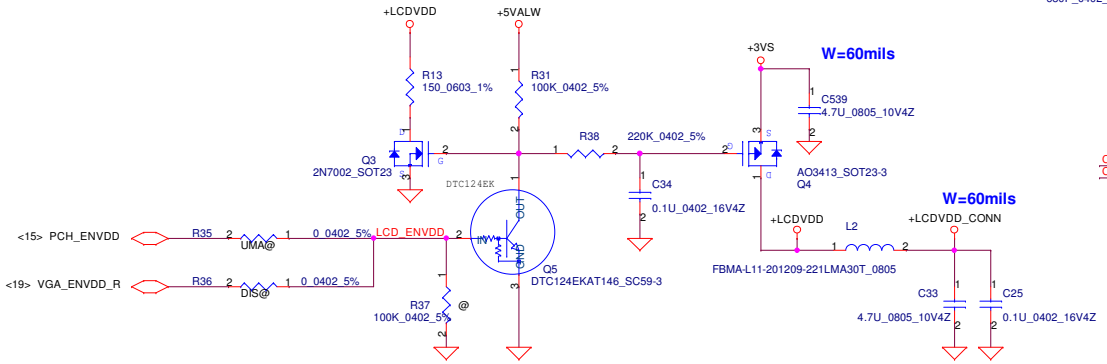
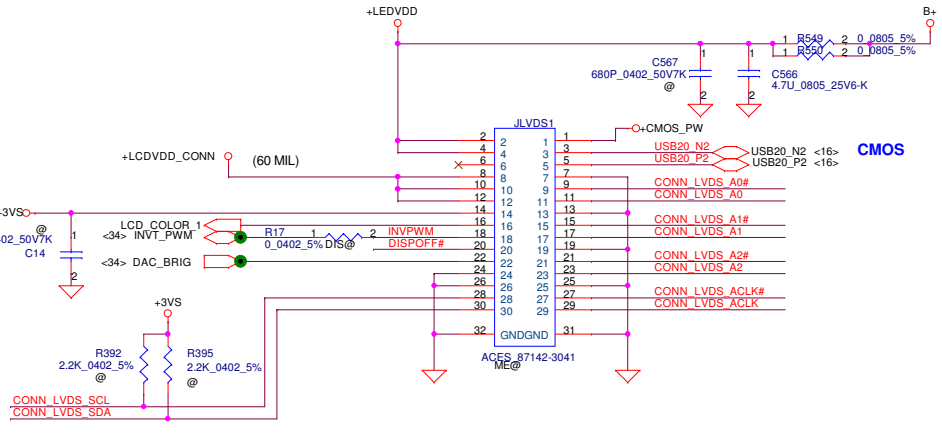
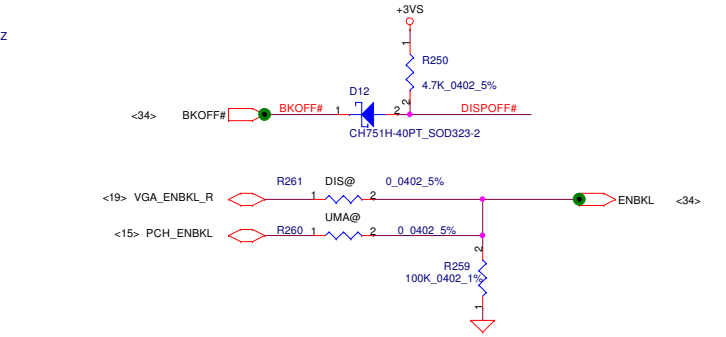
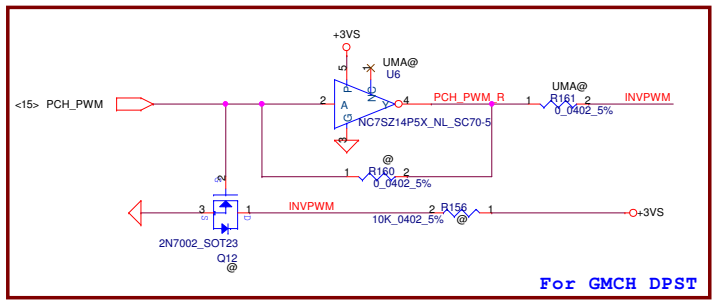


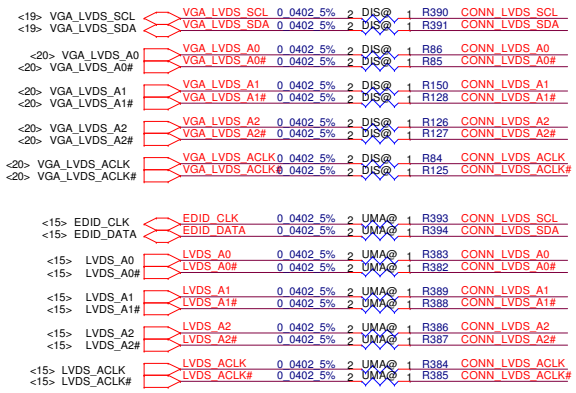
LCD POWER CIRCUIT



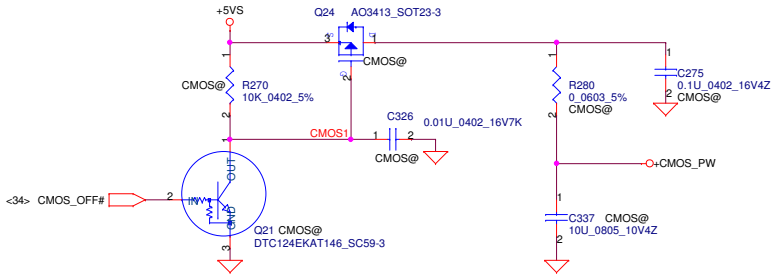








CMOS Camera



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.			
Title: LVDS/CAMERA			
Size: B	Document Number: LA-5752P		Rev: 0.3
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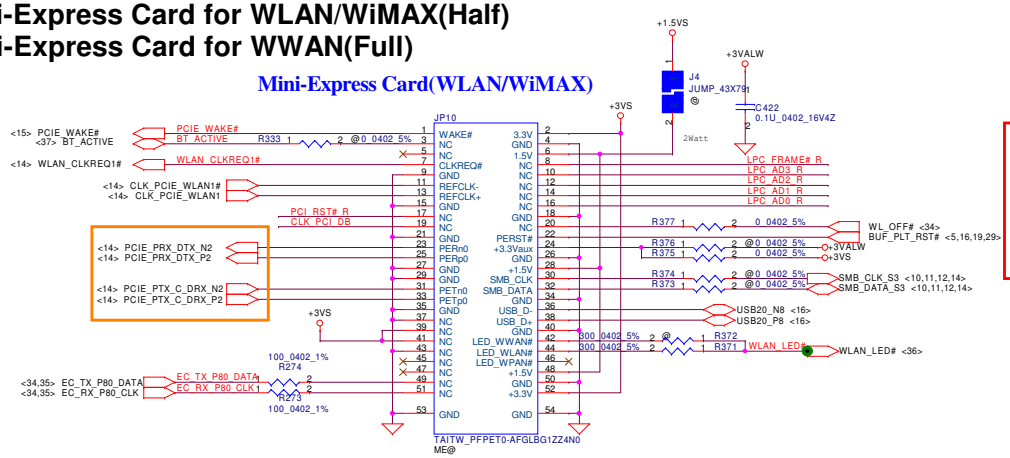
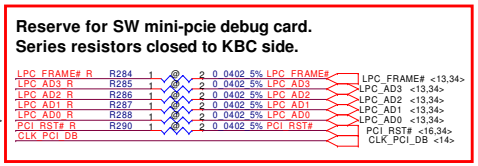
Mini-Express Card for WLAN/WiMAX(Half)
Mini-Express Card for WWAN(Full)

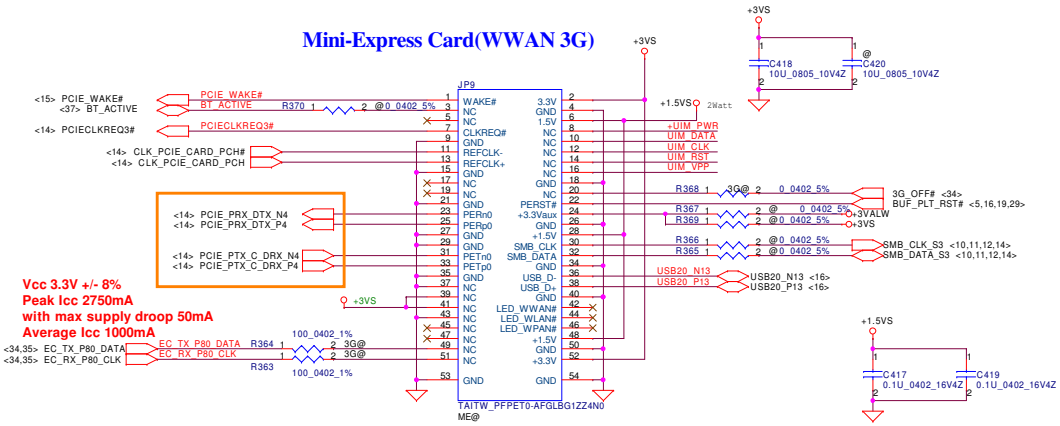
Mini-Express Card(WLAN/WiMAX)

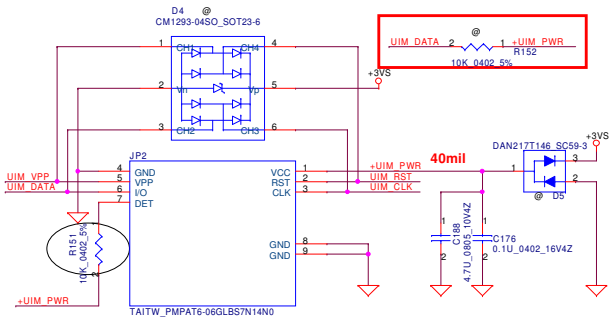


Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

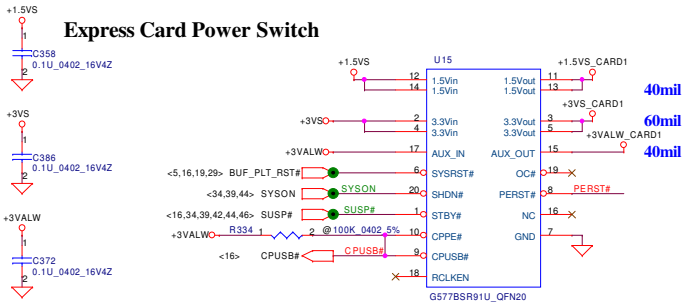


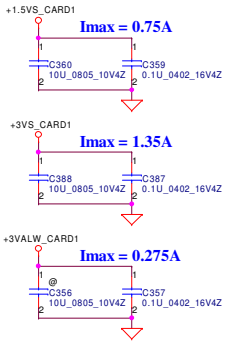
Mini-Express Card(WWAN 3G)



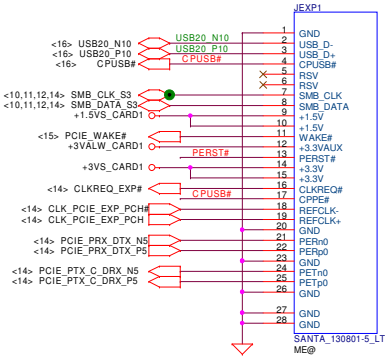


Express Card Power Switch





New Card 34mm Socket (Left/TOP)



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.			
Title	Mini-Card/Nwe Card/SIM		
Size	Document Number		Rev
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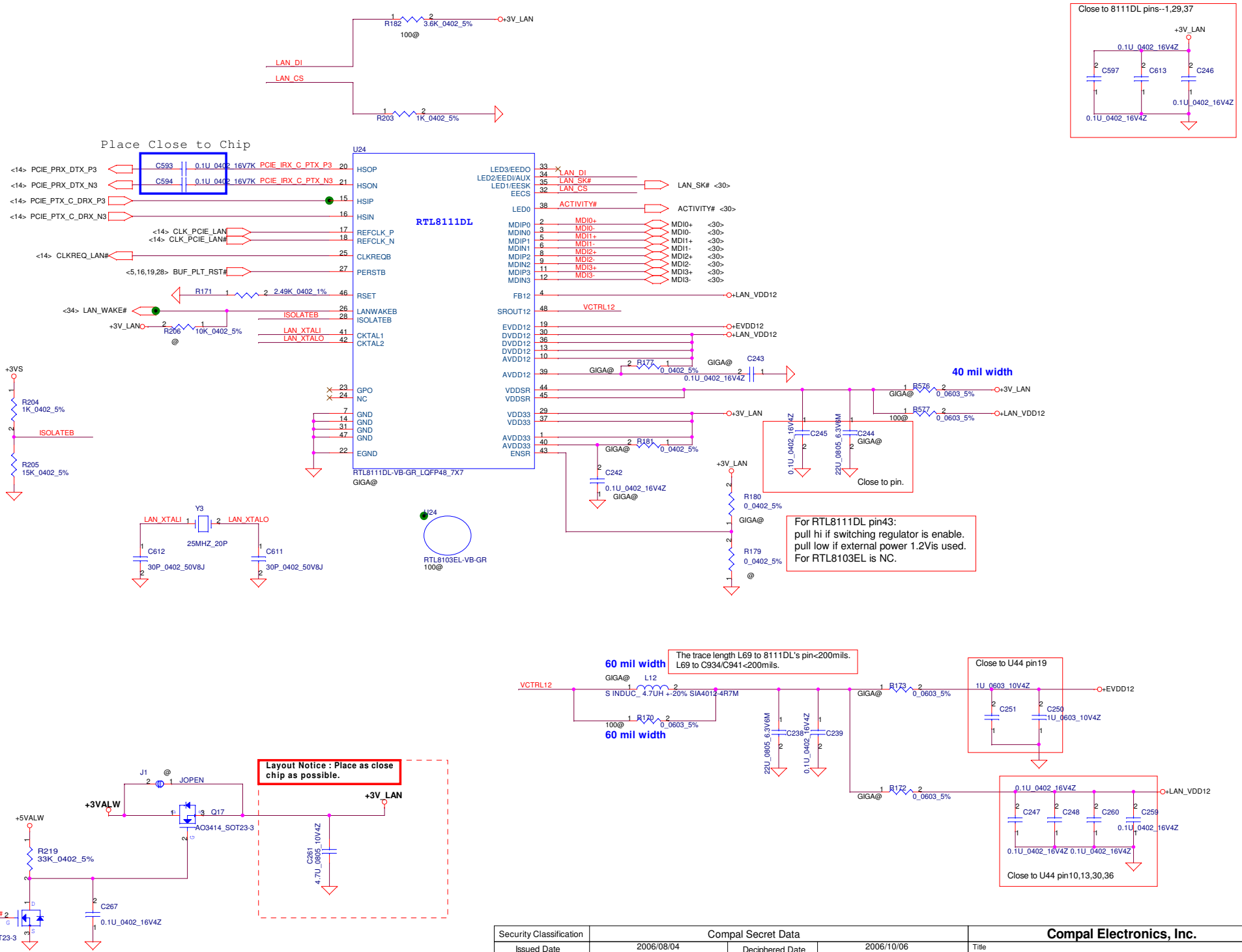
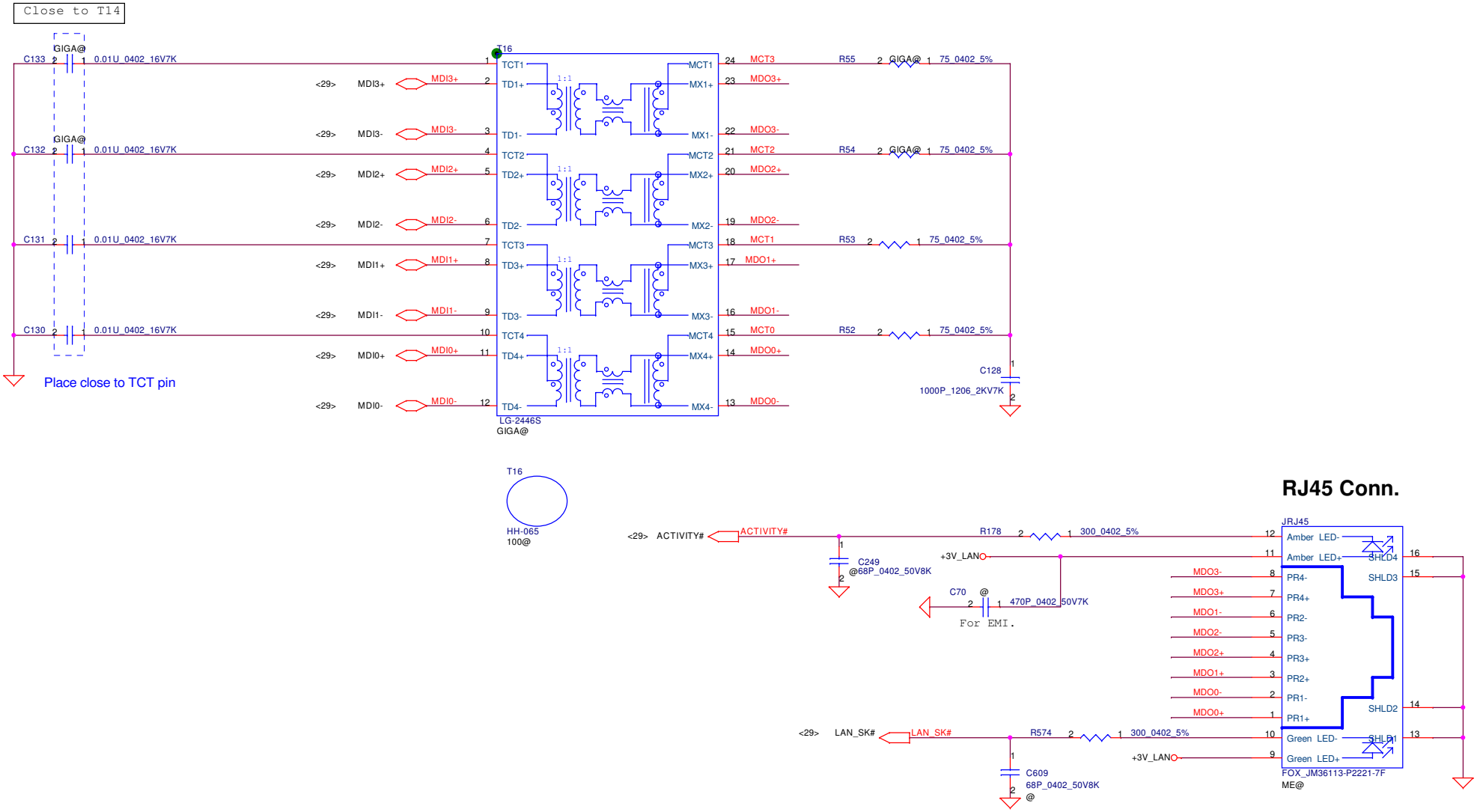


Security Classification	Compal Secret Data		
Issued Date	2006/08/04	Deciphered Date	2006/10/06

Compal Electronics, Inc.

Title	RTL8103EL	
Size: Custom	Document Number: LA-5752P	Rev: 0.3
Date: Thursday, October 29, 2009	Sheet 29 of 51	



Security Classification	Compal Secret Data		
Issued Date	2009/03/20	Deciphered Date	2010/03/20

Compal Electronics, Inc.

Title: **LAN_Transformer**

Size	Document Number	Rev
Custom	LA-5752P	0.3

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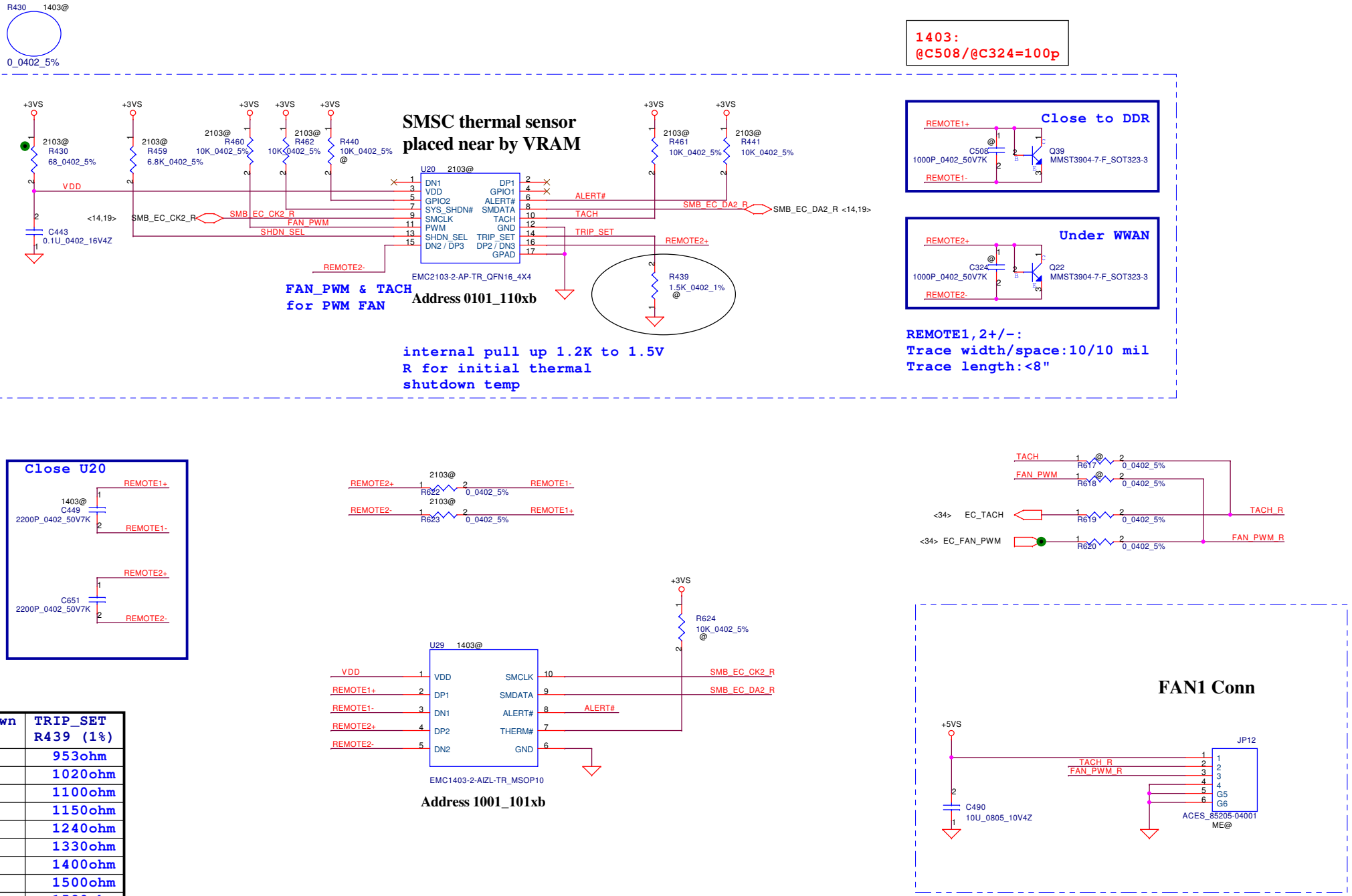

Shutdown Temp	TRIP_SET R439 (1%)
93	953ohm
94	1020ohm
95	1100ohm
96	1150ohm
97	1240ohm
98	1330ohm
99	1400ohm
100	1500ohm
101	1580ohm
102	1690ohm
103	1820ohm
104	1960ohm
105	2050ohm

Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

Compal Electronics,Ltd.

Title: EMC2103/1403_Thermal sensor/FAN

Size: Custom | Document Number: LA-5752P | Rev: 0.3

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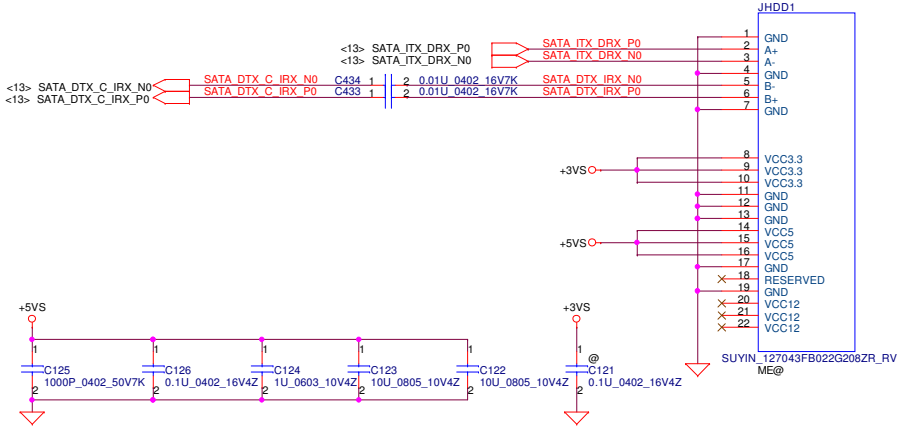
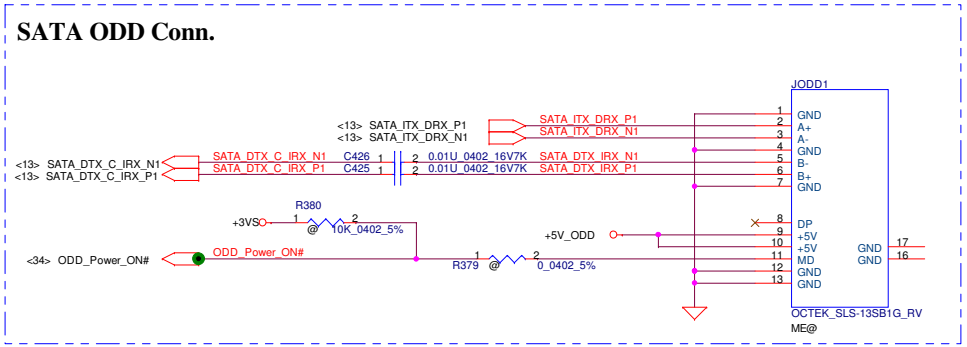
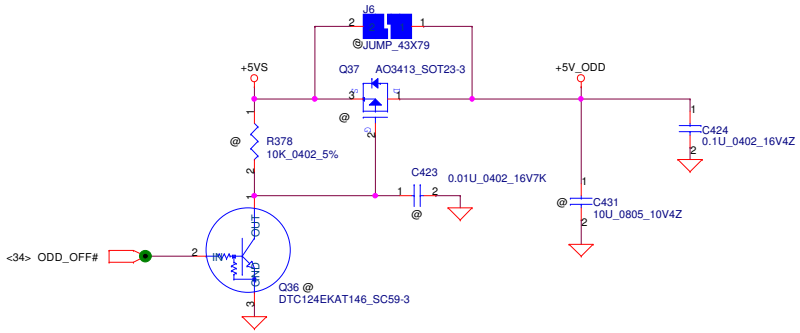
SATA HDD Conn.



SATA ODD Conn.



ODD Power Control



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.			
Title: HDD/ODD Connector			
Size: B	Document Number: LA-5752P		Rev: 0.3
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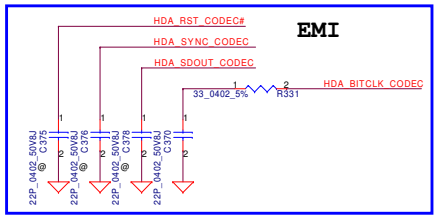
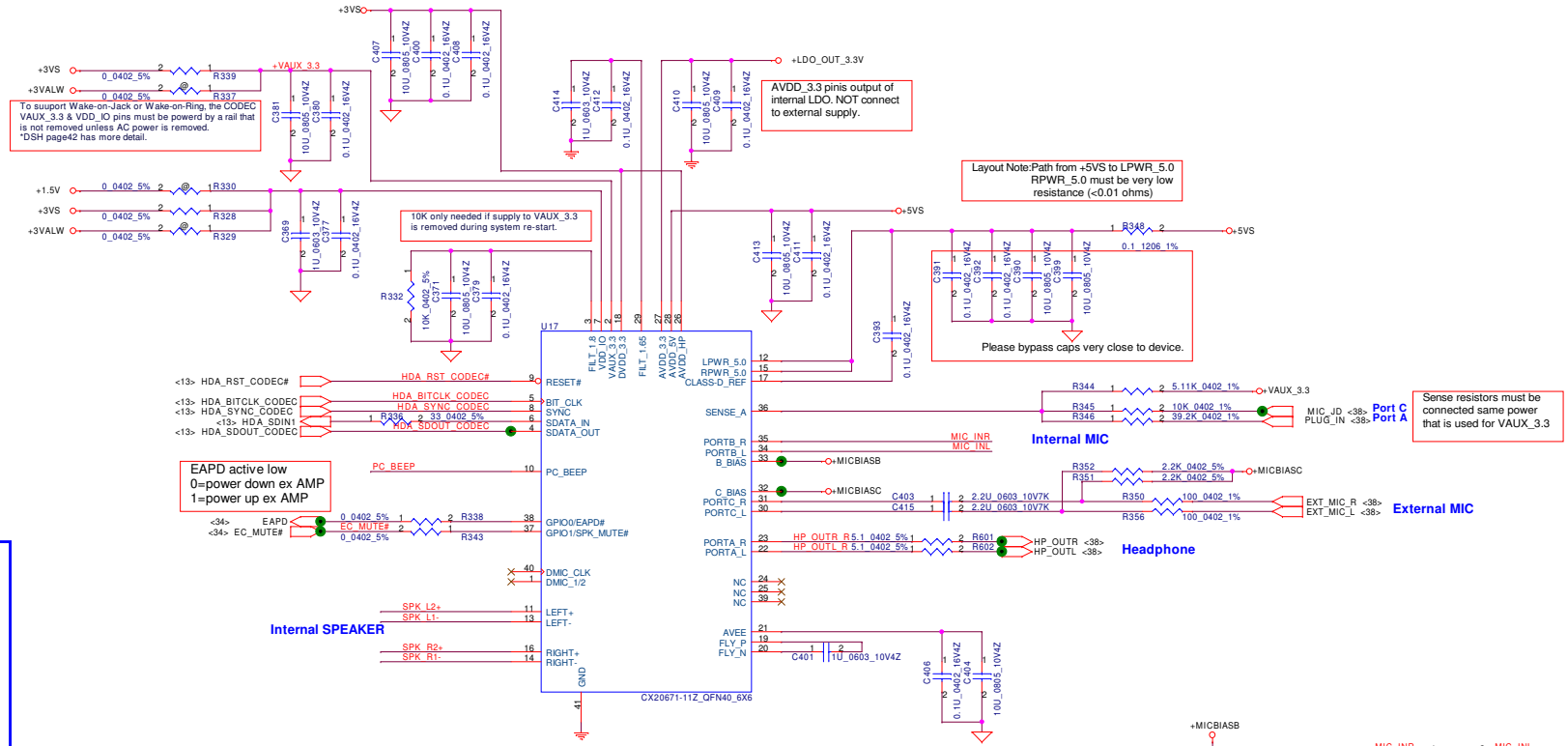
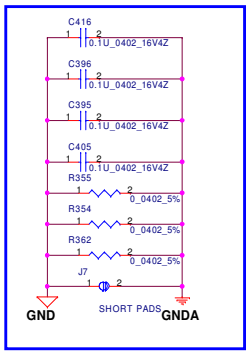
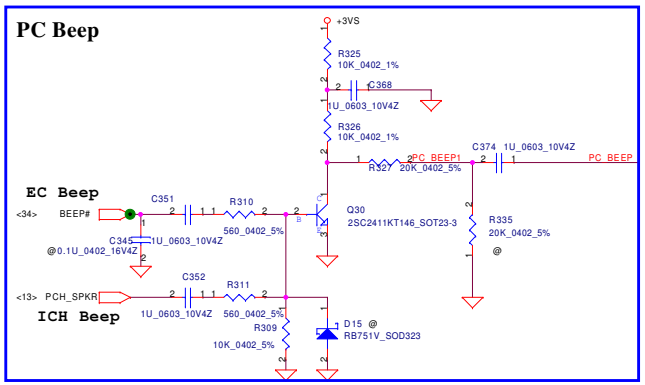
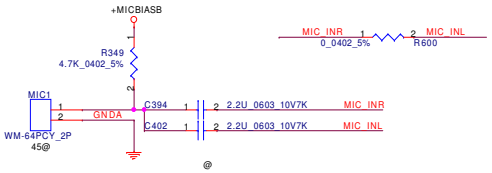
CX20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).



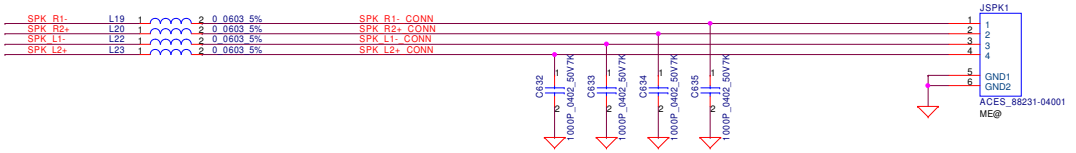








wide 20MIL



Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

Compal Electronics,Ltd.

Title: CX20671 Codec

Size: C | Document Number: LA-5752P | Rev: 0.3

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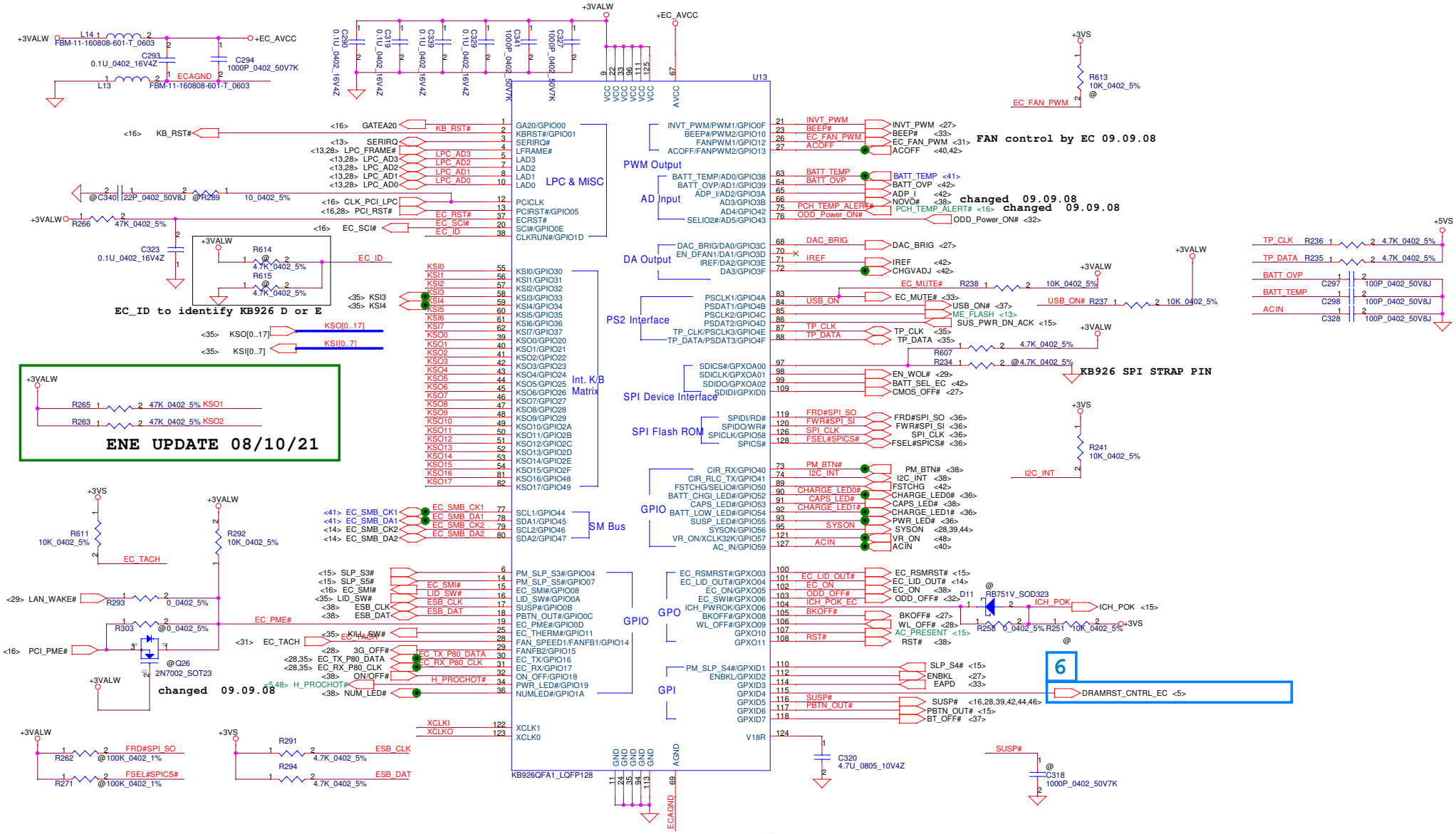

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **BIOS & EC I/O Port**

Size	Document Number	Rev
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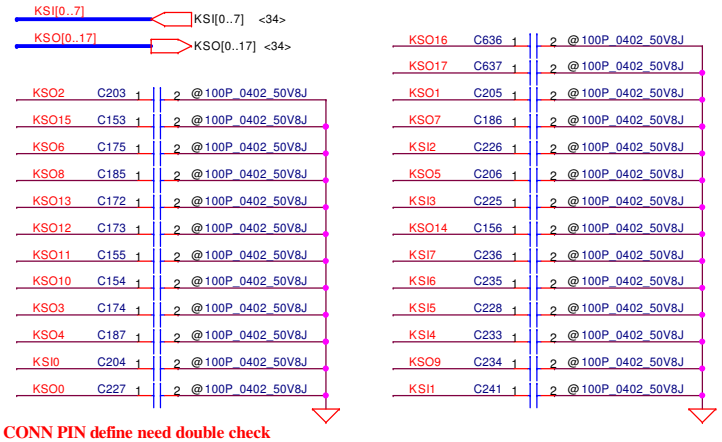
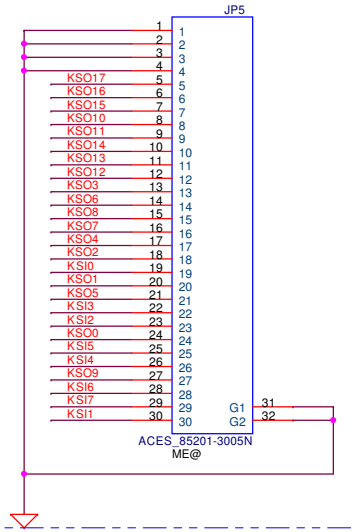
INT_KBD Conn.

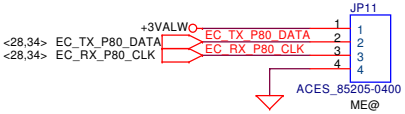


CONN PIN define need double check

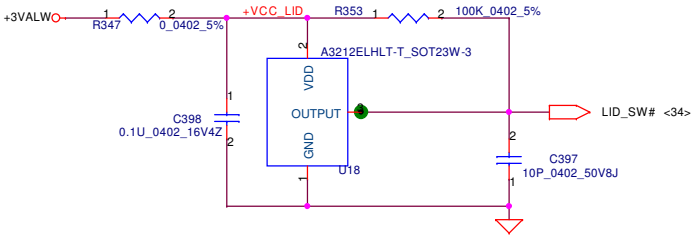
reversal of NIWE1



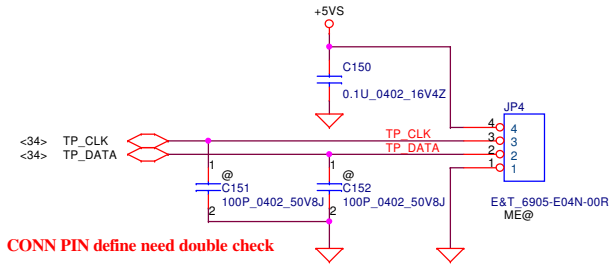
EC DEBUG PORT



Lid Switch

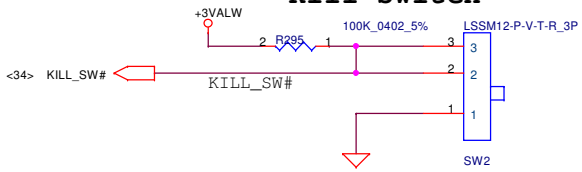


To TP/B Conn.



CONN PIN define need double check

Kill Switch



Kill

STATUS	
1,2(LOW)	OFF
2,3(HI)	ON

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.			
Title: KB /SW /LPC Debug Conn.			
Size: B	Document Number: LA-5752P		Rev: 0.3
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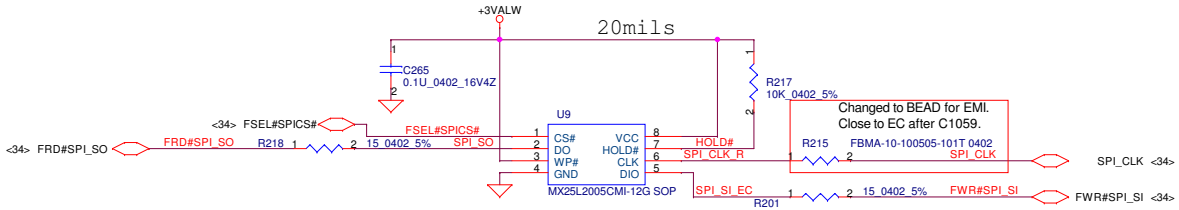
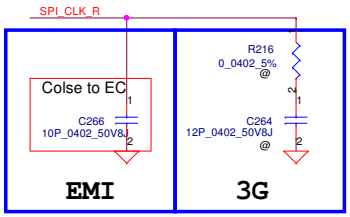
FOR EC 256KB SPI ROM
(150mil PACKAGE)
P/N : SA00003GK00

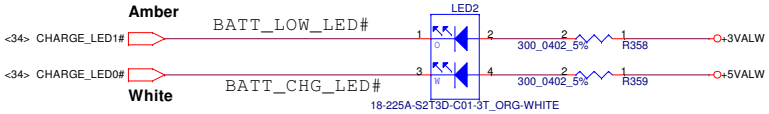




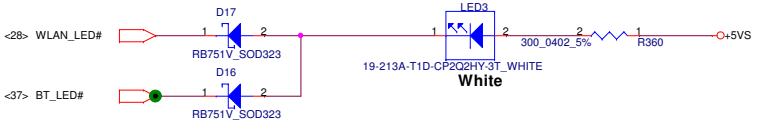
LED

SC500005B00

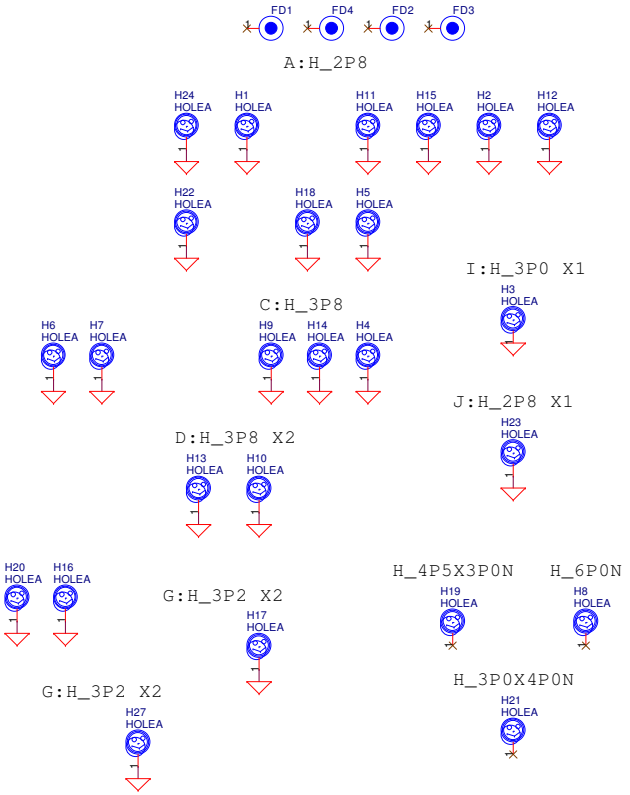
SC500006M00



SC500005B00



SC500005B00



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: LED/EC SPI ROM

Size	Document Number	Rev
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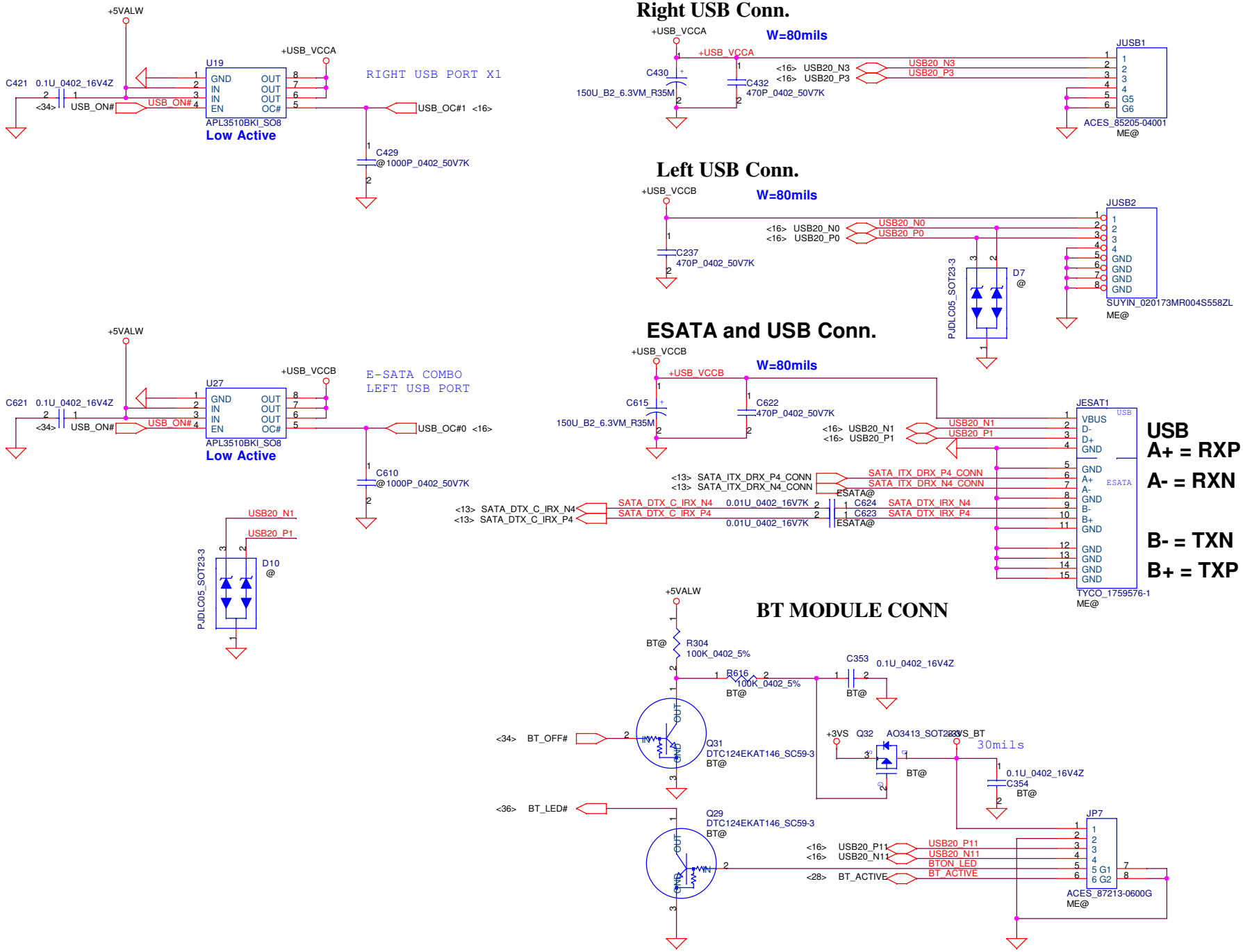

Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title: USB ports/BT/E-SATA

Size	Document Number	Rev
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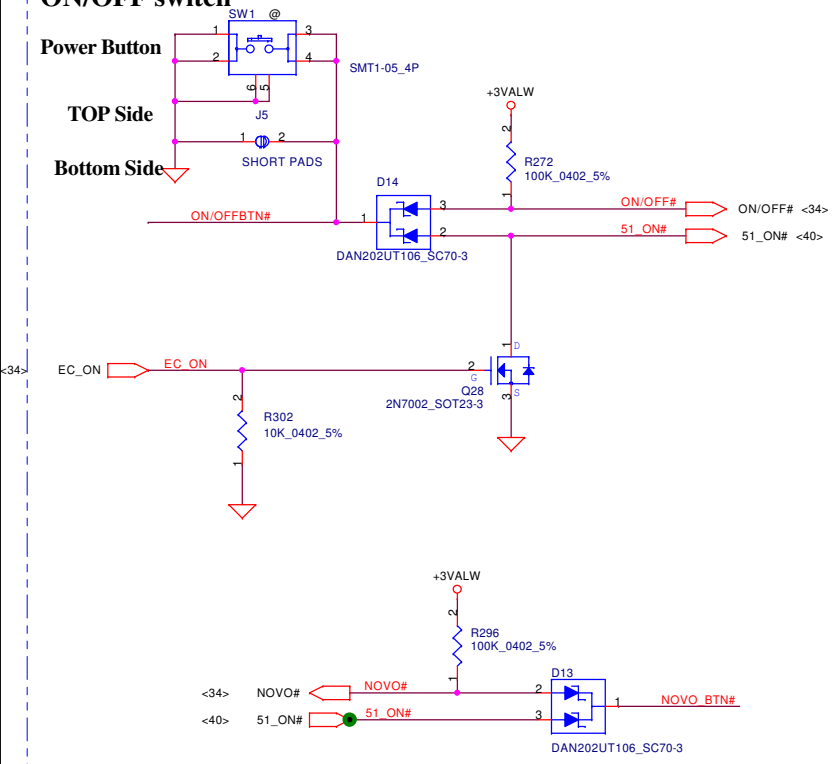
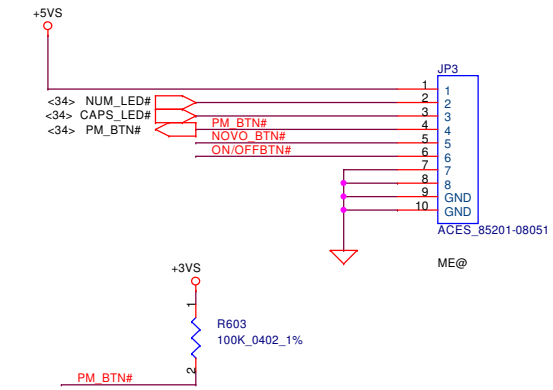
ON/OFF switch

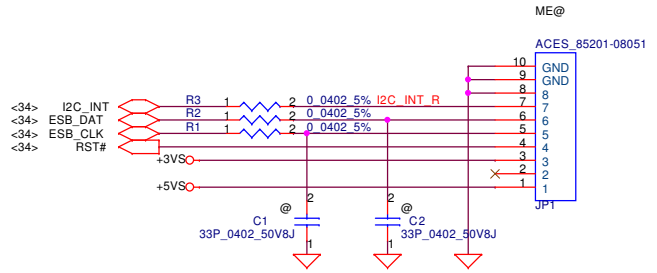


Power Bottom Board Conn. 8pin

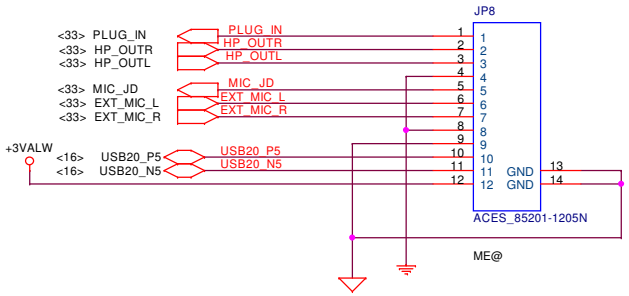


EMI REQUEST 1ST = SCA00000E00
2ST = SCA00000R00

Cap Sensor Board Conn. 6pin
ENE SB3534



Card Reader/Audio Jack SB CONN



Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

Compal Electronics,Ltd.

Title: **Audio Jack & SW connector**

Size	Document Number	Rev
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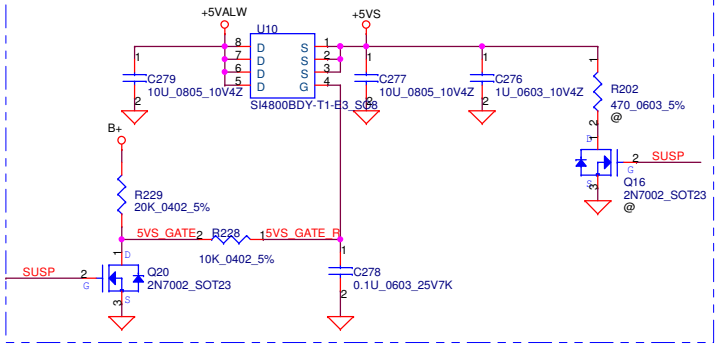
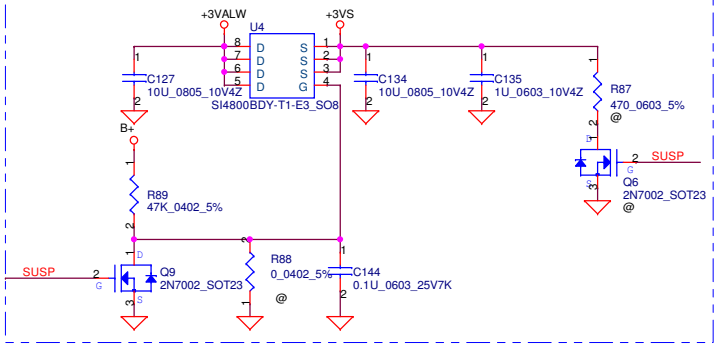
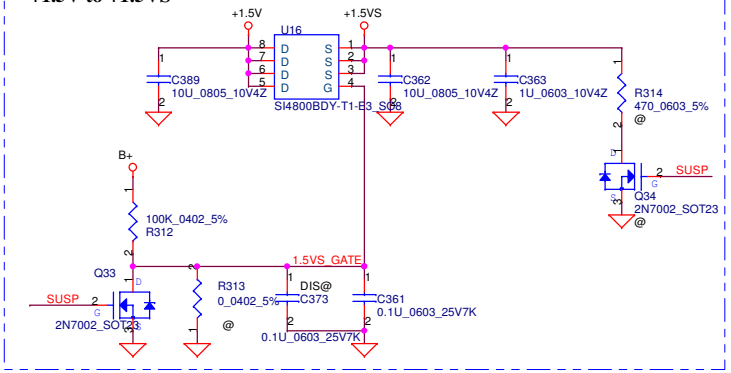
+5VALW TO +5VS

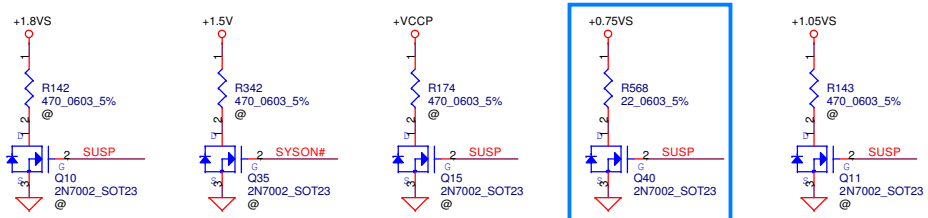


+3VALW TO +3VS

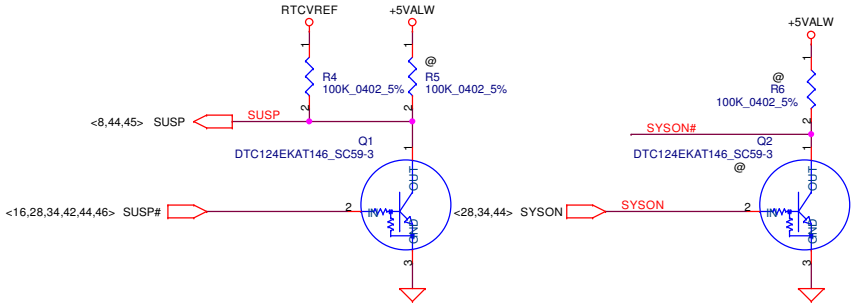


+1.5V to +1.5VS





For Intel S3 Power Reduction.



Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
Custom	LA-5752P	0.3

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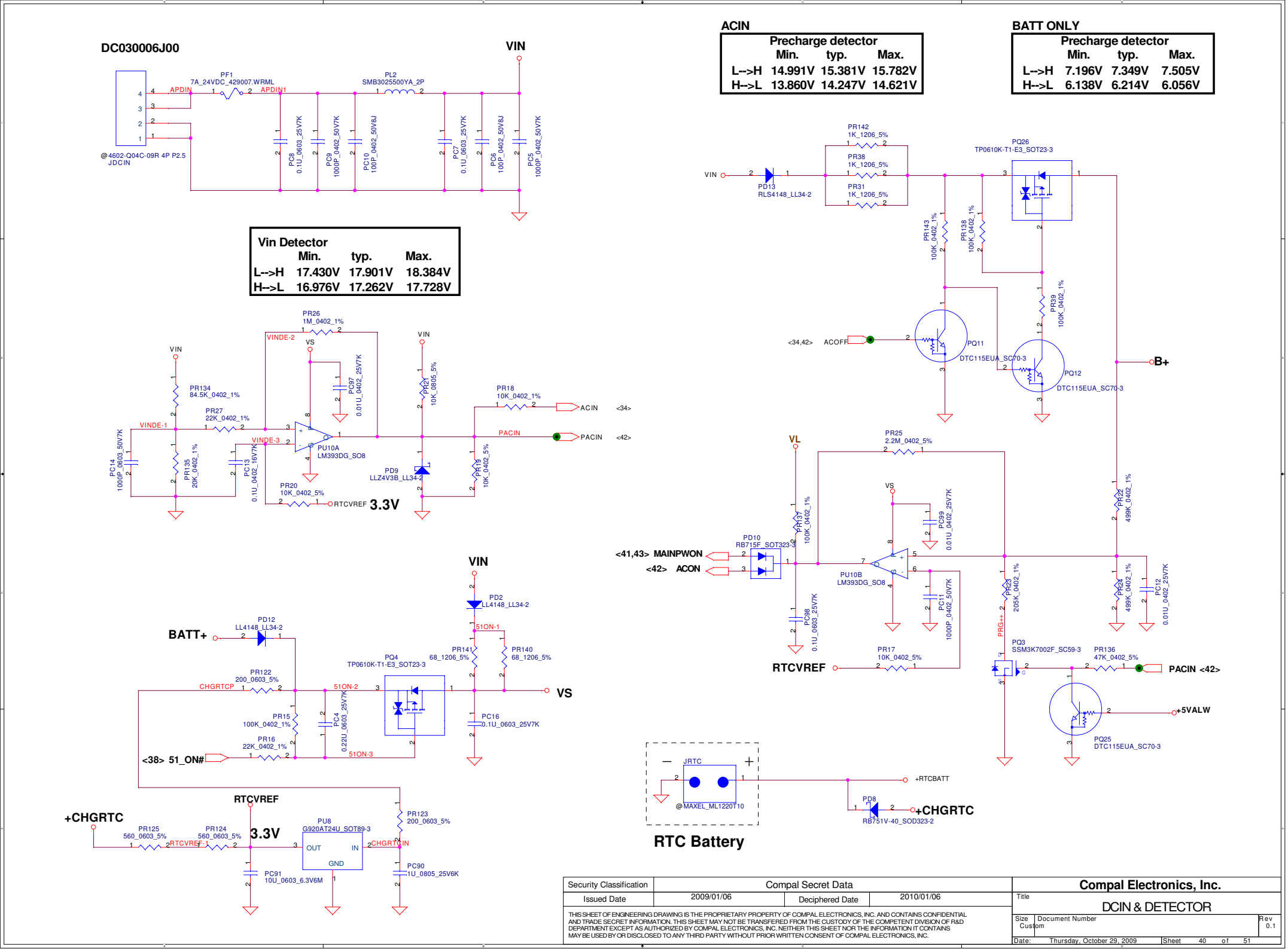

Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/01/06

Compal Electronics, Inc.

Title: DCIN & DETECTOR

Size	Document Number	Rev
Custom		0.1

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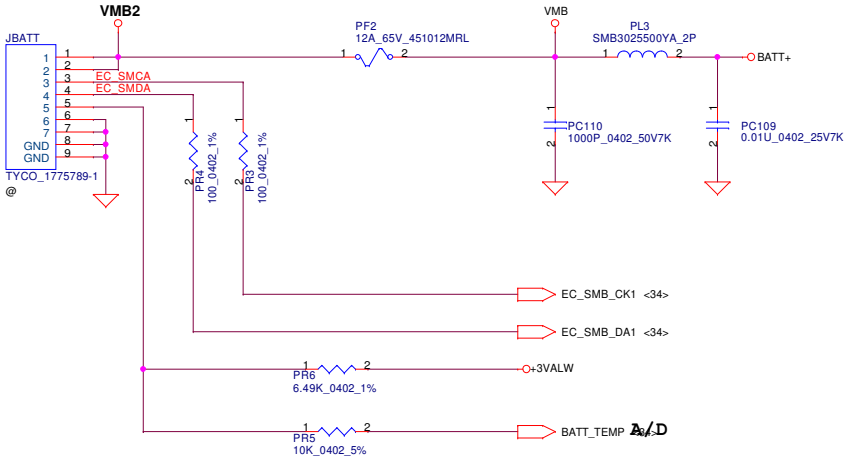
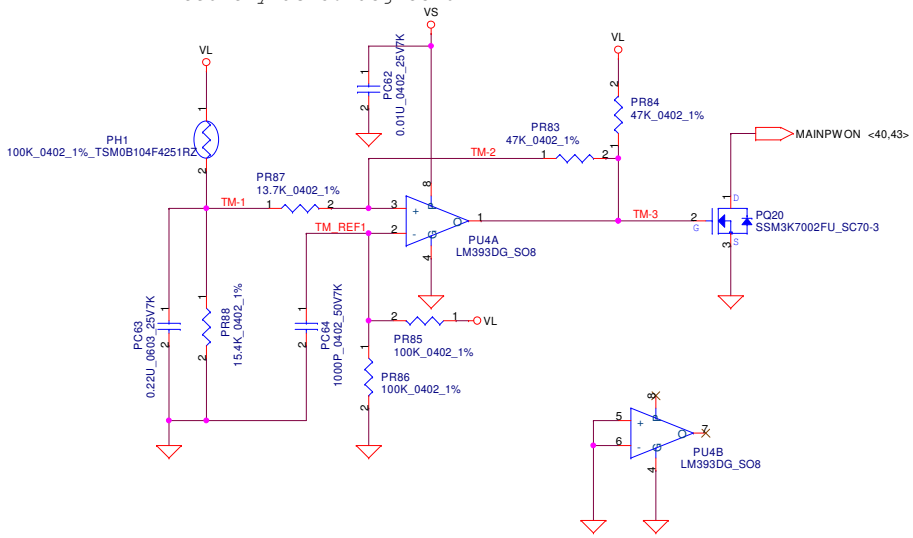
PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C





Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/01/06

Compal Electronics, Inc.

Title: BATTERY CONN / OTP

Size | Document Number | Rev 0.1

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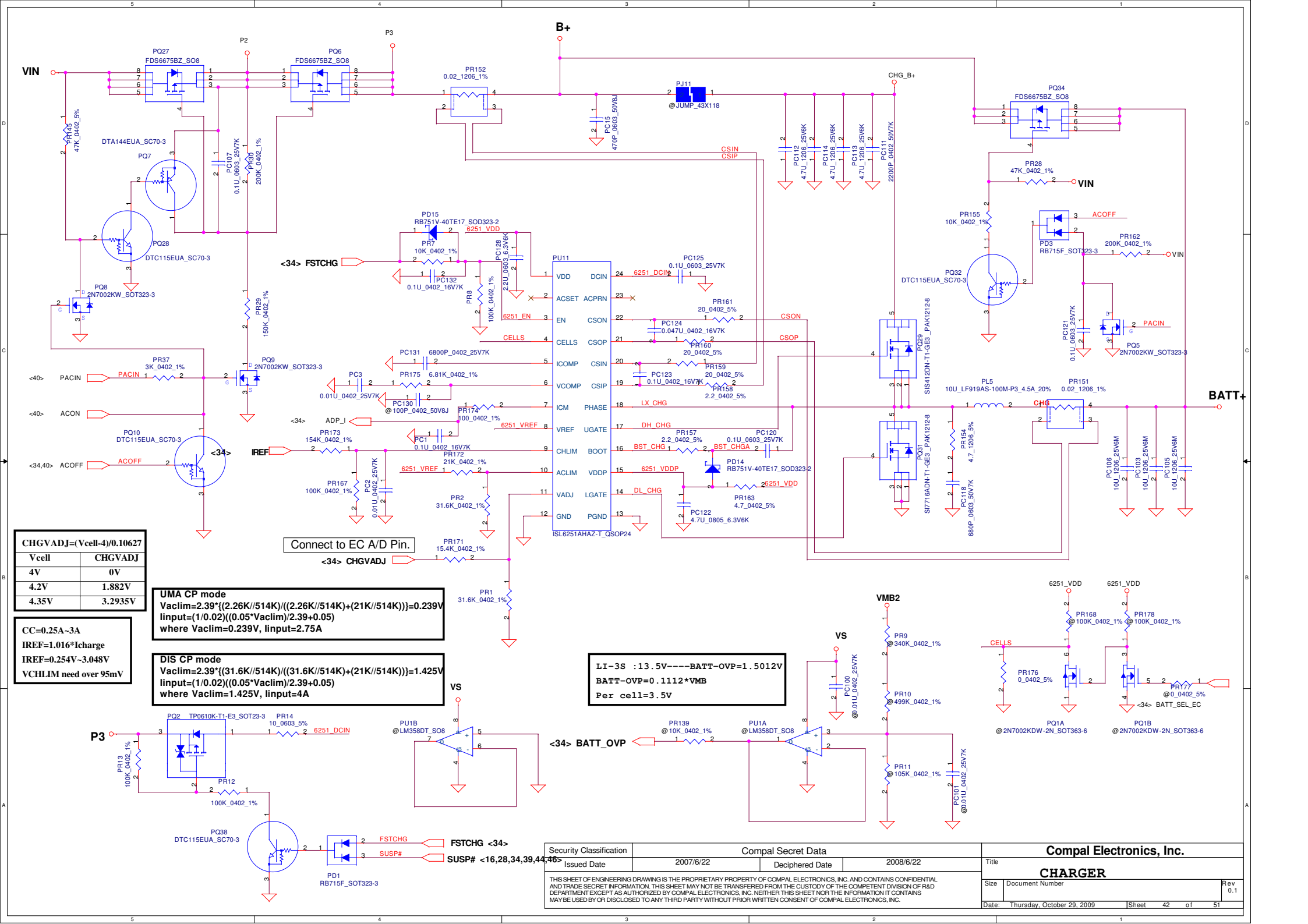

Security Classification	Compal Secret Data		
Issued Date	2007/6/22	Deciphered Date	2008/6/22

Compal Electronics, Inc.

Title: **CHARGER**

Size	Document Number	Rev
		0.1

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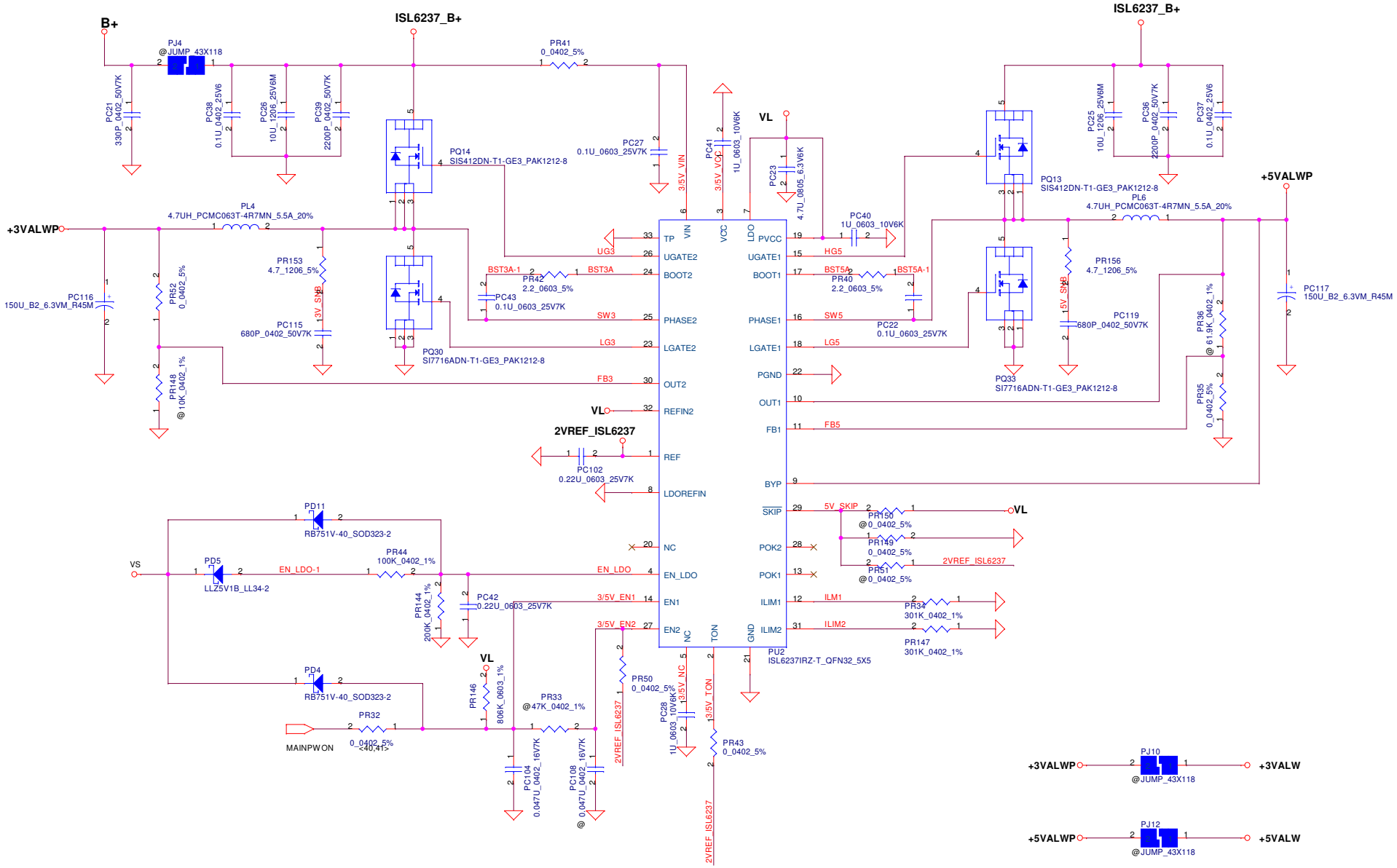

Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/01/06

Compal Electronics, Inc.

Title: **3VALW/5VALW**

Size	Document Number	Rev
Custom		0.1

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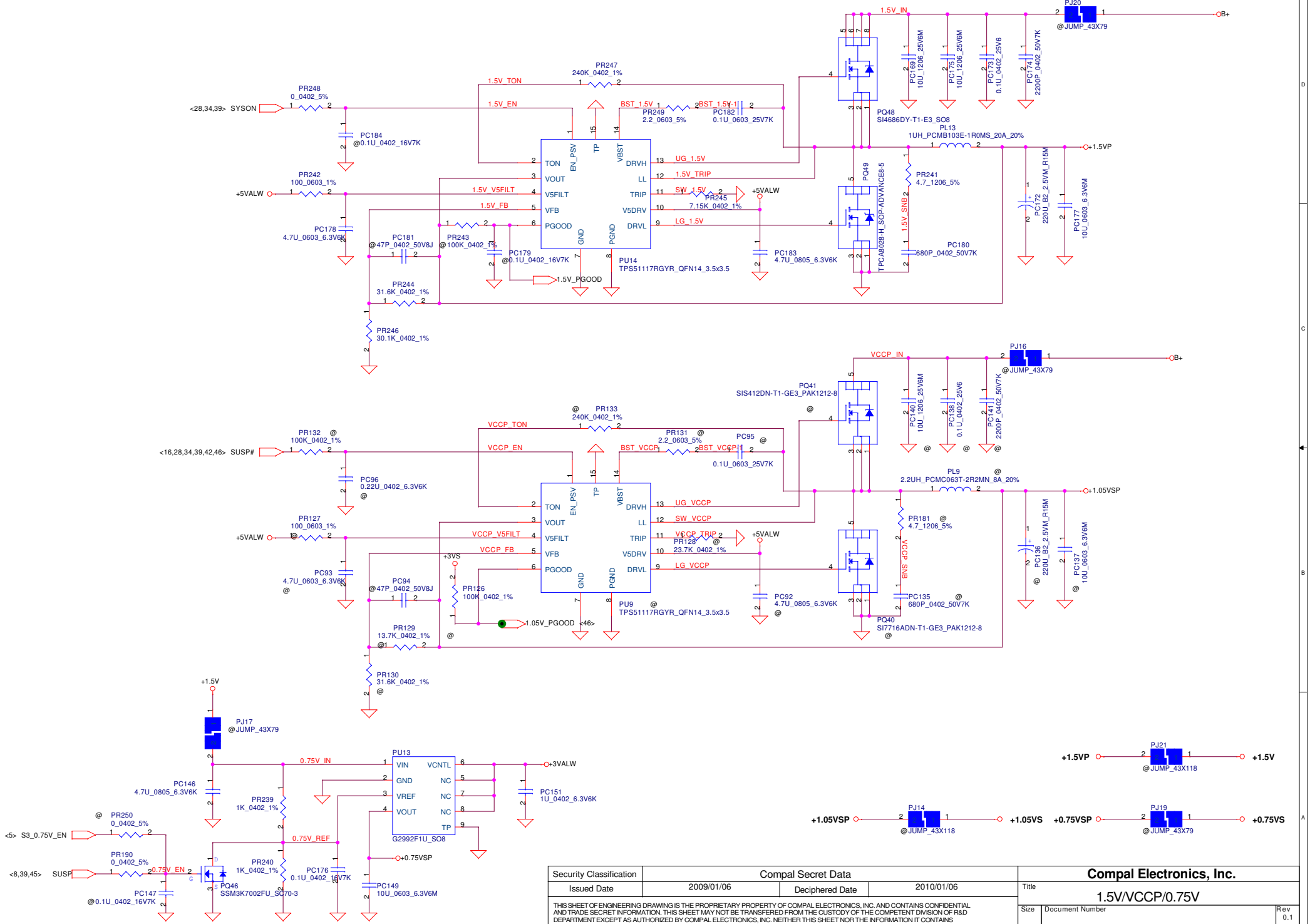

Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/01/06

Compal Electronics, Inc.

Title: 1.5V/VCCP/0.75V

Size	Document Number	Rev
		0.1

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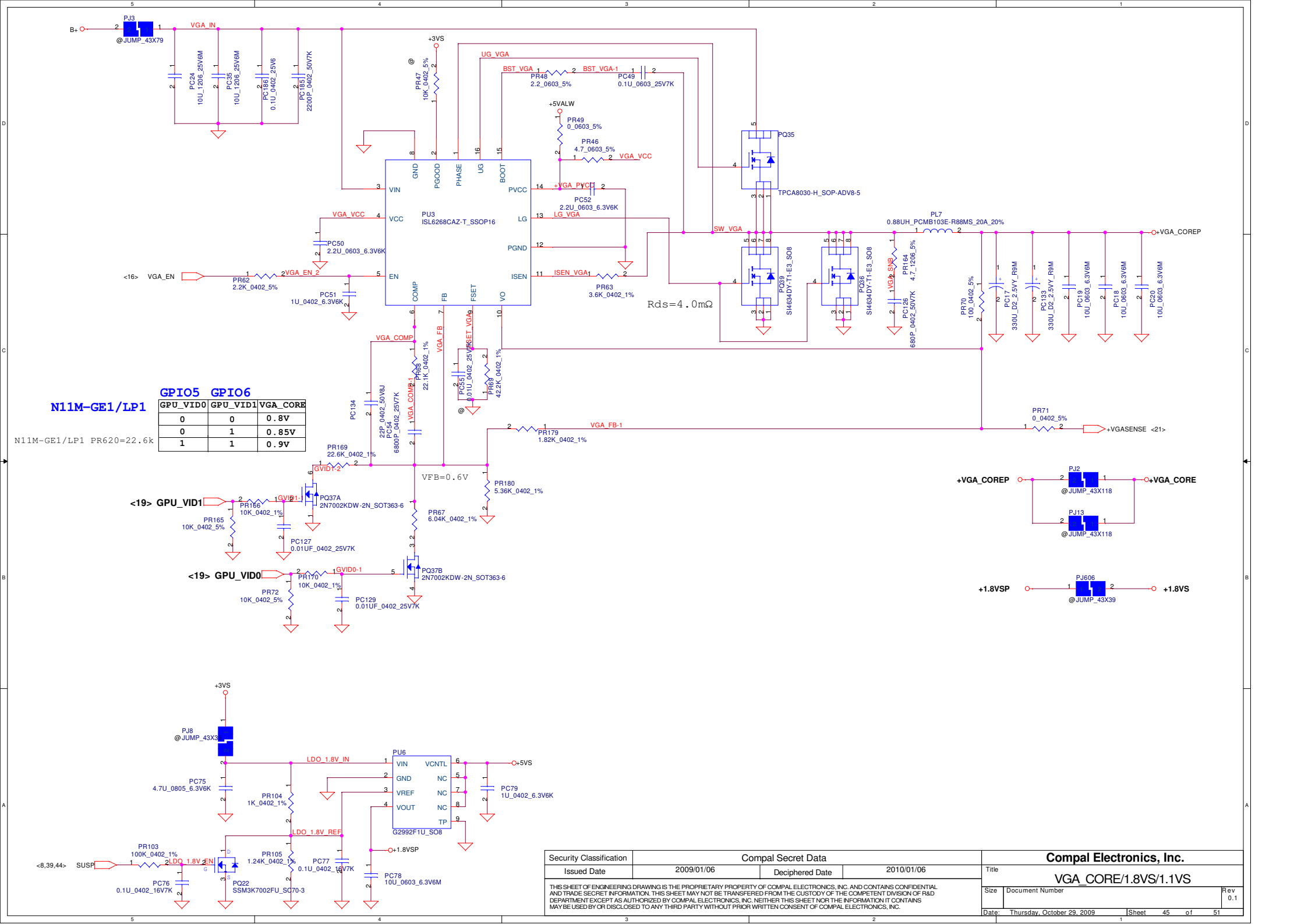


N11M-GE1/LP1

N11M-GE1/LP1 PR620=22.6k

GPIO5	GPIO6	
GPU_VID0	GPU_VID1	VGA_CORE
0	0	0.8V
0	1	0.85V
1	1	0.9V

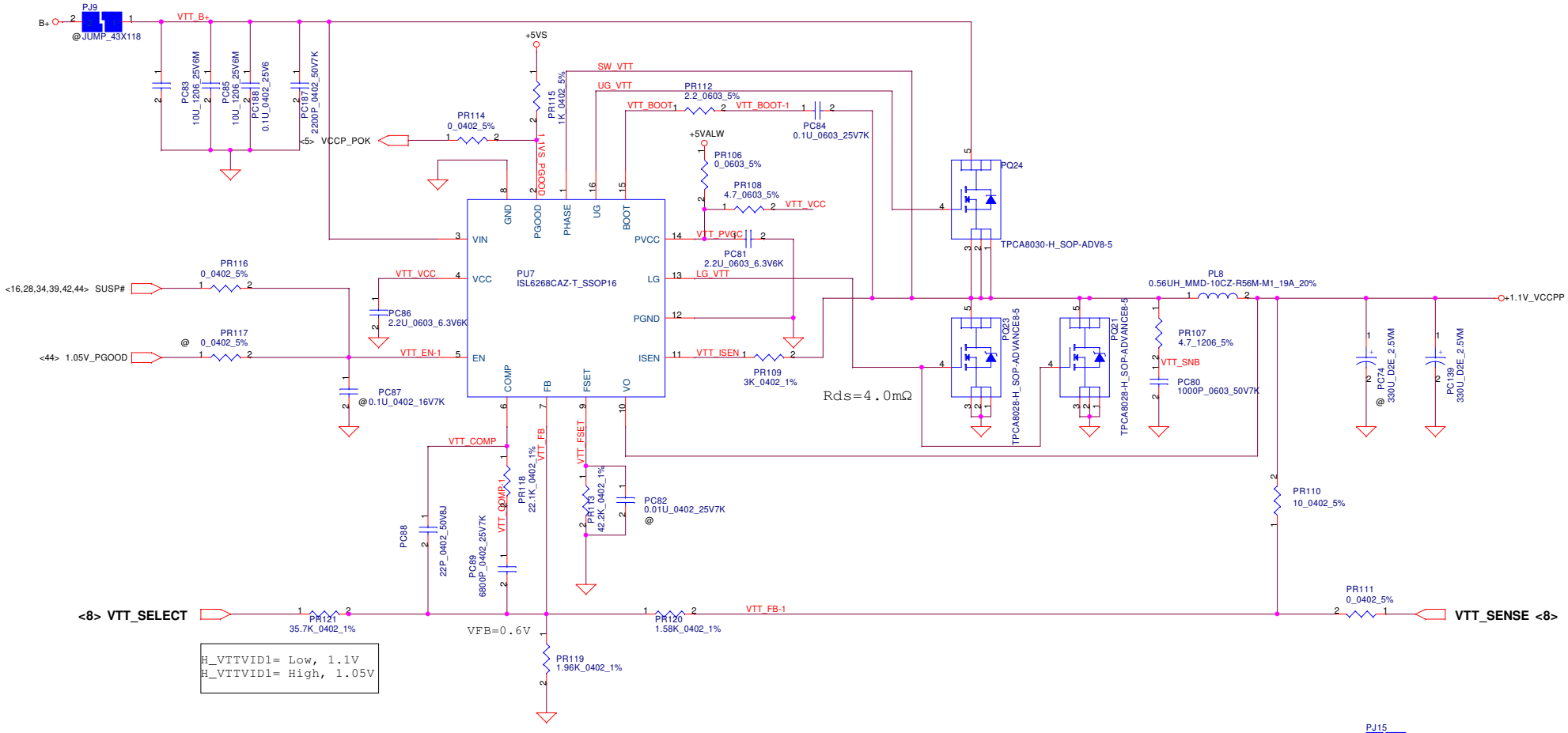
Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/01/06

Compal Electronics, Inc.

Title: VGA_CORE/1.8VS/1.1VS

Size	Document Number	Rev
		0.1

Date: Thursday, October 29, 2009 | Sheet 45 of 51



Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/01/06

Compal Electronics, Inc.

Title: +1.1VS_VTT

Size	Document Number	Rev
Custom		0.1

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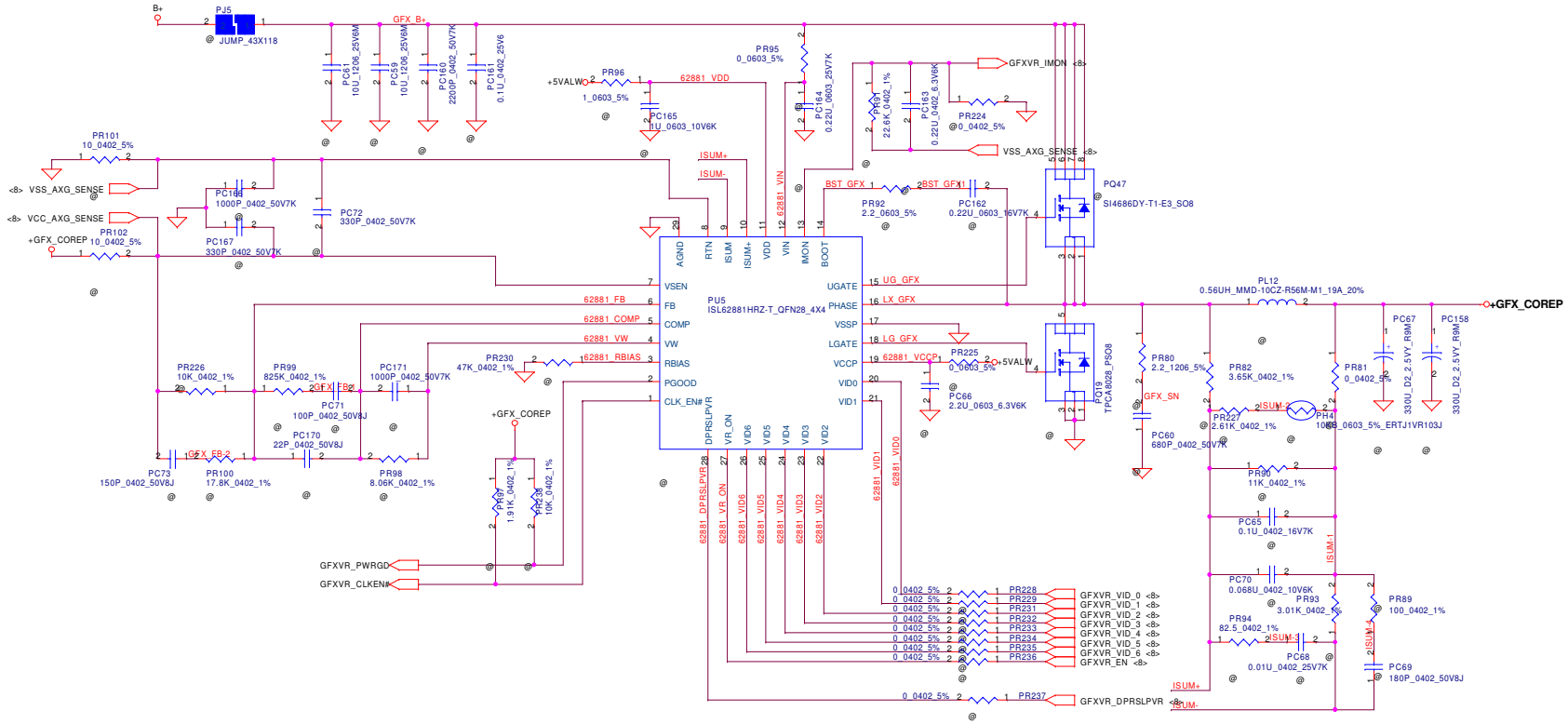

(15A,600mils ,Via NO.= 30)

Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/01/06

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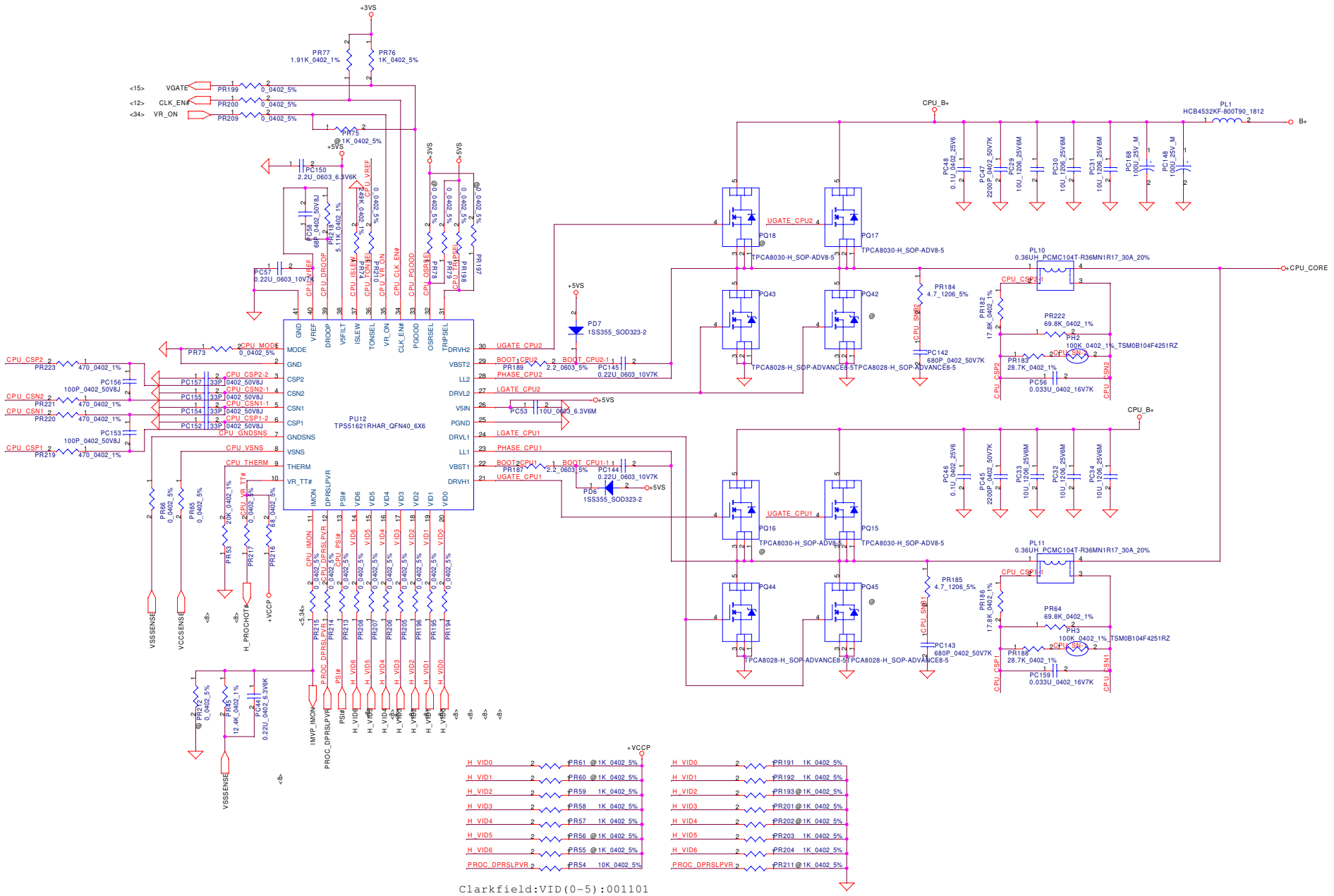
Compal Electronics, Inc.

Title: **GFX_CORE**

Size	Document Number	Rev
		0.1

Date: Thursday, October 29, 2009 | Sheet 47 of 51



Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/01/06

Compal Electronics, Inc.			
Title	CPU_CORE		
Size	Document Number		Rev 0.1
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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17				20081022	

Compal Electronics, Inc.

Title: PIR (PWR)

Size: Custom | Document Number: <Doc> | Rev: 0.1

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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
				EVT TO DVT

Compal Electronics, Inc.

Title: **HW PIR**

Size	Document Number	Rev
B	LA-5752P	0.3

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Compal Electronics, Inc.	
Title	HW PIR
Size: B	Document Number: LA-5751
Rev: 0.3	
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