

IGT30

Compal **Schematics Document** *Confidential*

Mobile Merom uFCPGA with Intel
Crestline_GM/PM+ICH8-M core logic

Monday, December 25, 2006

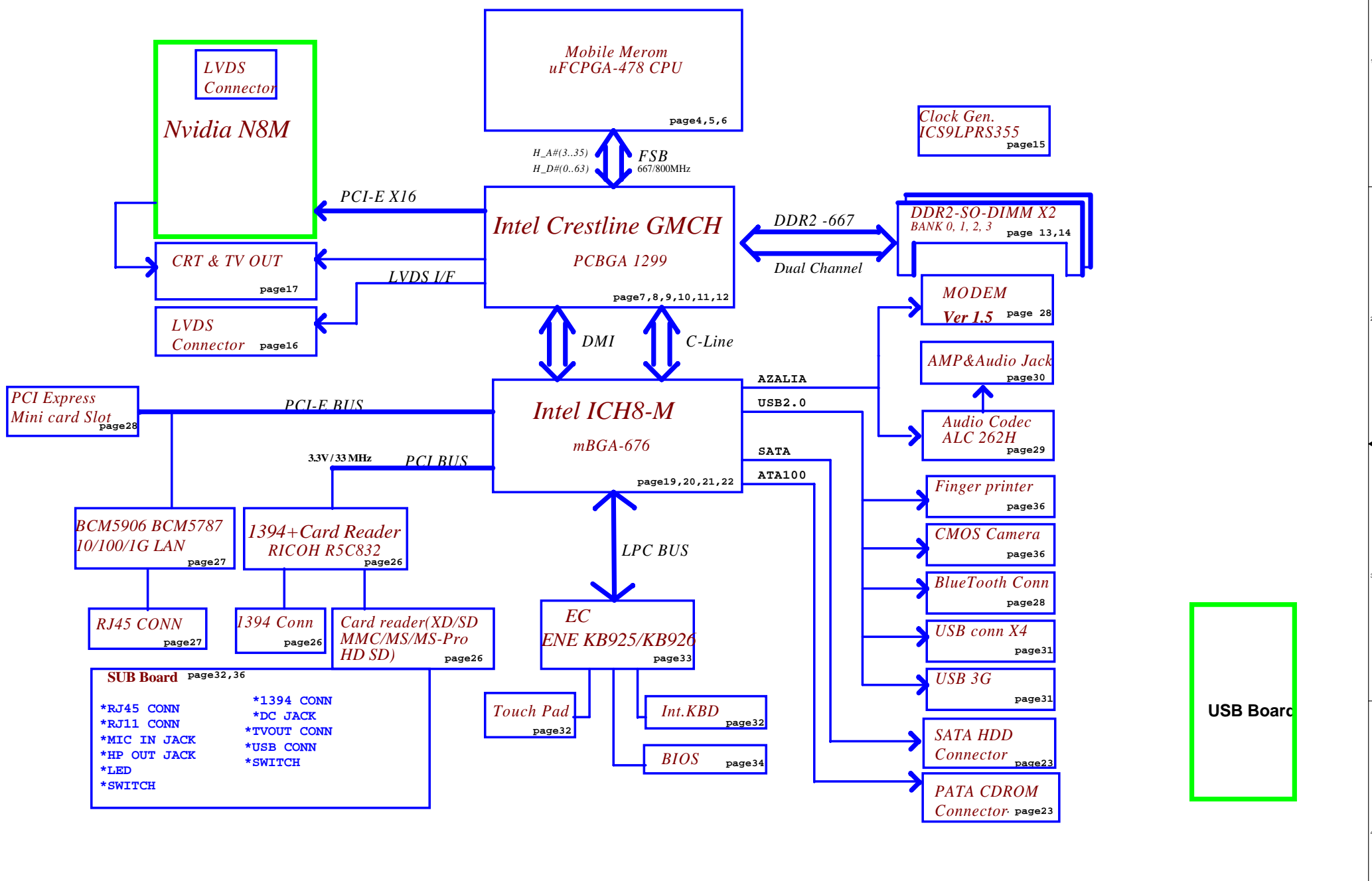
REV:0.1

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LEFT SWITCH Board

LEDs Board



TP Board

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Block Diagram			

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Voltage Rails O MEANS ON X MEANS OFF

power plane / State	+B LDO3 LDO5	+5VALW +3VALW	+1.8V +5V +0.9V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.25VS +VGA_CORE +CPU_CORE +VCCP	CLOCK
S0	O	O	O	O	O
S3	O	O	O	X	O
S5 S4/AC	O	O	X	X	O
S5 S4/ Battery only	O	X	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X	X

O MEANS ON S3 : STR
X MEANS OFF S4 : STD
 S5 : SOFT OFF

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
1394	AD22	0	PIRQG/H

EC SM Bus1 address

EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 100X b
EEPROM(24C16/02)	1010 000X b		

ICH8 SM Bus address

Device	Address
Clock Generator (ICS954226)	1101 001Xb
DDRII DIMM0	1010 000Xb
DDRII DIMM1	1010 010Xb

SKU ID Table

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
* 0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOM Structure

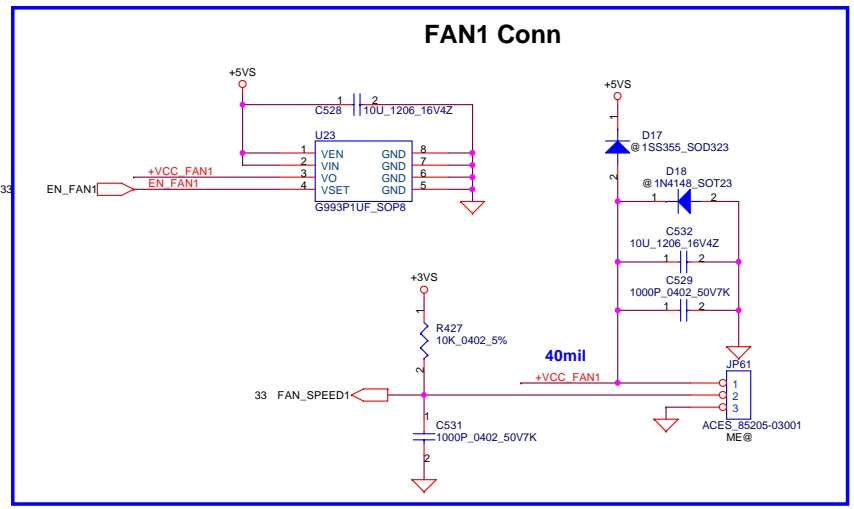
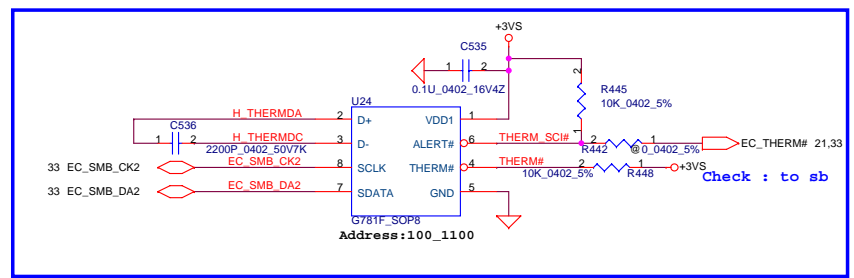
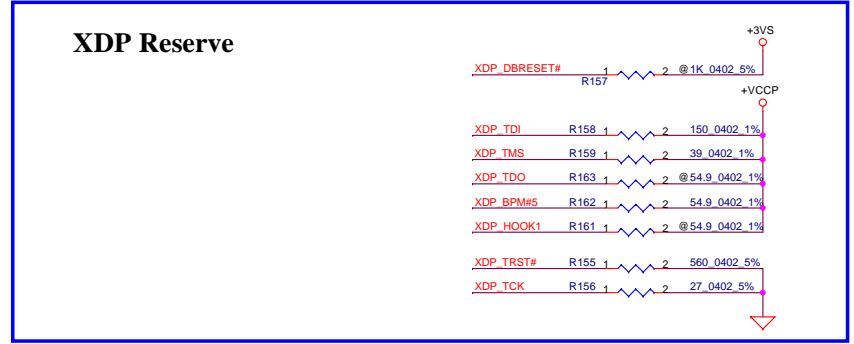
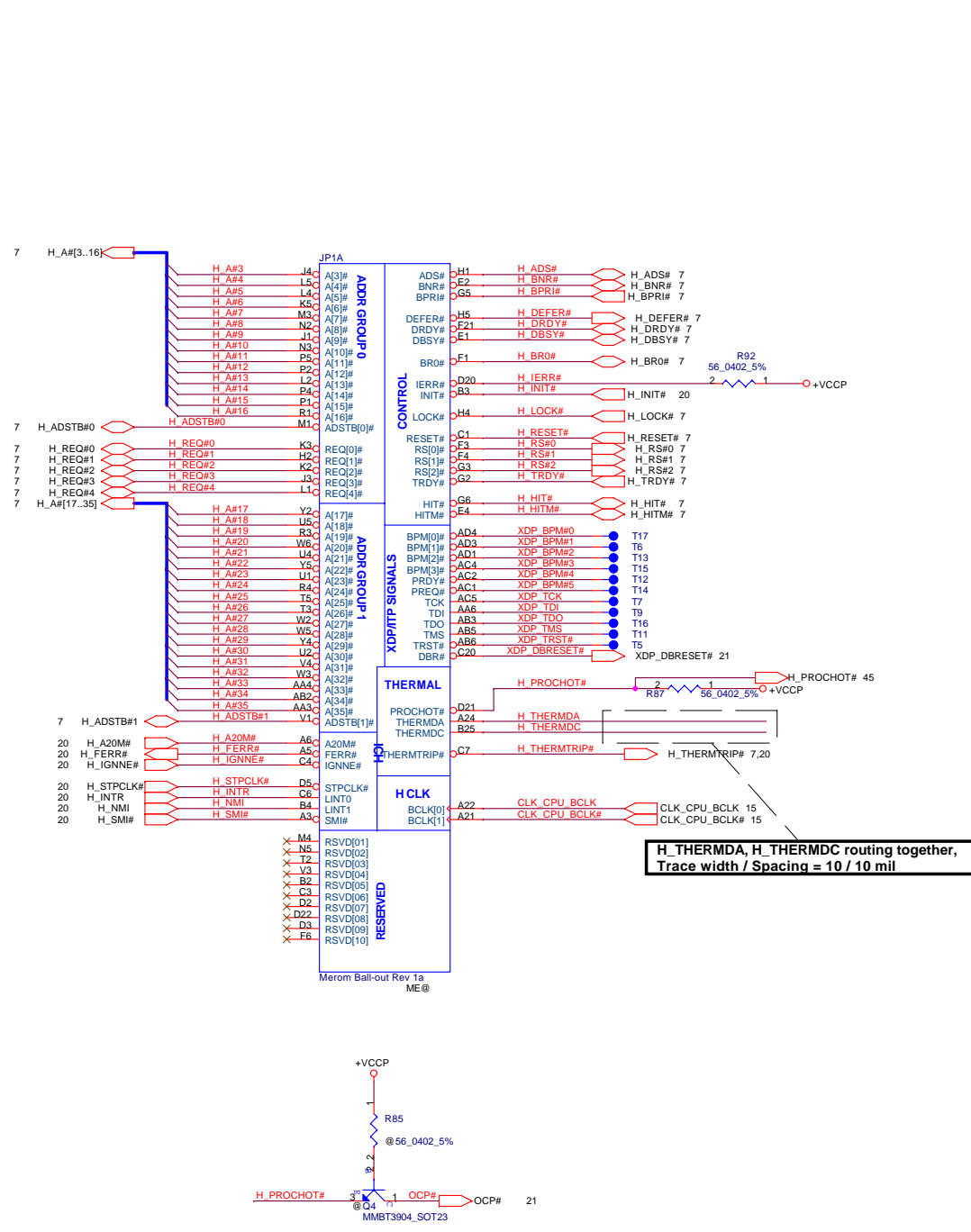
MARK	FUNCTION
@	NC FOR ALL
GIGA@	BCM5787
100@	BCM5906
UMA@	Internal 965GM
VGA@	965PM + Ext VGA

Address

USB PORT LIST

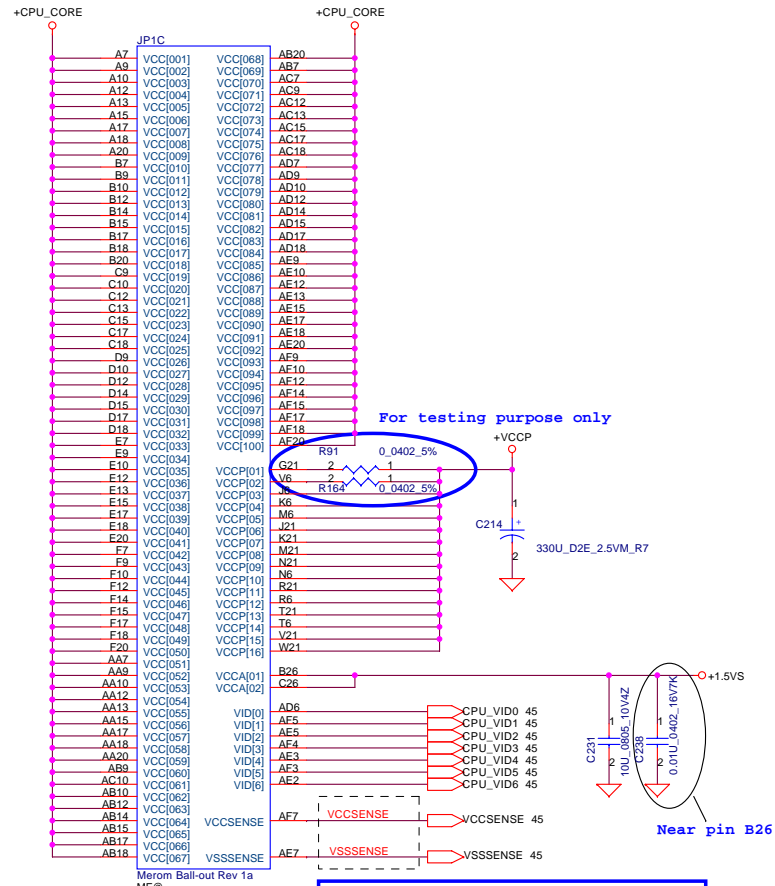
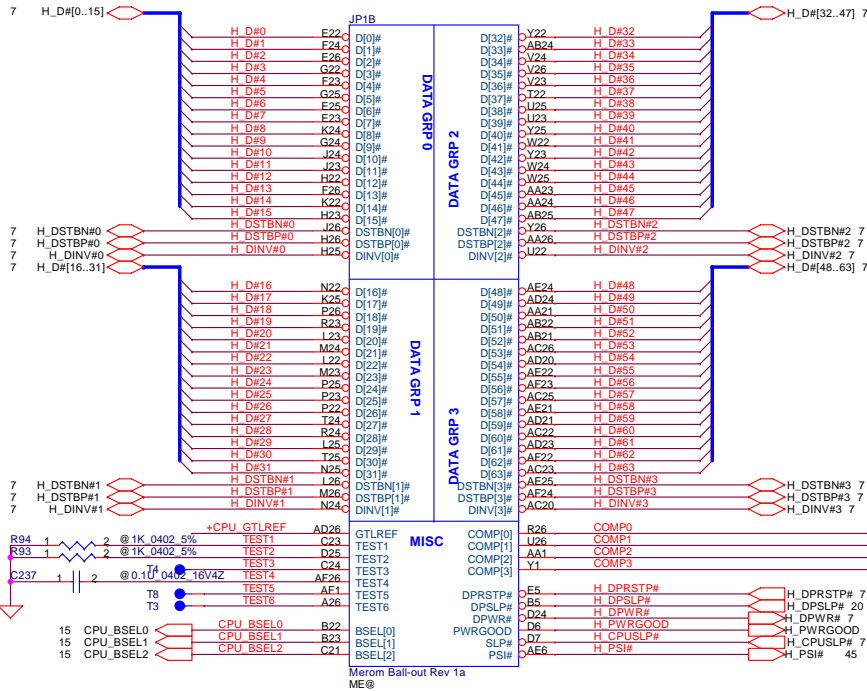
PORT	DEVICE
0	LEFT SIDE
1	WIRELESS
2	RIGHT SIDE
3	CMOS
4	RIGHT SIDE
5	NEW CARD
6	
7	BT (HDL20)
8	
9	3G

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Title			
Merom(1/3)-AGTL+/XDP			
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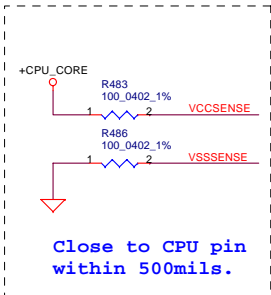
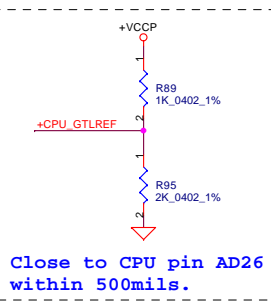


layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TFS

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

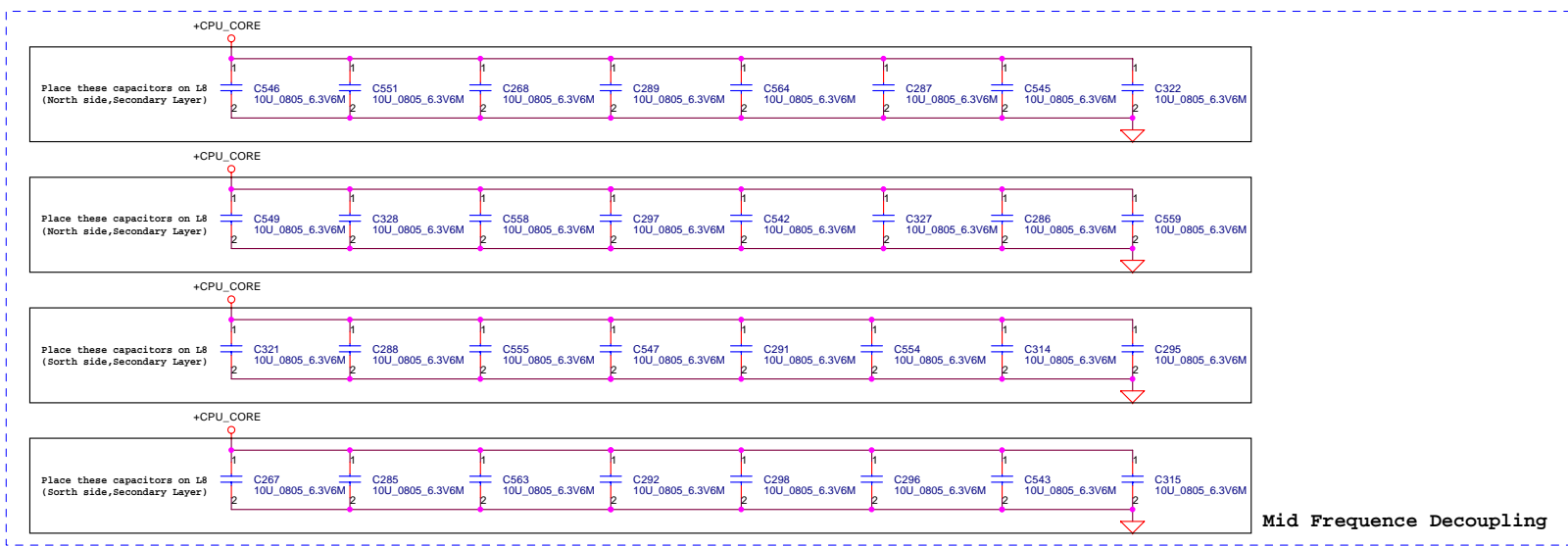
Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

Length match within 25 mils. The trace width/space/other is 20/7/25.

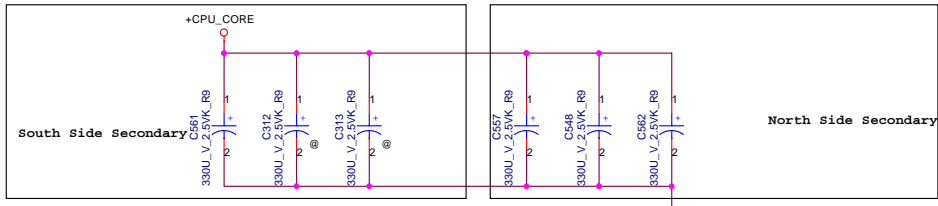


JP1D		
A4	VSS1001	VSS1092
A8	VSS1002	VSS1093
A11	VSS1003	VSS1094
A14	VSS1004	VSS1095
A16	VSS1005	VSS1096
A19	VSS1006	VSS1097
A23	VSS1007	VSS1098
B2	VSS1008	VSS1099
B6	VSS1009	VSS1100
B8	VSS1010	VSS1101
B11	VSS1011	VSS1102
B13	VSS1012	VSS1103
B16	VSS1013	VSS1104
B19	VSS1014	VSS1105
B21	VSS1015	VSS1106
B24	VSS1016	VSS1107
C5	VSS1017	VSS1108
C8	VSS1018	VSS1109
C11	VSS1019	VSS1110
C14	VSS1020	VSS1111
C16	VSS1021	VSS1112
C19	VSS1022	VSS1113
C2	VSS1023	VSS1114
C22	VSS1024	VSS1115
C25	VSS1025	VSS1116
D1	VSS1026	VSS1117
D4	VSS1027	VSS1118
D8	VSS1028	VSS1119
D11	VSS1029	VSS1120
D13	VSS1030	VSS1121
D16	VSS1031	VSS1122
D19	VSS1032	VSS1123
D23	VSS1033	VSS1124
D26	VSS1034	VSS1125
E3	VSS1035	VSS1126
E6	VSS1036	VSS1127
E8	VSS1037	VSS1128
E11	VSS1038	VSS1129
E14	VSS1039	VSS1130
E16	VSS1040	VSS1131
E19	VSS1041	VSS1132
E21	VSS1042	VSS1133
E24	VSS1043	VSS1134
F5	VSS1044	VSS1135
F8	VSS1045	VSS1136
F11	VSS1046	VSS1137
F13	VSS1047	VSS1138
F16	VSS1048	VSS1139
F19	VSS1049	VSS1140
F2	VSS1050	VSS1141
F25	VSS1051	VSS1142
G1	VSS1052	VSS1143
G4	VSS1053	VSS1144
G11	VSS1054	VSS1145
G23	VSS1055	VSS1146
G26	VSS1056	VSS1147
H3	VSS1057	VSS1148
H6	VSS1058	VSS1149
H21	VSS1059	VSS1150
H24	VSS1060	VSS1151
J2	VSS1061	VSS1152
J5	VSS1062	VSS1153
J22	VSS1063	VSS1154
J25	VSS1064	VSS1155
K1	VSS1065	VSS1156
K4	VSS1066	VSS1157
K23	VSS1067	VSS1158
K26	VSS1068	VSS1159
L3	VSS1069	VSS1160
L6	VSS1070	VSS1161
L21	VSS1071	VSS1162
L24	VSS1072	VSS1163
M2	VSS1073	VSS1164
M5	VSS1074	VSS1165
M22	VSS1075	VSS1166
M25	VSS1076	VSS1167
N1	VSS1077	VSS1168
N4	VSS1078	VSS1169
N23	VSS1079	VSS1170
N26	VSS1080	VSS1171
P3	VSS1081	VSS1172
		VSS1173
		VSS1174
		VSS1175
		VSS1176
		VSS1177
		VSS1178
		VSS1179
		VSS1180
		VSS1181
		VSS1182
		VSS1183
		VSS1184
		VSS1185
		VSS1186
		VSS1187
		VSS1188
		VSS1189
		VSS1190
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		VSS1192
		VSS1193
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		VSS1199
		VSS1200

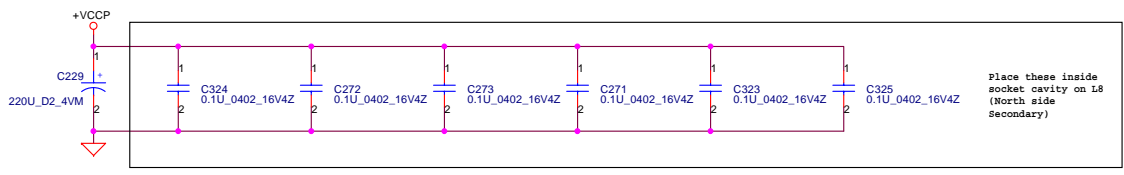
Merom Ball-out Rev 1a



Mid Frequency Decoupling

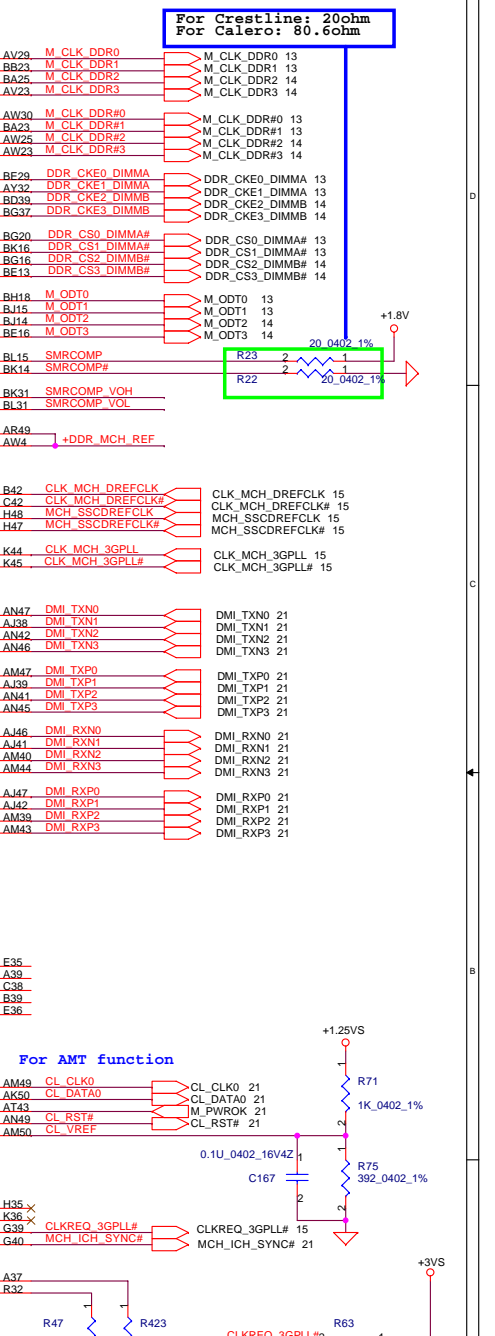
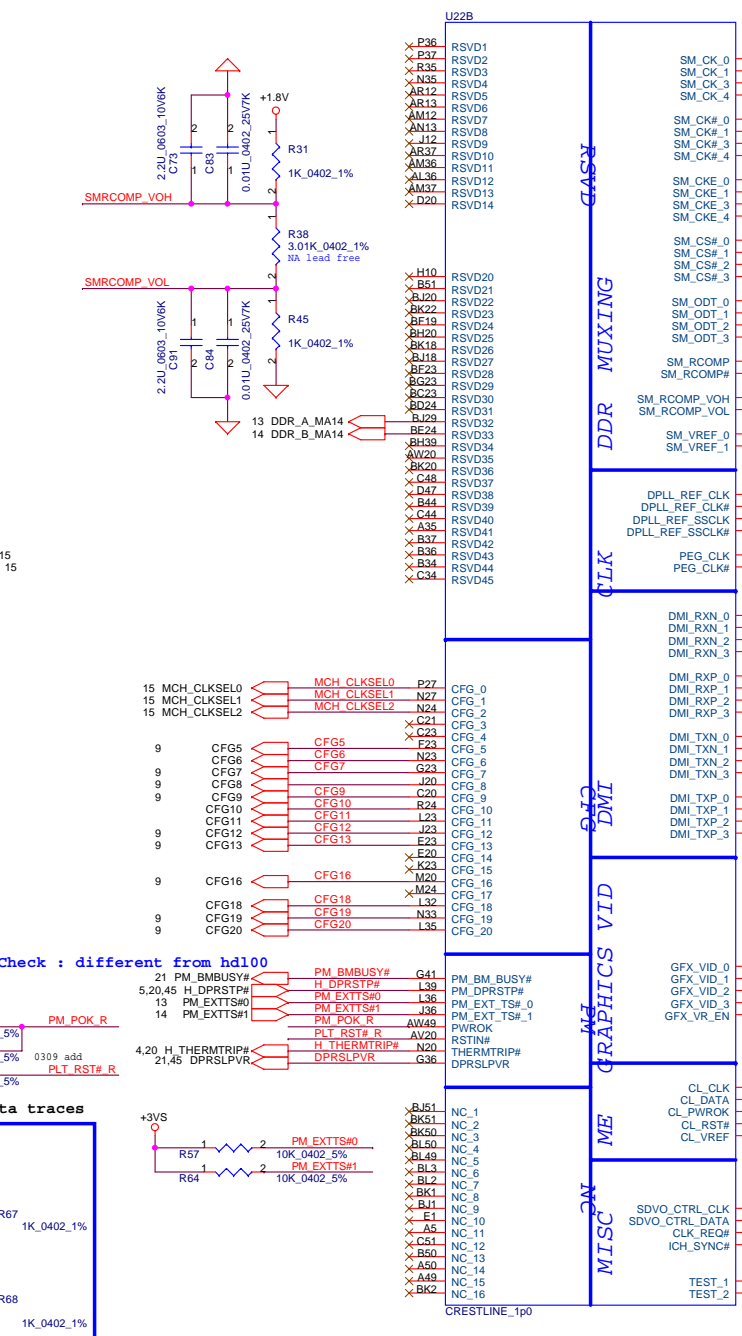
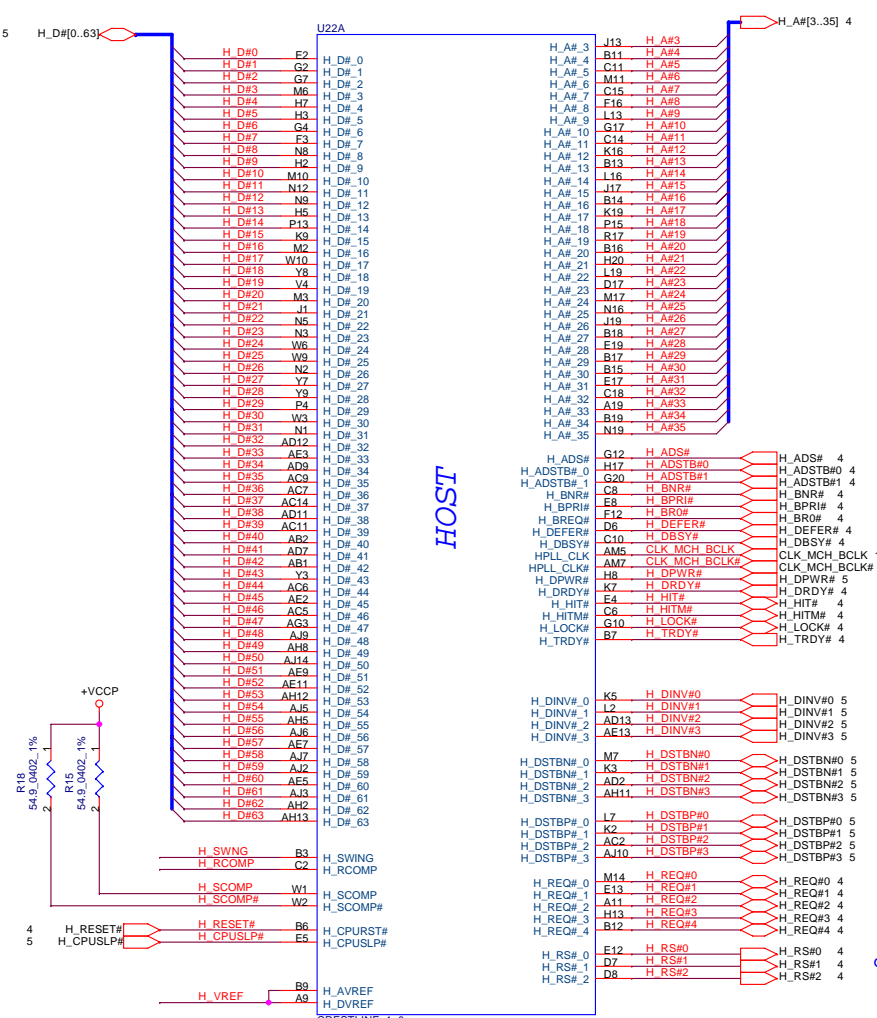


ESR <= 1.5m ohm
Capacitor > 1980uF

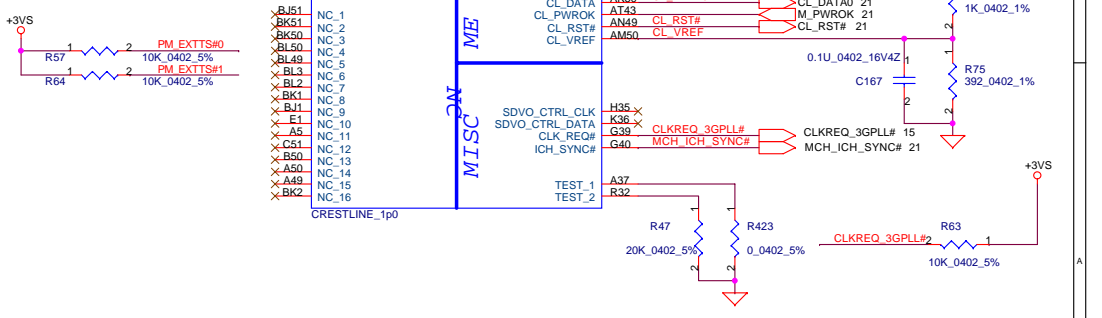
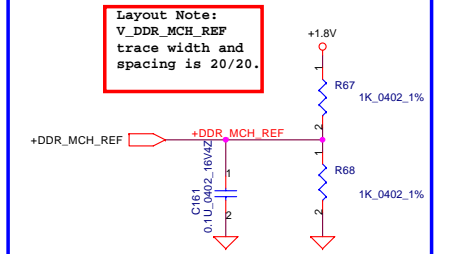
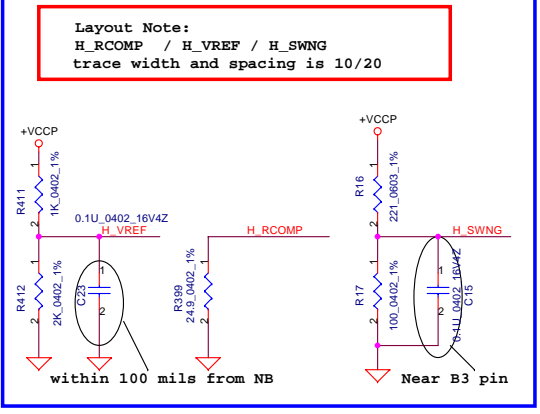


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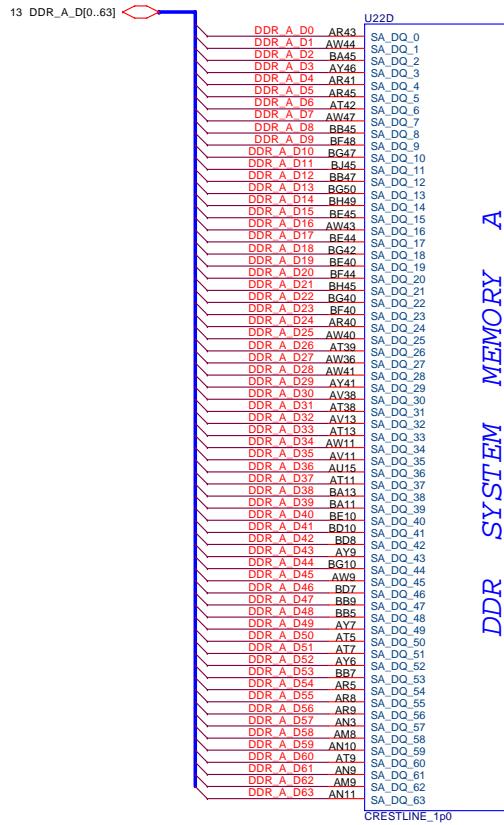
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Merom(3/3)-GND&Bypass		
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layout note:
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces

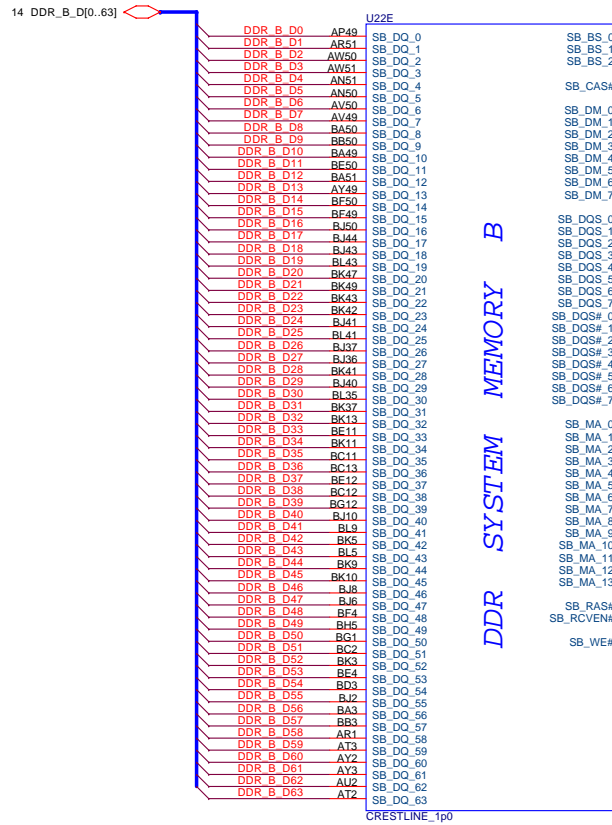


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CRESTLINE_1p0

DDR SYSTEM MEMORY A

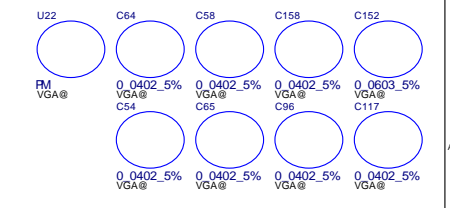
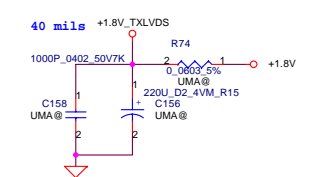
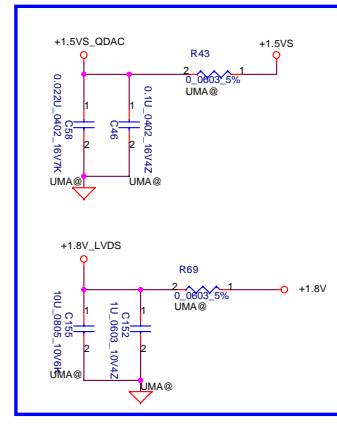
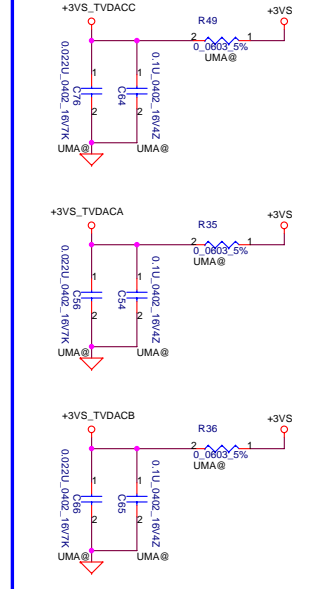
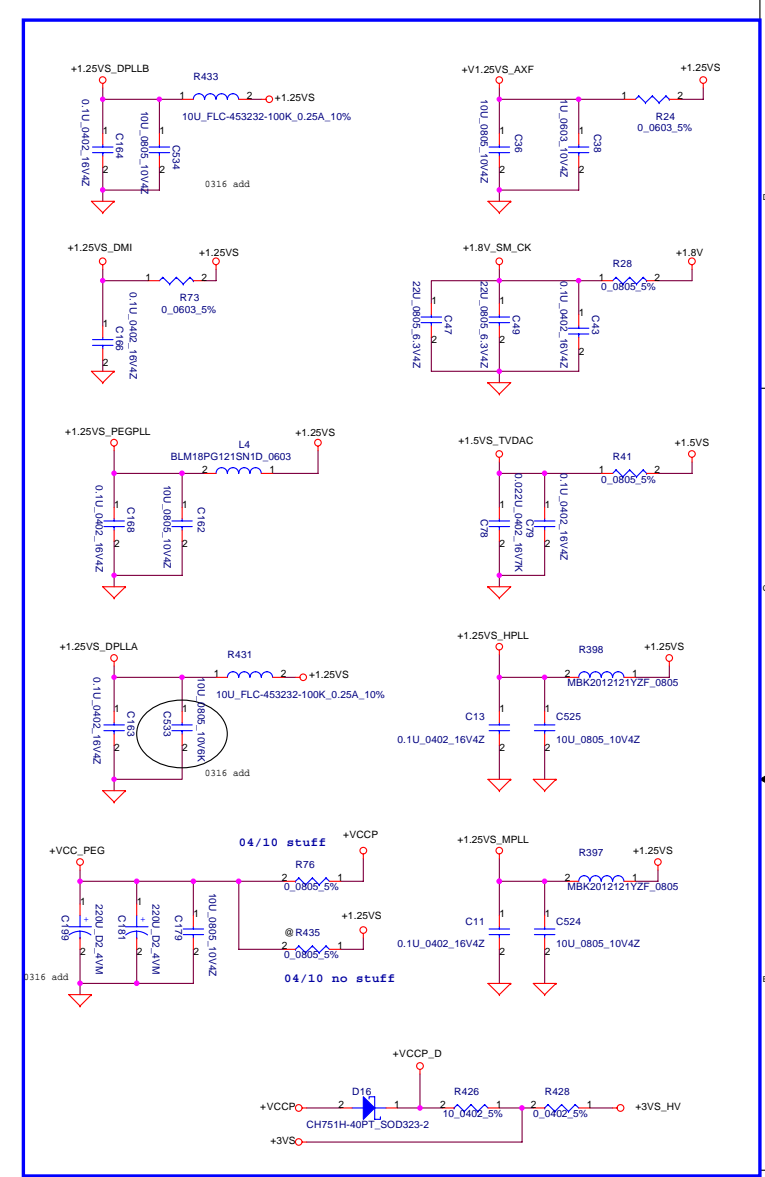
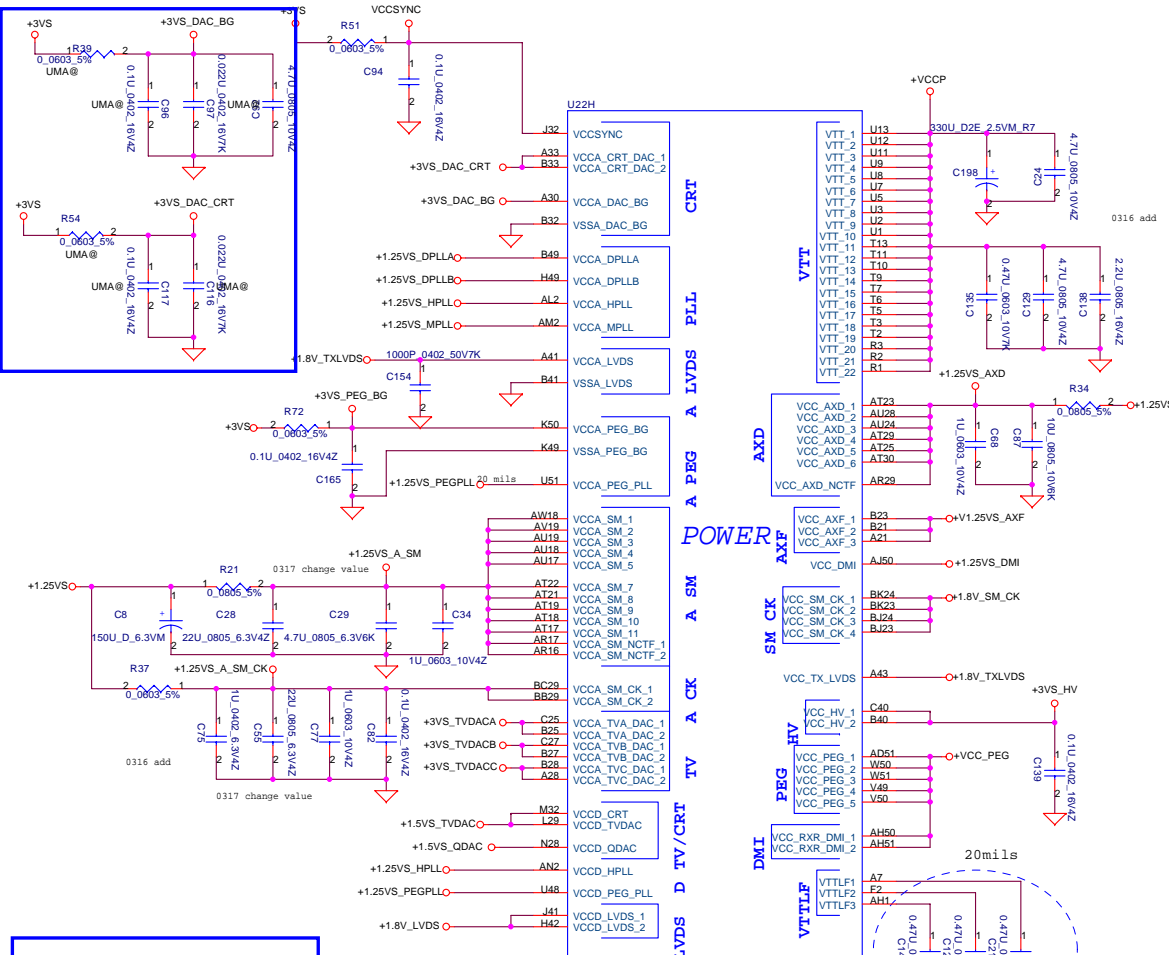


CRESTLINE_1p0

DDR SYSTEM MEMORY B

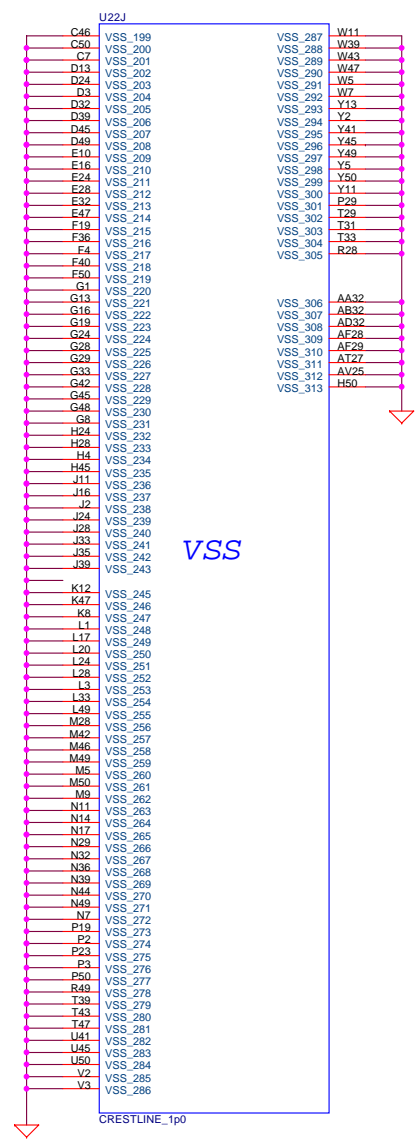
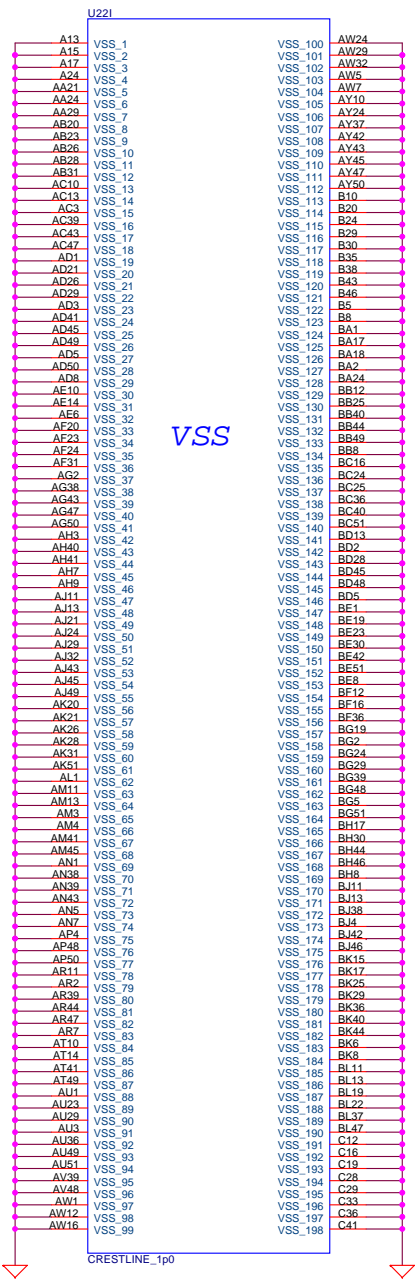
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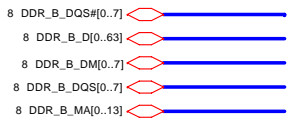


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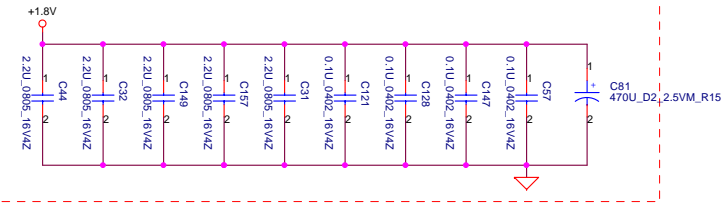
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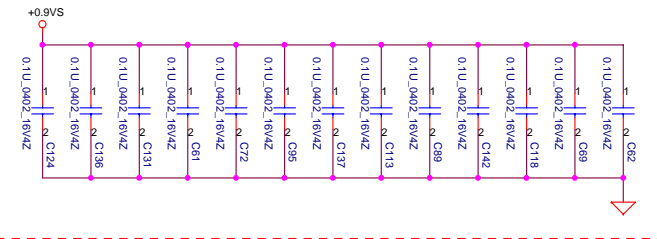
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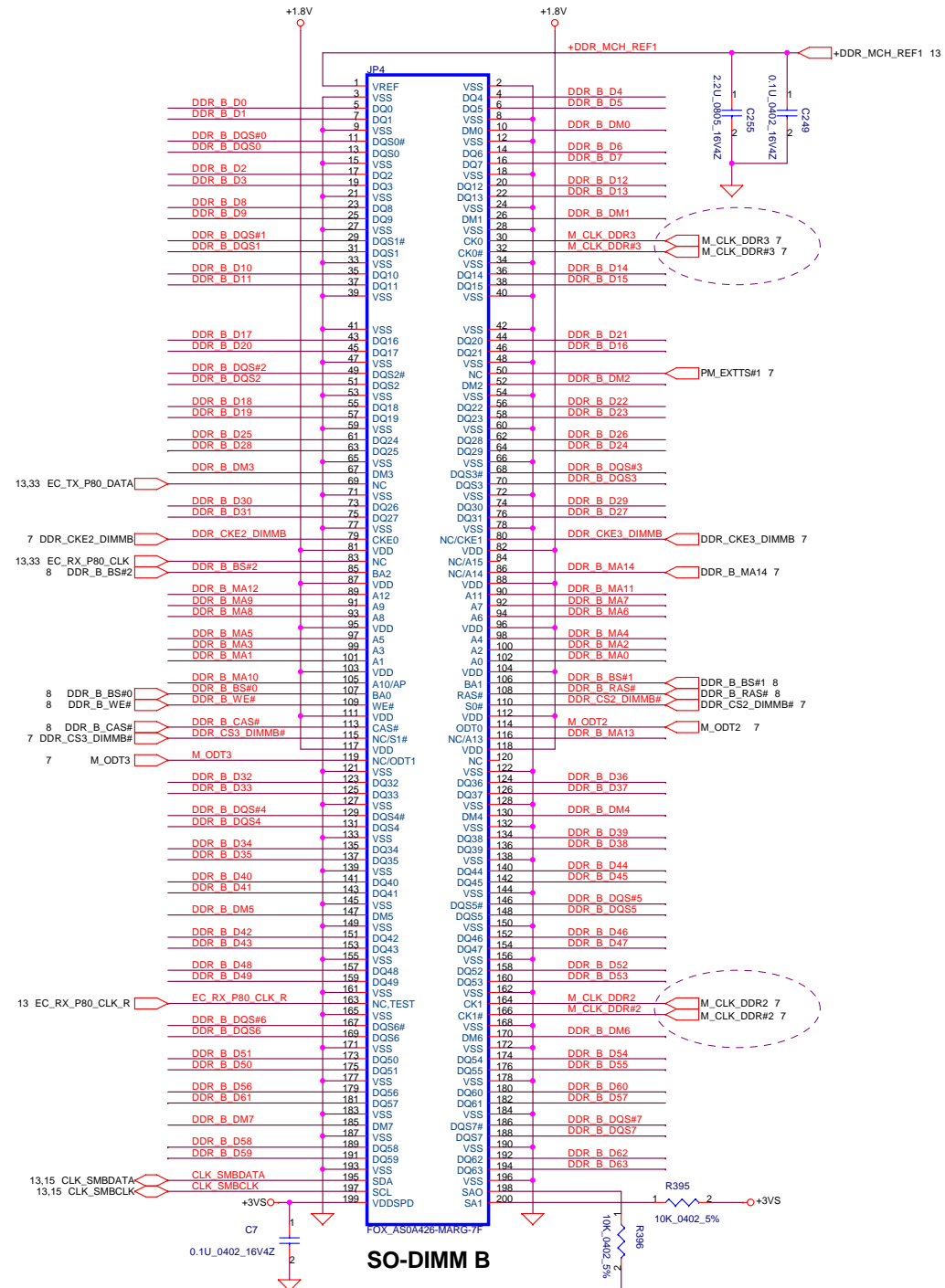
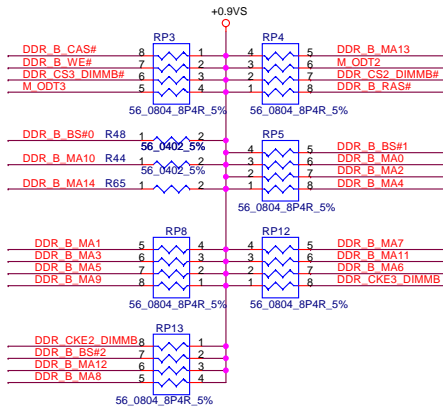
Layout Note:
Place near JP42



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistor closely JP42, all trace length Max=1.5"

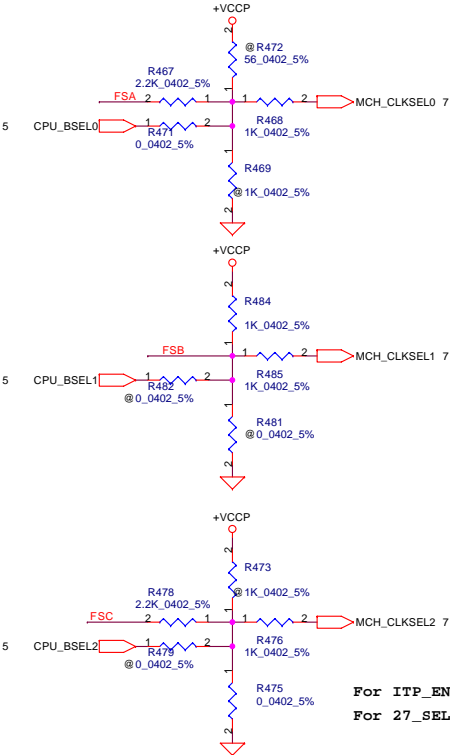


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				DDR II-SODIMM SLOT2	
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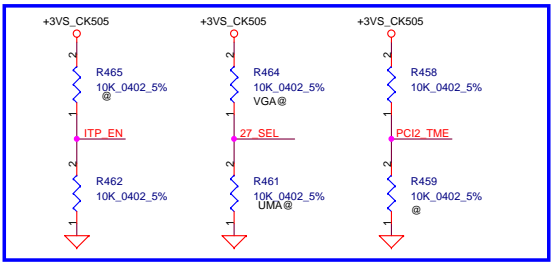
FSLC	FSLB	FSLA	CPU	SRC	PCI
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz
0	1	0	200	100	33.3
0	1	1	166	100	33.3

FSB Frequency Selet:

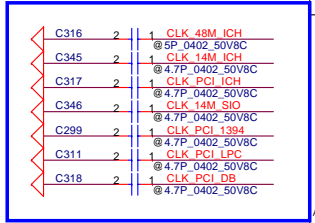
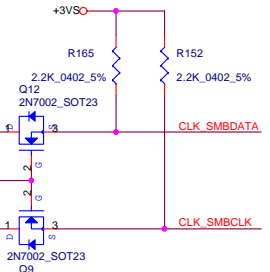
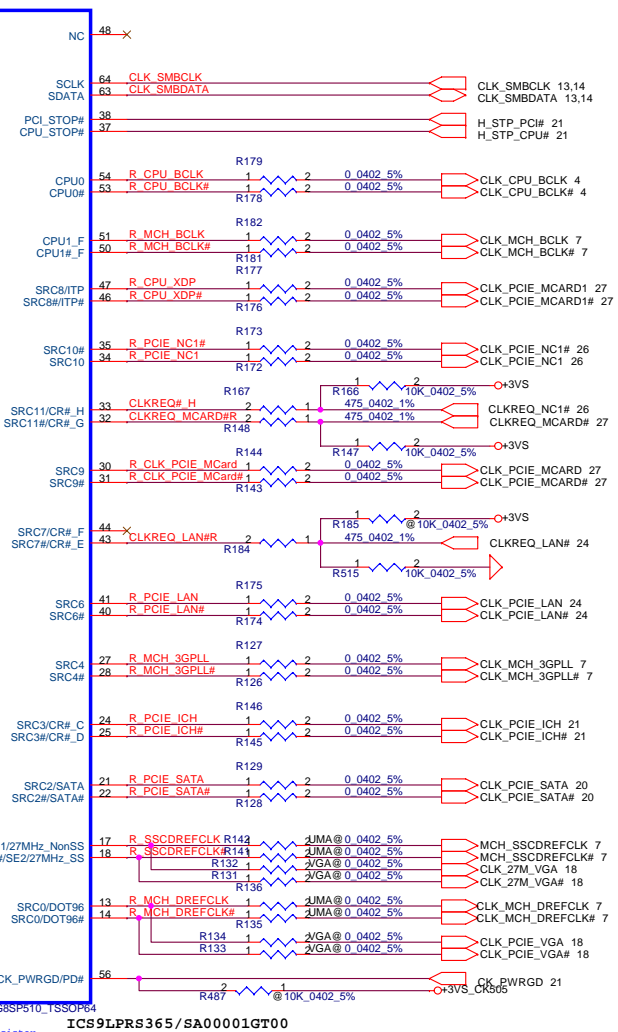
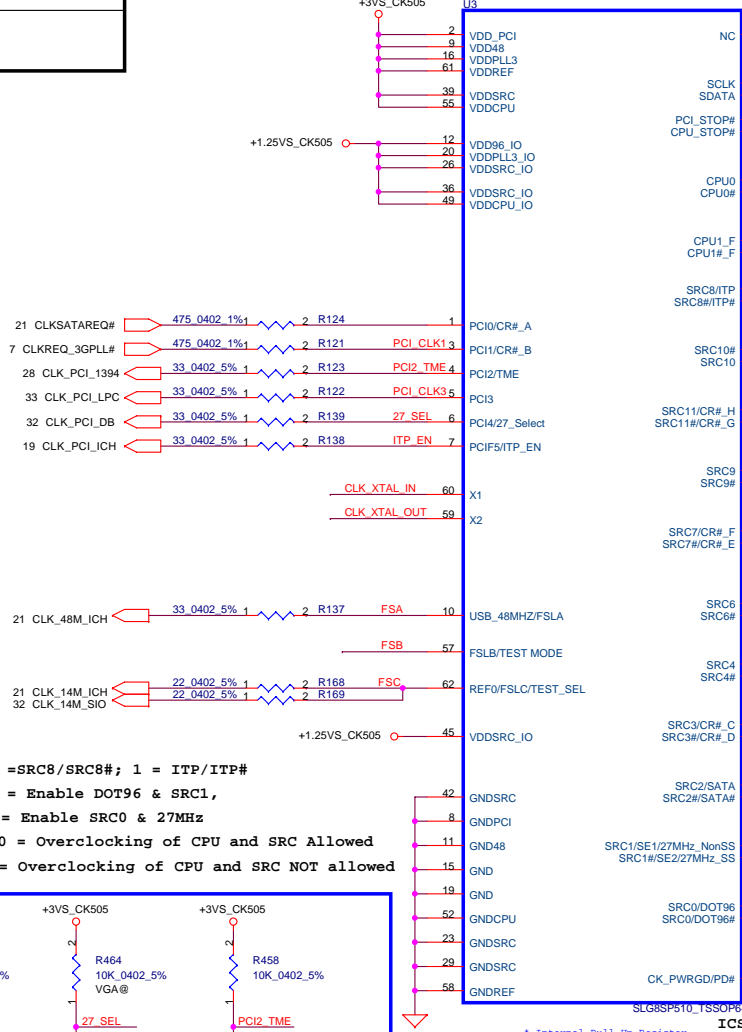
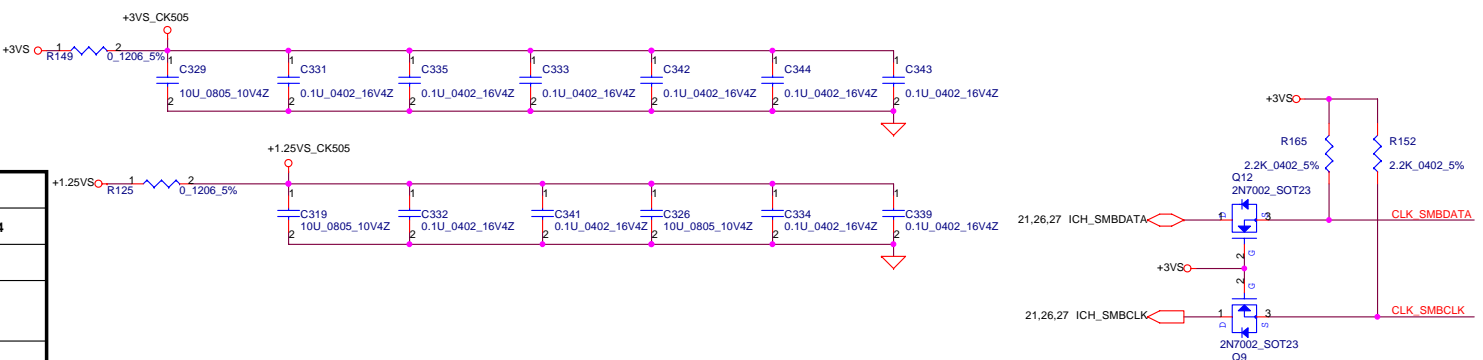
CPU Driven	Stuff	R919	R940	R956
*(Default)	No Stuff	R914	R921	R930
	Stuff	R959	R930	R914
667MHz	No Stuff	R919	R940	R956
	Stuff	R949	R943	R921
800MHz	No Stuff	R919	R940	R956
	Stuff	R949	R943	R914



For ITP_EN, 0 = SRC8/SRC8#, 1 = ITP/ITP#
 For 27_SEL, 0 = Enable DOT96 & SRC1, 1 = Enable SRC0 & 27MHz
 For PCI2_EN, 0 = Overclocking of CPU and SRC Allowed, 1 = Overclocking of CPU and SRC NOT allowed

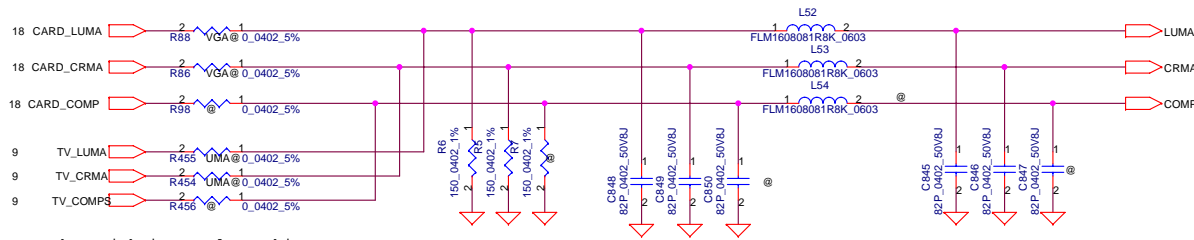


Routing the trace at least 10mil



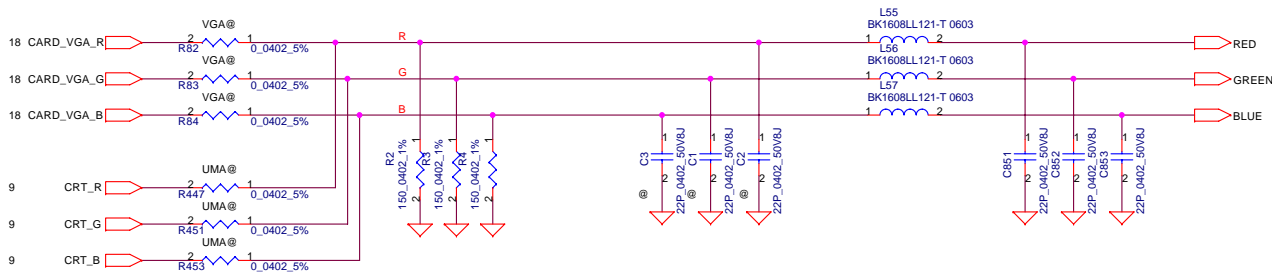
Place close to U41

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Issued Date	2006/08/04	Deciphered Date	2006/10/06	Compal Electronics, Inc.
				Clock generator
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Date: Monday, December 25, 2006				Rev 0.1
Sheet 15 of 47				

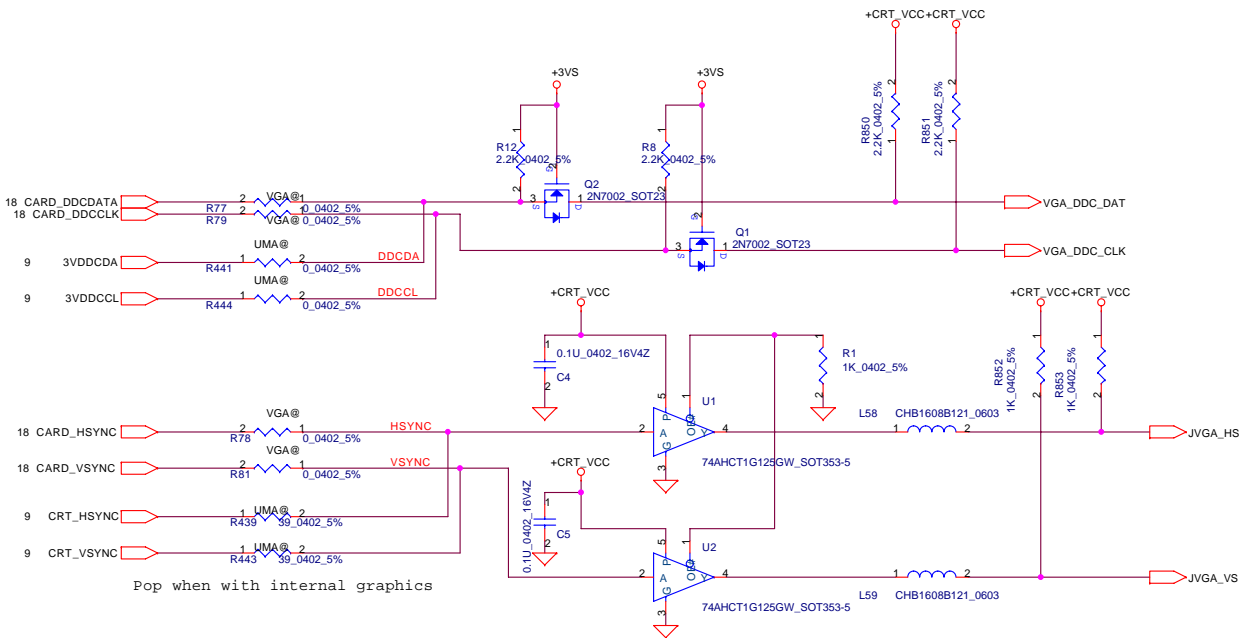


Pop when with internal graphics

CRT Conn.



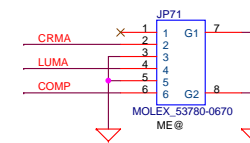
Pop when with internal graphics



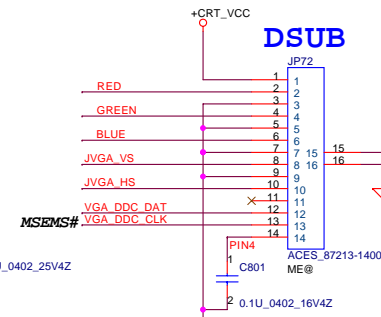
Pop when with internal graphics

VGA I/O PORT Connector

S-VIDEO



DSUB

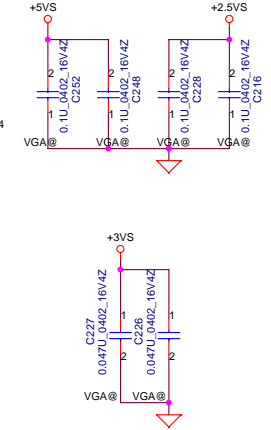
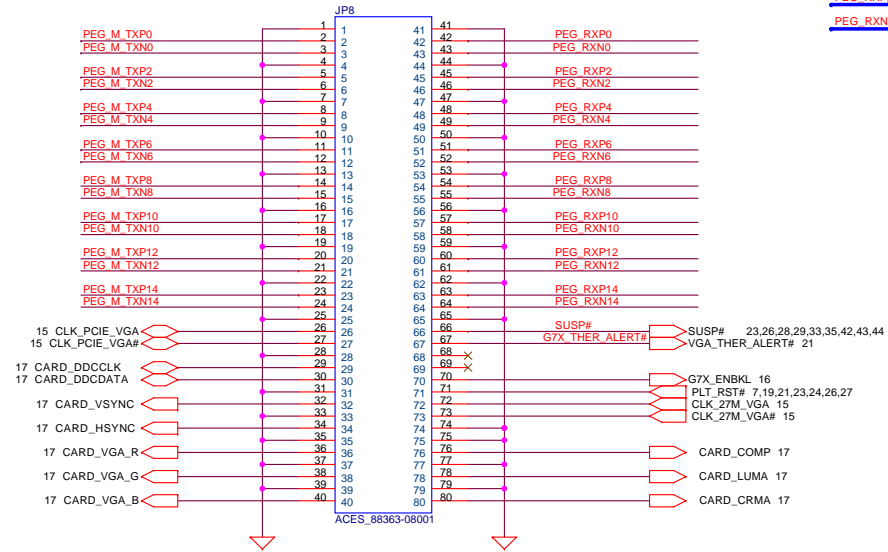
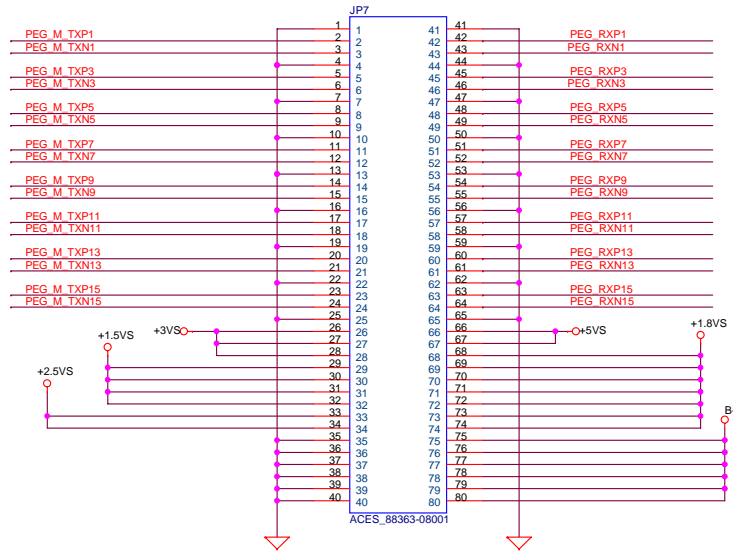


PIN ASSIGNMENT

PIN	D-SUB	FUNCTION	PIN	SVIDEO	FUNCTION
1	9	+CRT_VCC	1	1	NC
2	1	RED	2	4	CRMA
3	6	GND	3	2	GND
4	2	GREEN	4	3	LUMA
5	7	GND	5	5	GND
6	3	BLUE	6	6	CVBS
7	8	GND			
8	14	VSYNC			
9	10	GND			
10	13	HSYNC			
11	11	SENSE			
12	12	SM_DAT			
13	15	SM_CLK			
14	4	PIN4			

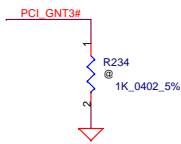
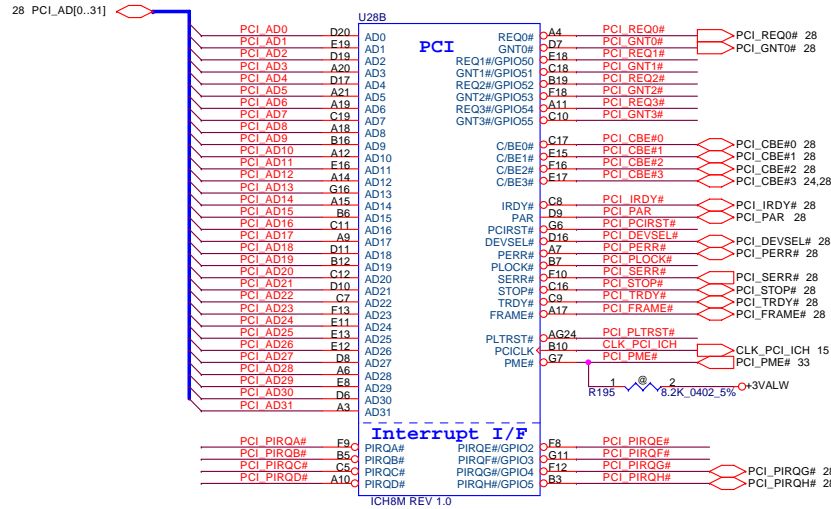
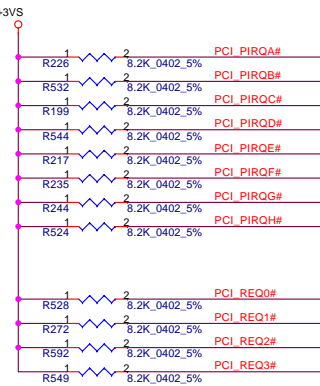
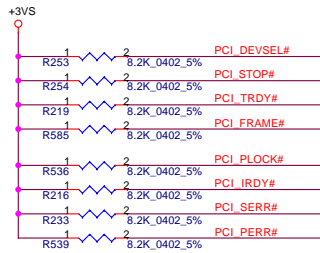
MAX. 4.06A @ 1.8V
 MAX. 130mA @ 2.5V
 MAX. 655mA @ 3.3V

PEG_M_TXP[0..15] PEG_M_TXN[0..15] 9
 PEG_M_TXN[0..15] PEG_M_TXN[0..15] 9
 PEG_RXP[0..15] PEG_RXP[0..15] 9
 PEG_RXN[0..15] PEG_RXN[0..15] 9



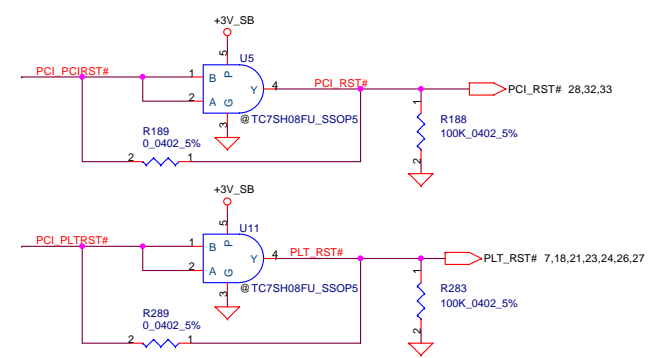
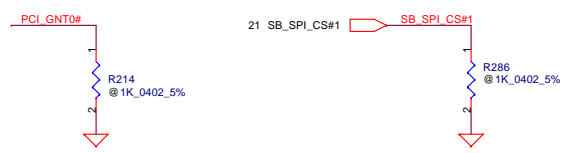
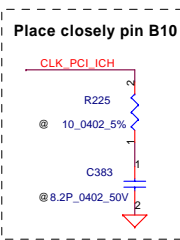
Title		
Compal Electronics, Inc.		
VGA/B connector		
Size	Document Number	Rev
Customer	IGT30 LA-3571P	0.1
Date:	Monday, December 25, 2006	Sheet 18 of 47

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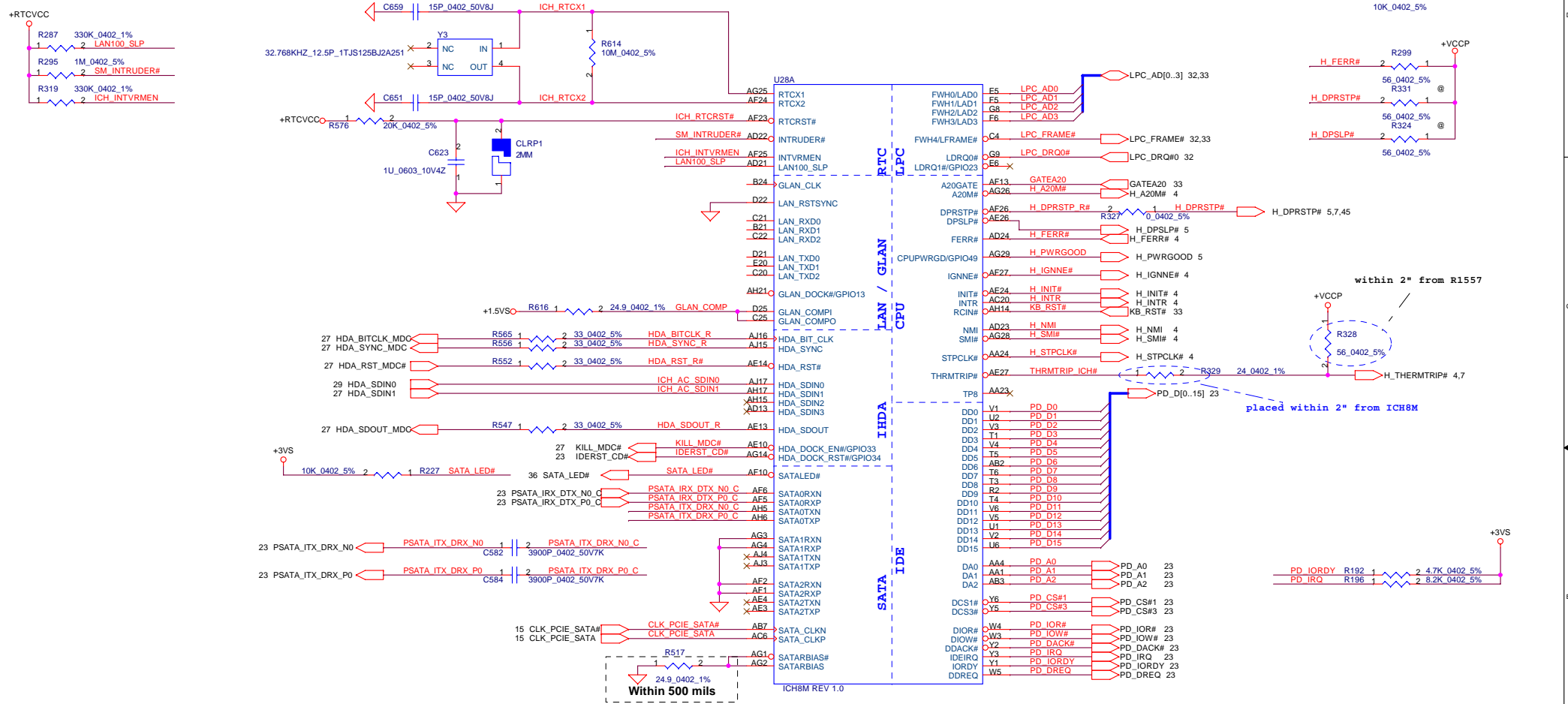
A16 swap override Strap	
Low=	A16 swap override Enble
High=	Default *

Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

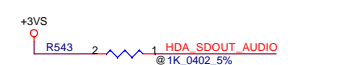


ICH8M Internal VR Enable Strap
(Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)

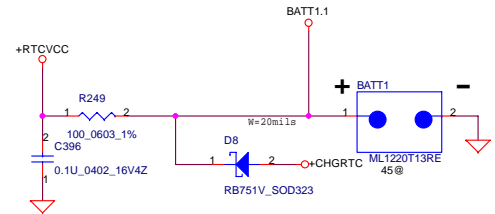
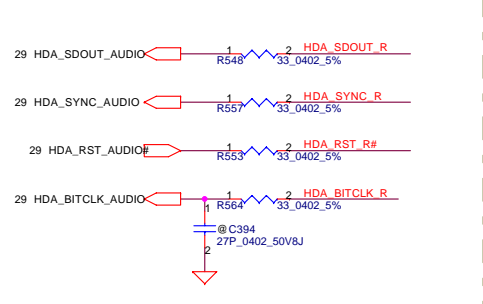
LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)
ICH_INTVRMEN	High = Internal VR Enabled(Default)



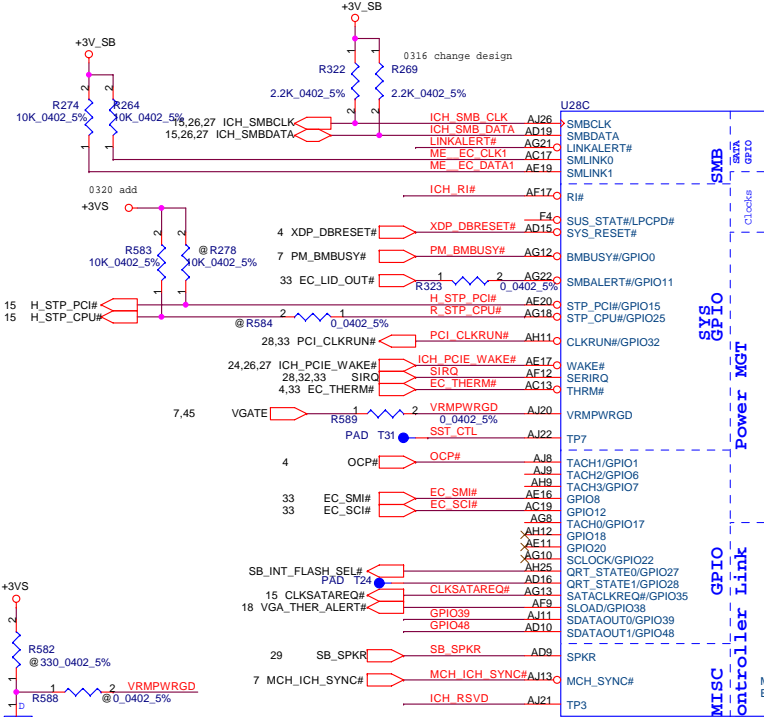
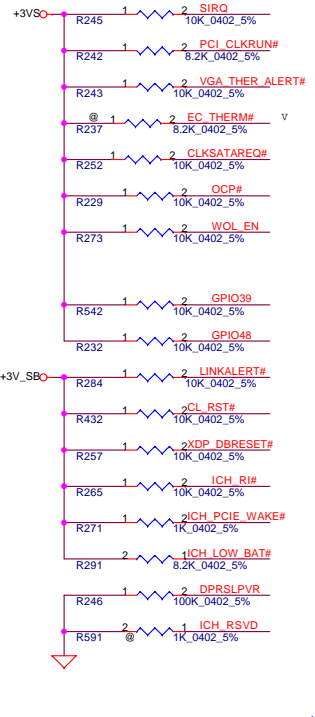
XOR CHAIN ENTRANCE STRAP:RSVD



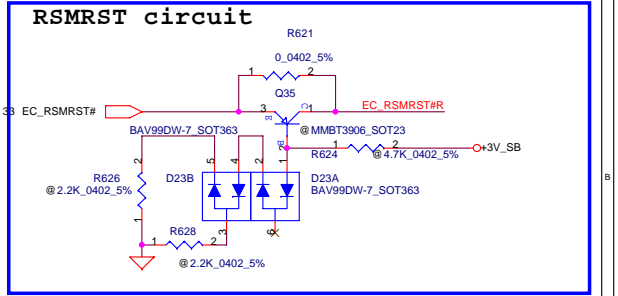
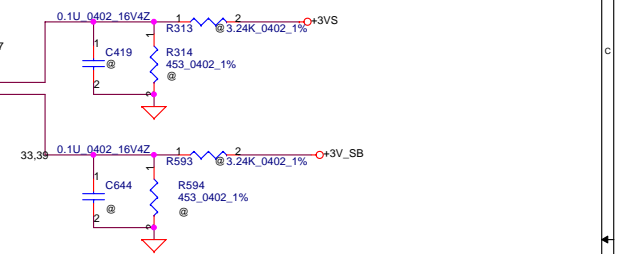
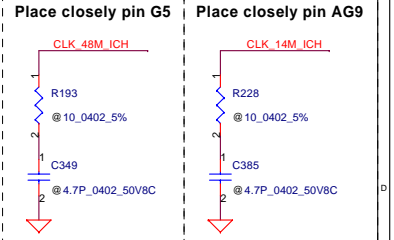
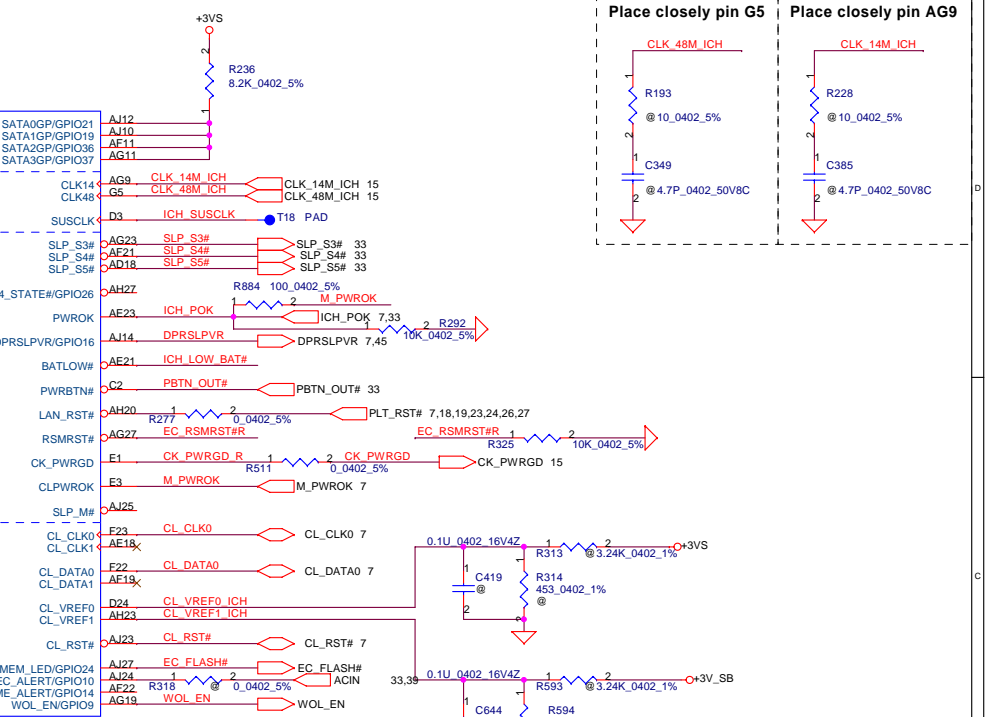
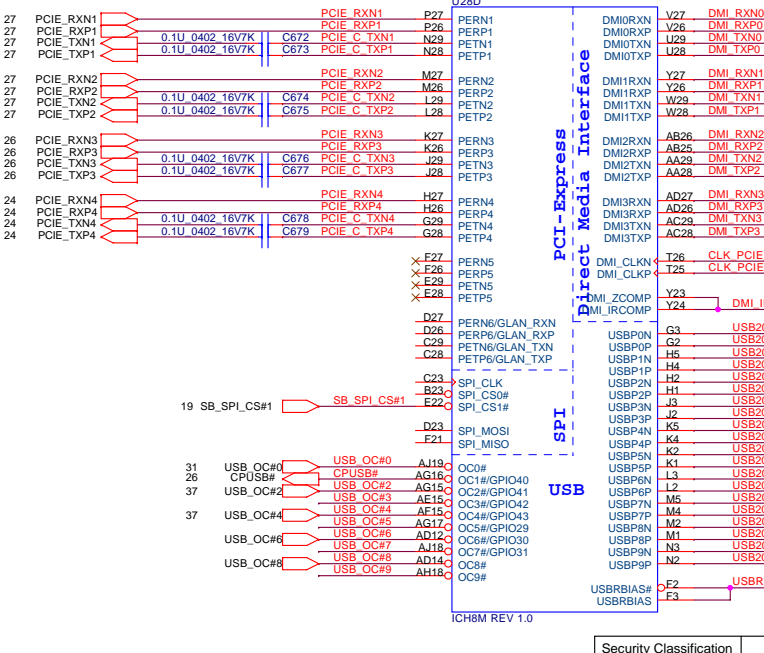
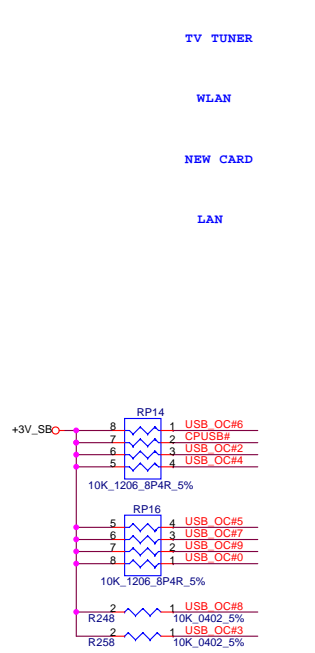
Close to ICH



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Issued Date	2006/08/04	Deciphered Date	2006/10/06	ICH8(2/4) LAN,HD,IDE,LPC	
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				Date	Monday, December 25, 2006
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				Rev	0.1

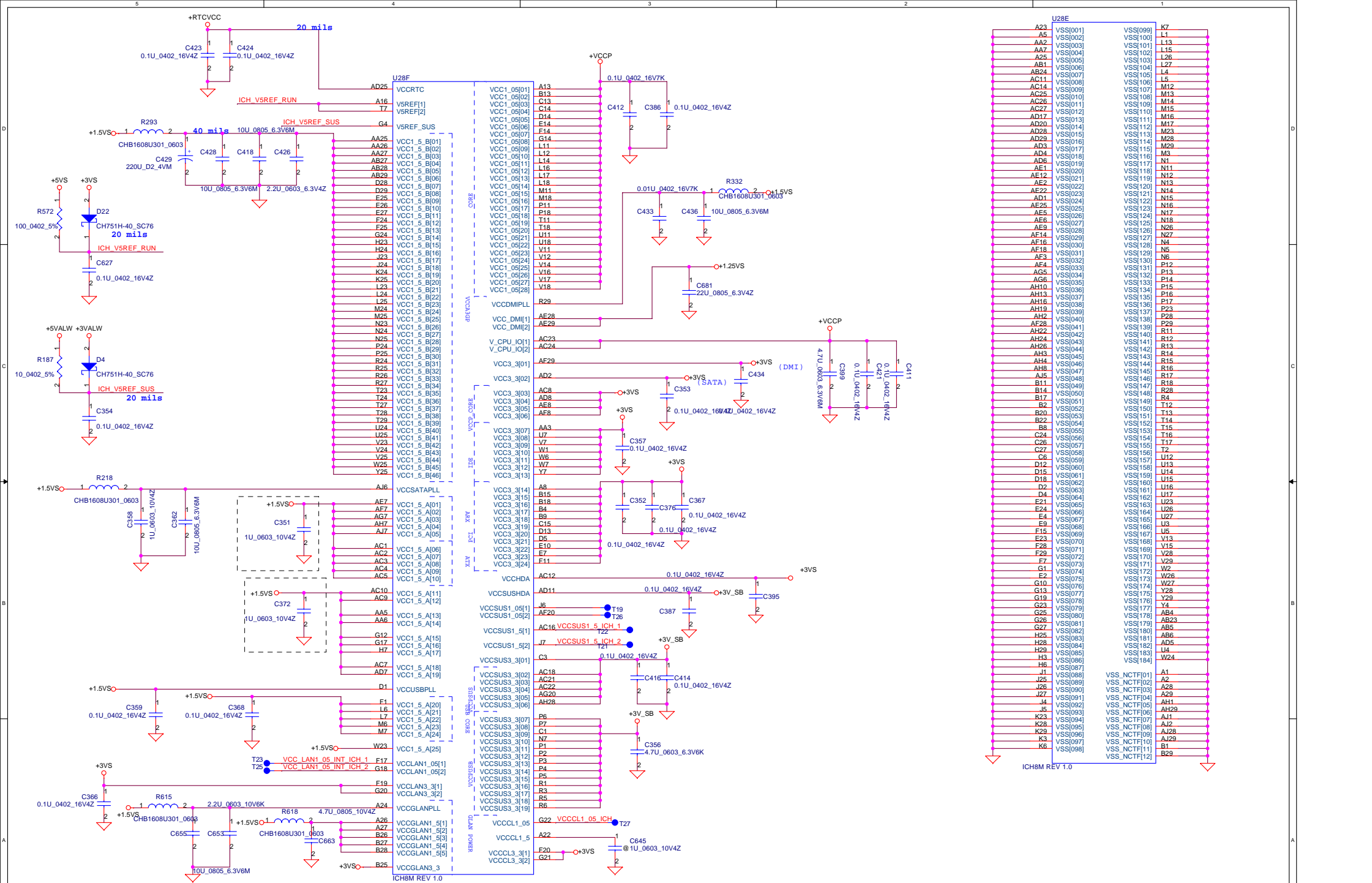


low-->default
High-->No boot



USB PORT LIST

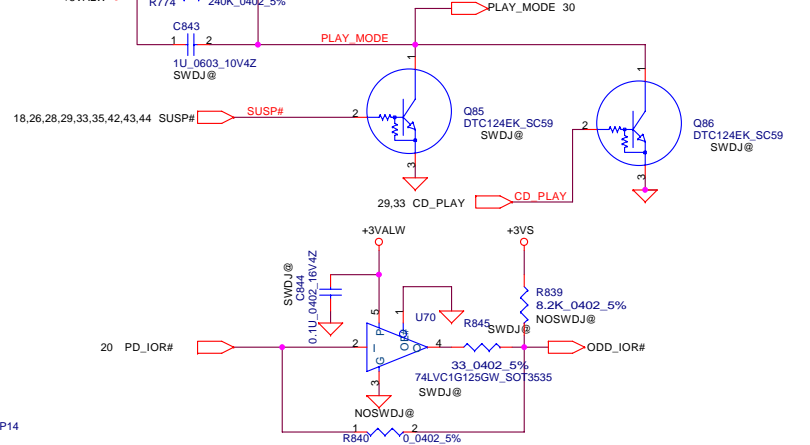
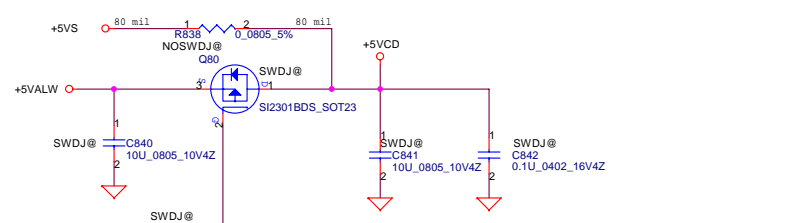
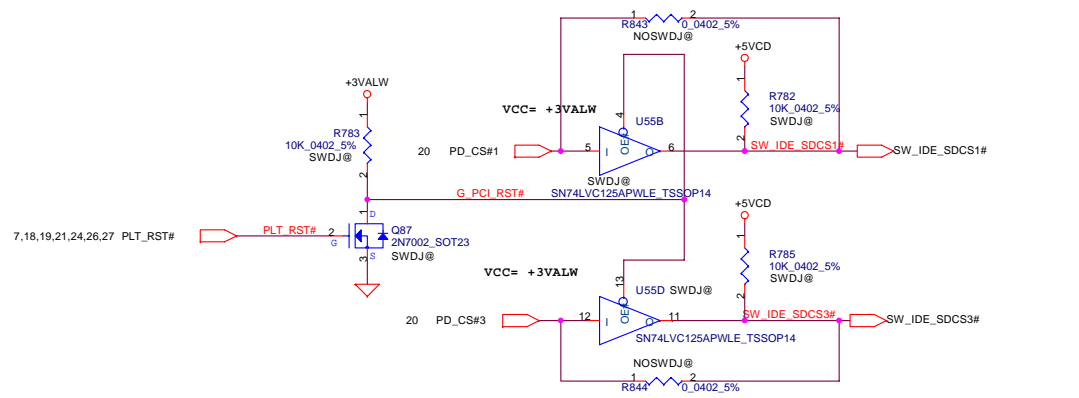
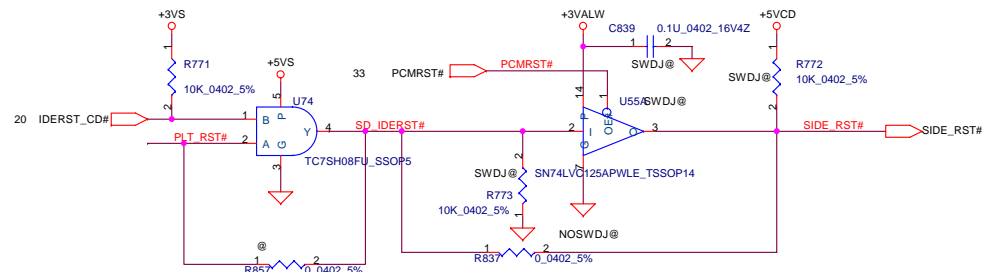
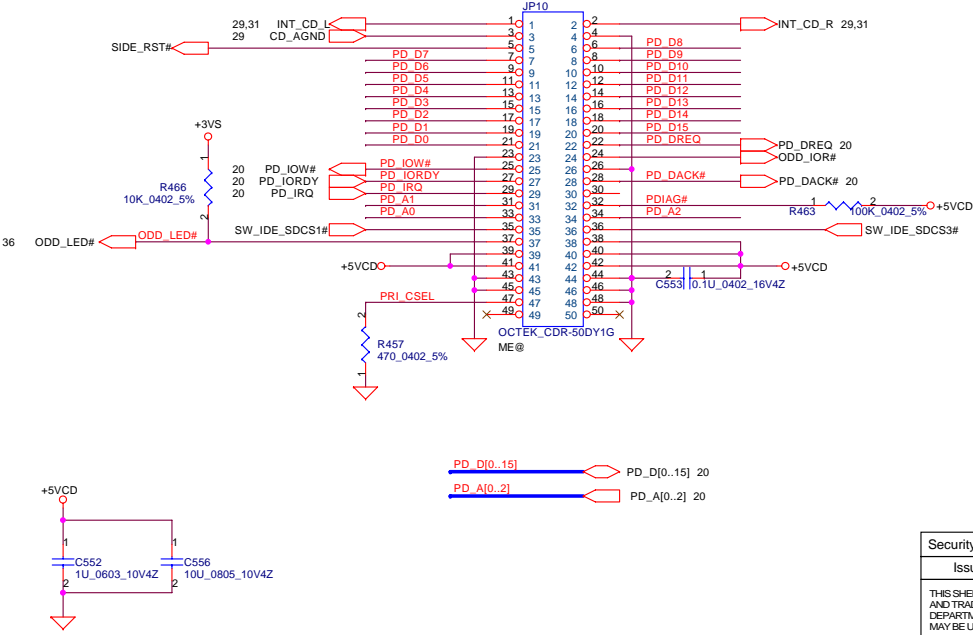
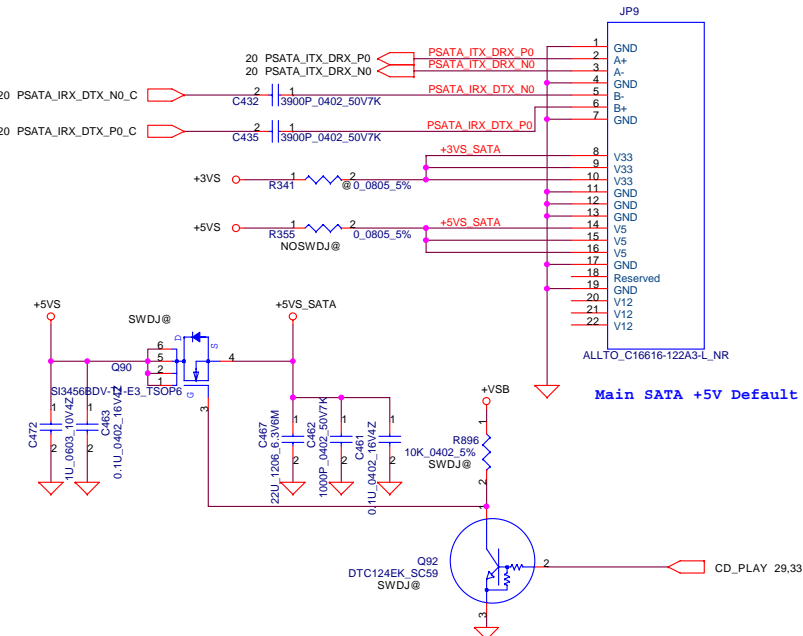
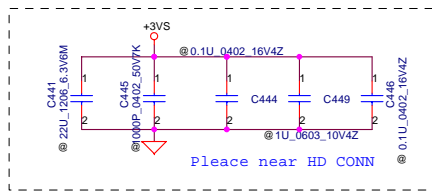
PORT	DEVICE
0	LEFT SIDE
1	WIRELESS
2	RIGHT SIDE
3	CMOS
4	RIGHT SIDE
5	NEW CARD
6	
7	BT (HDL20)
8	
9	3G



Security Classification	Compal Secret Data	
Issued Date	2006/08/04	Deciphered Date
		2006/10/06

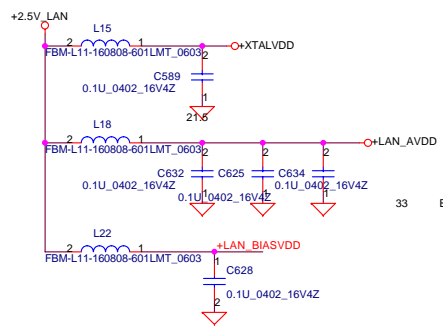
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		ICH8(4/4) POWER&GND	
Size	Document Number	Rev	
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Date:	Monday, December 25, 2006	Sheet	22 of 47

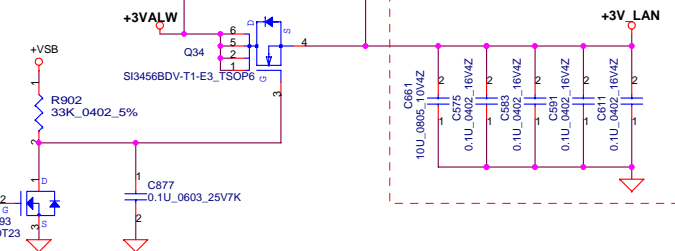


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				Custom	IGT30 LA-3571P
				Date	Monday, December 25, 2006
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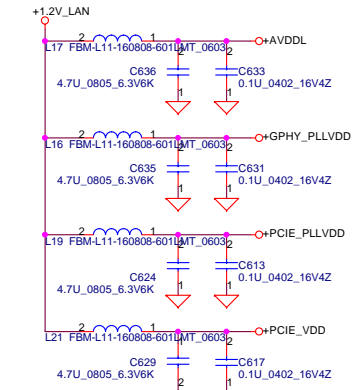
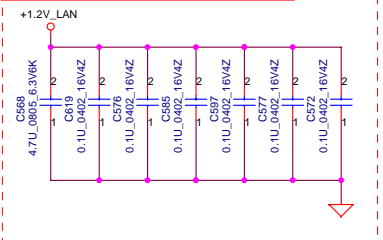
Layout Notice : Filter place as close chip as possible.



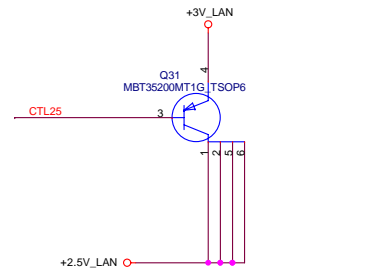
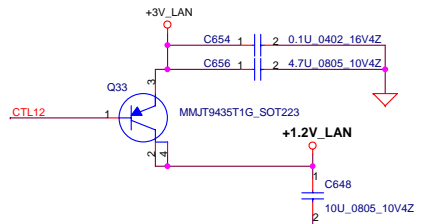
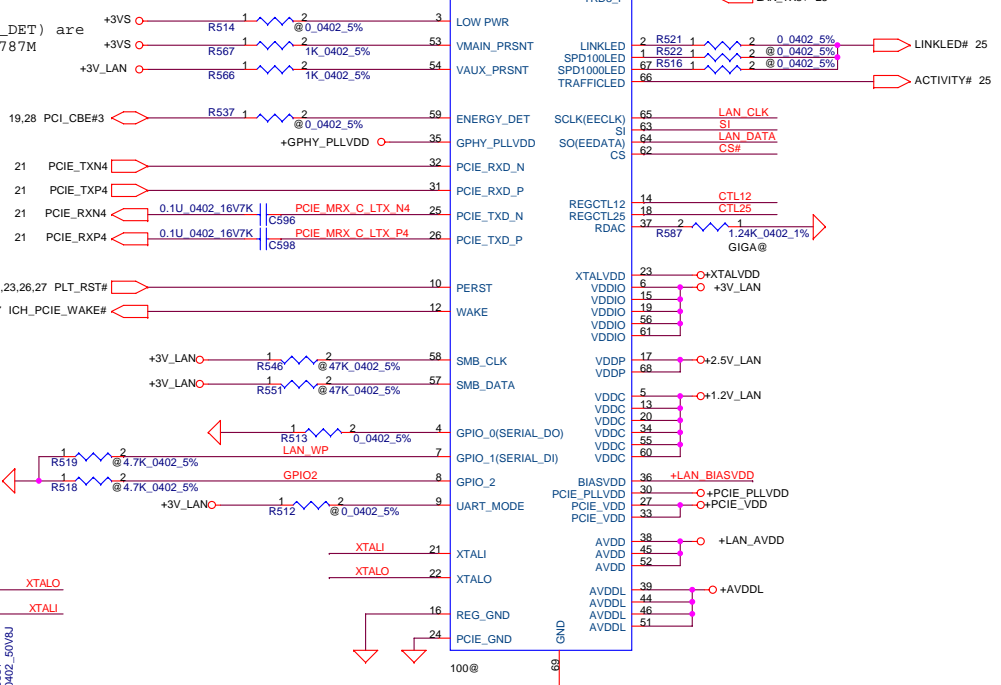
Layout Notice : Place as close chip as possible.



Layout Notice : 1.2V filter. Place as close chip as possible.



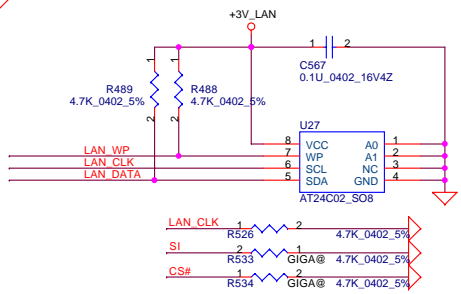
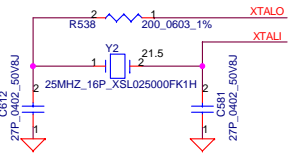
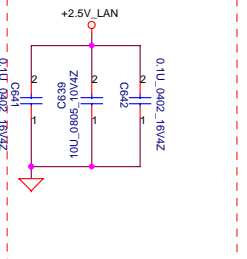
(CLKREQ#) and (ENERGY_DET) are only supported in BCM5787M



Notice : 4.7u 6.3V capacitor Thickness 1.25mm

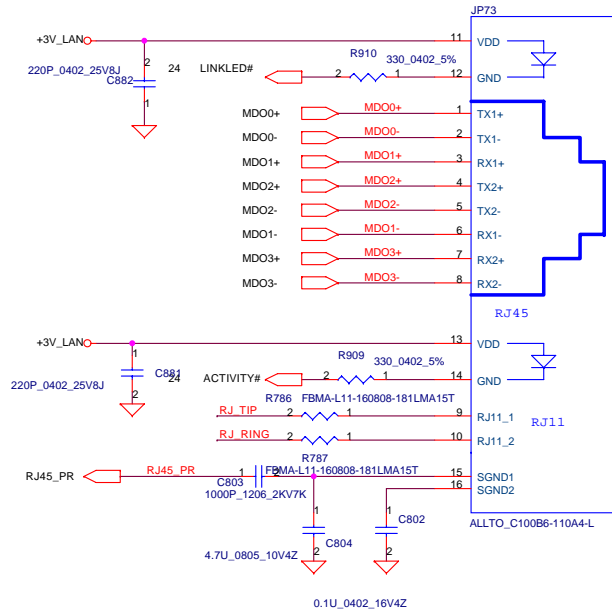
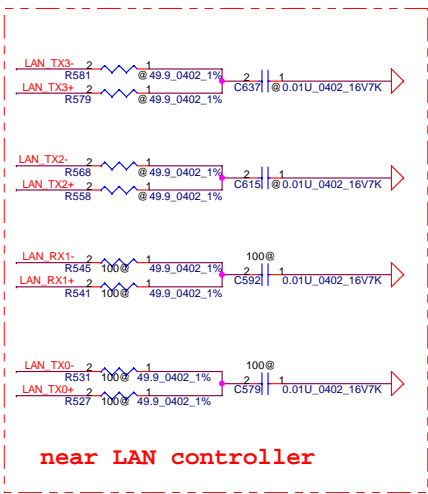
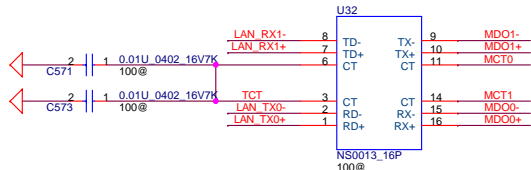
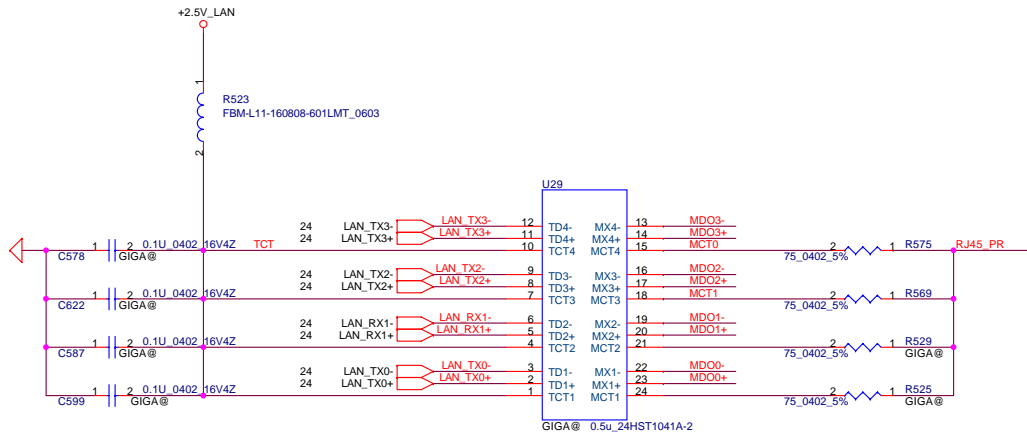
Layout Notice : Filter place as close chip as possible.

Layout Notice : Place as close chip as possible.

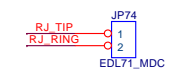


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				Customer	IGT30 LA-3571P	0.1
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RJ11+RJ45 CONN

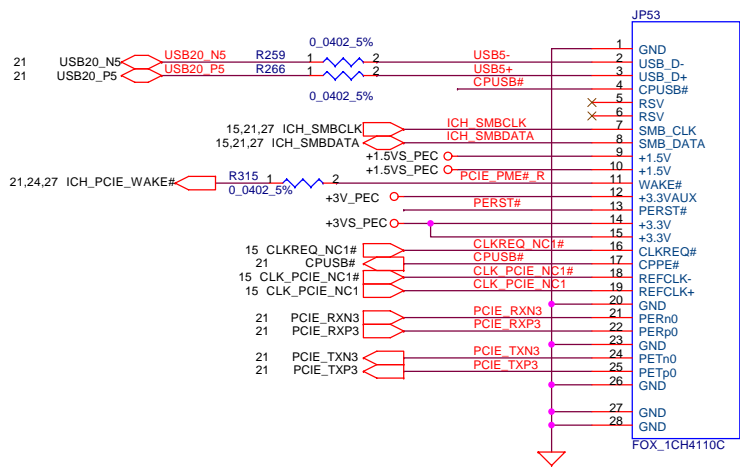
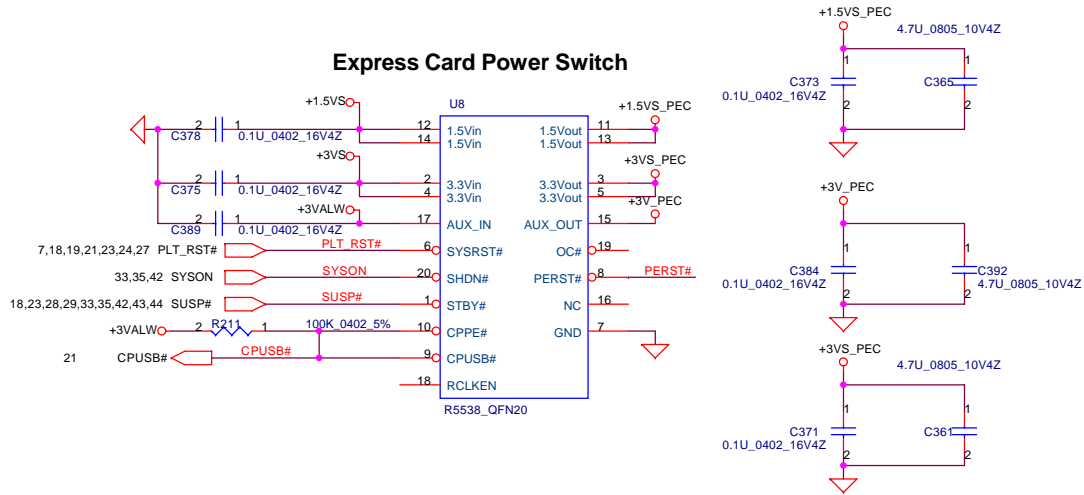


MDC CONN



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			Custom	IGT30 LA-3571P	0.1
			Date:	Monday, December 25, 2006	Sheet 25 of 47

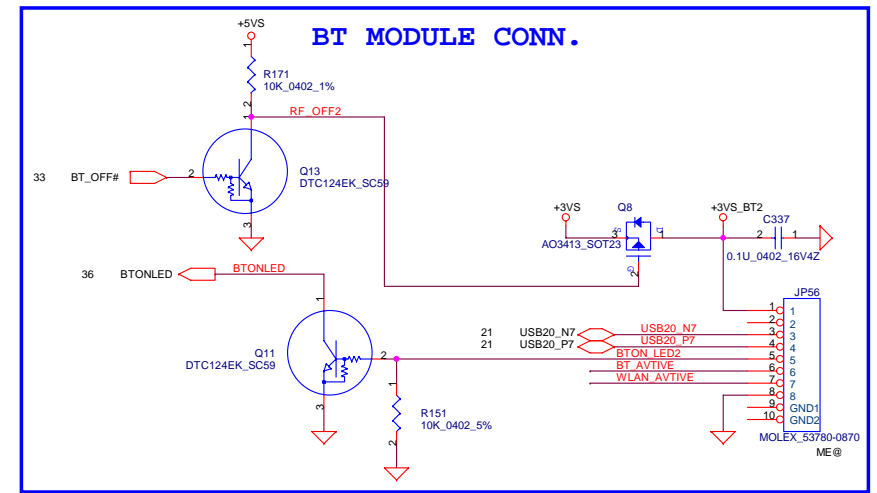
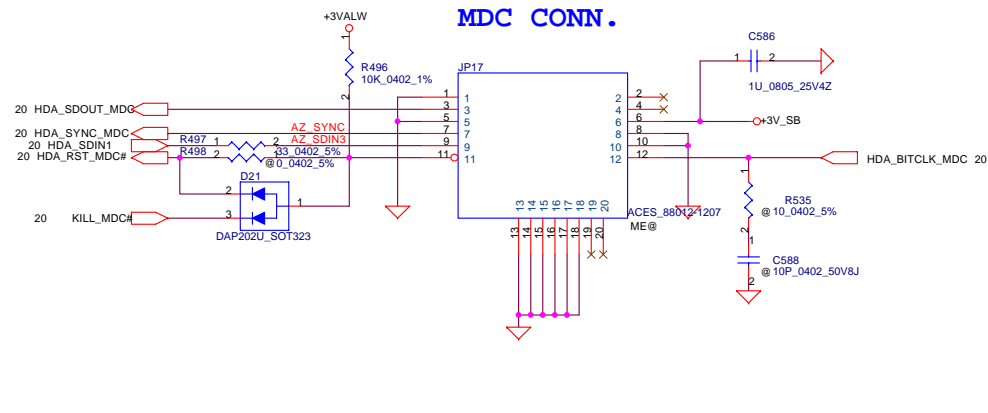
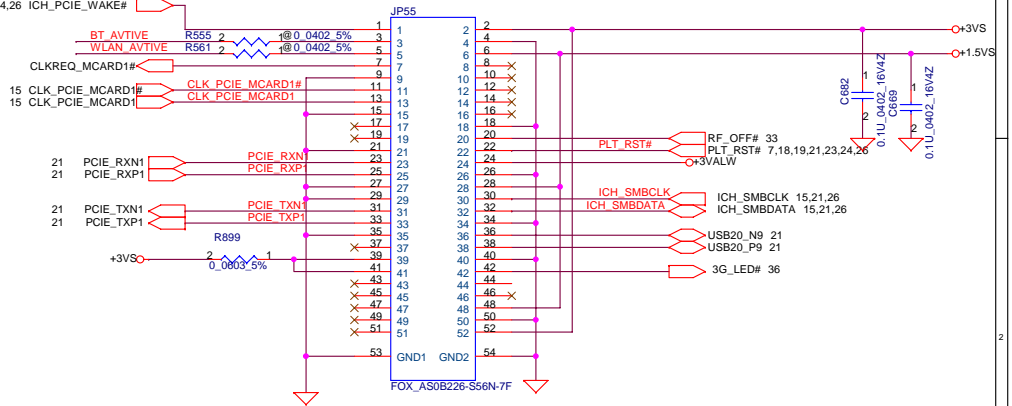
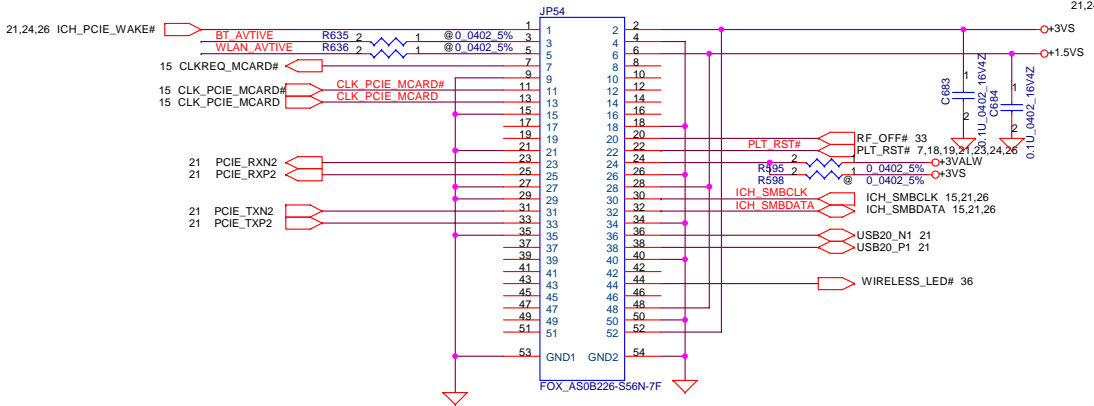
Express Card Power Switch



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Size	Custom	Document Number	IGT30 LA-3571P	Rev	0.1
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Mini-Express Card(Slot 1-WLAN)

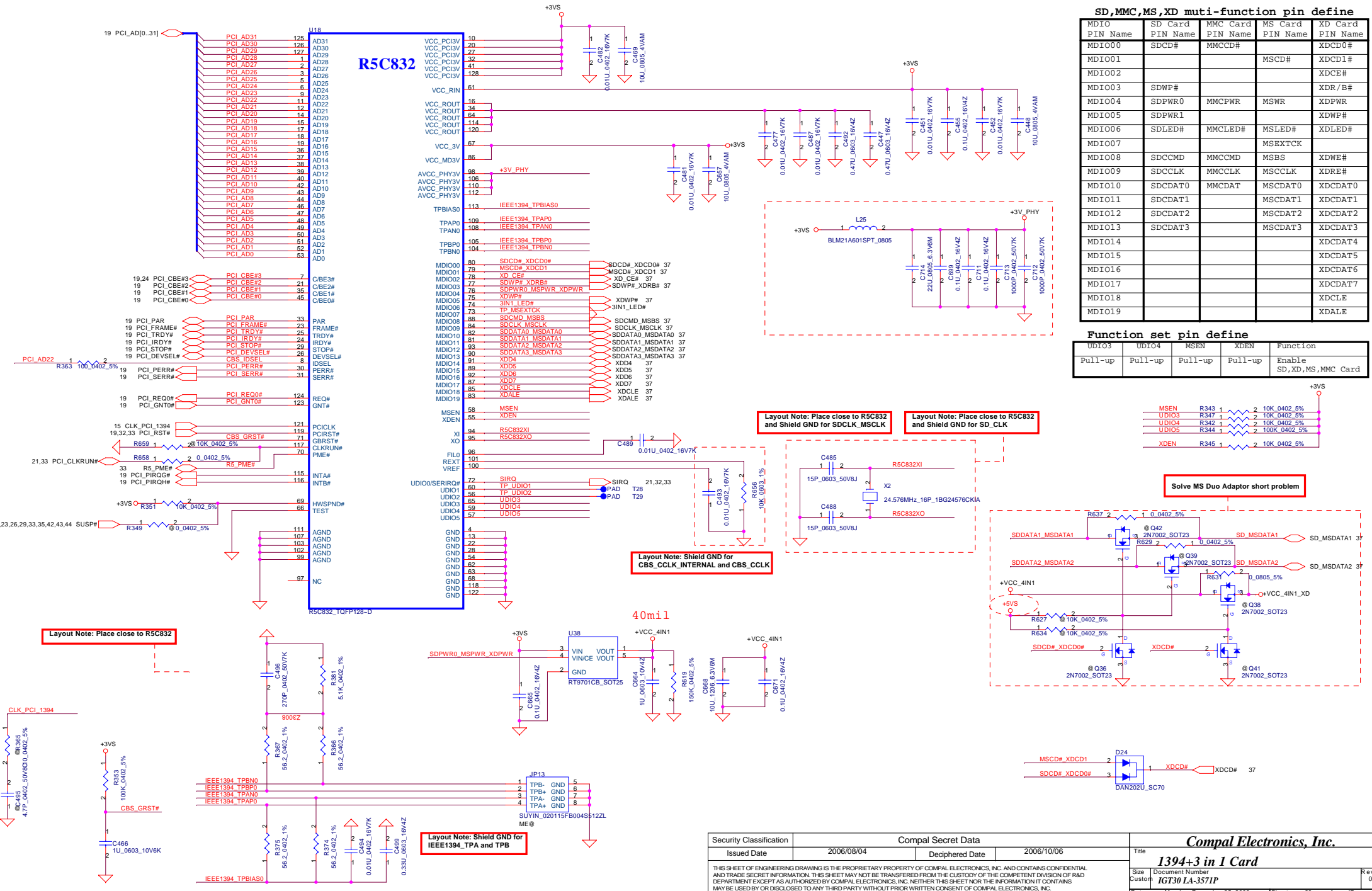
Mini-Express Card(Slot 2-3G)



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		2006/10/06

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Compal Electronics, Inc.	
Title	Mini Card / MDC CONN
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SD,MMC,MS,XD multi-function pin define

MDIO PIN Name	SD Card PIN Name	MMC Card PIN Name	MS Card PIN Name	XD Card PIN Name
MDIO00	SDCD#	MMCCD#		XDCD0#
MDIO01			MSCD#	XDCD1#
MDIO02				XDCE#
MDIO03	SDWP#			XDR/#
MDIO04	SDPWR0	MMC PWR	MSWR	XD PWR
MDIO05	SDPWR1			XDWP#
MDIO06	SDLED#	MMCLED#	MSLED#	XDLED#
MDIO07				MSEXTCK
MDIO08	SDCCMD	MMCCMD	MSBS	XDWE#
MDIO09	SDCLCK	MMCCLK	MSCCLK	XDRE#
MDIO10	SDCAT0	MMCDAT	MSCDAT0	XDCDAT0
MDIO11	SDCAT1		MSCDAT1	XDCDAT1
MDIO12	SDCAT2		MSCDAT2	XDCDAT2
MDIO13	SDCAT3		MSCDAT3	XDCDAT3
MDIO14				XDCDAT4
MDIO15				XDCDAT5
MDIO16				XDCDAT6
MDIO17				XDCDAT7
MDIO18				XDCLE
MDIO19				XDAL

Function set pin define

UDIO3	UDIO4	MSEN	XDEN	Function
Pull-up	Pull-up	Pull-up	Pull-up	Enable SD, XD, MS, MMC Card

Layout Note: Place close to R5C832 and Shield GND for SDCLK_MSCLK

Layout Note: Place close to R5C832 and Shield GND for SD_CLK

Layout Note: Shield GND for CBS_CCLK_INTERNAL and CBS_CCLK

Solve MS Duo Adaptor short problem

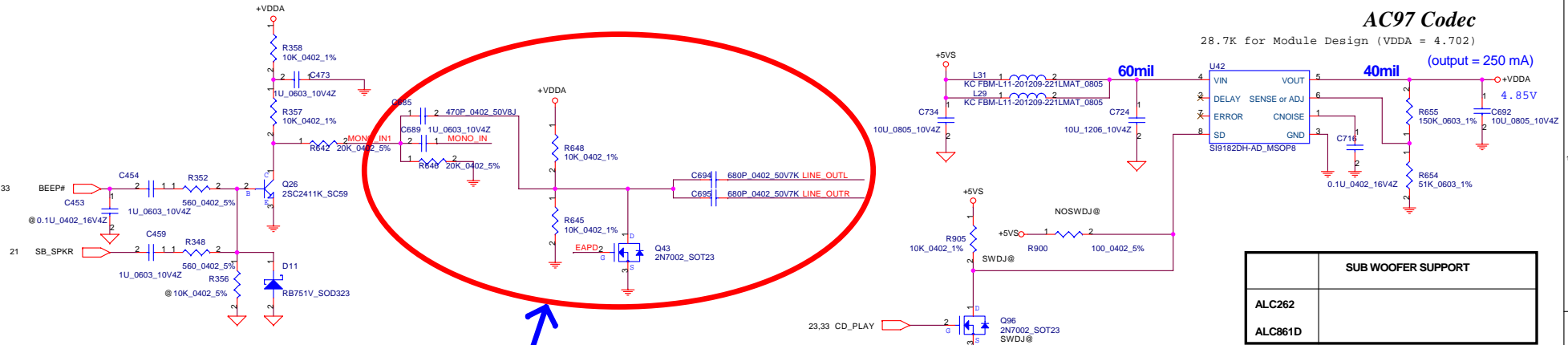
Layout Note: Place close to R5C832

Layout Note: Shield GND for IEEE1394_TPA and TPB

AC97 Codec

28.7K for Module Design (VDDA = 4.702)

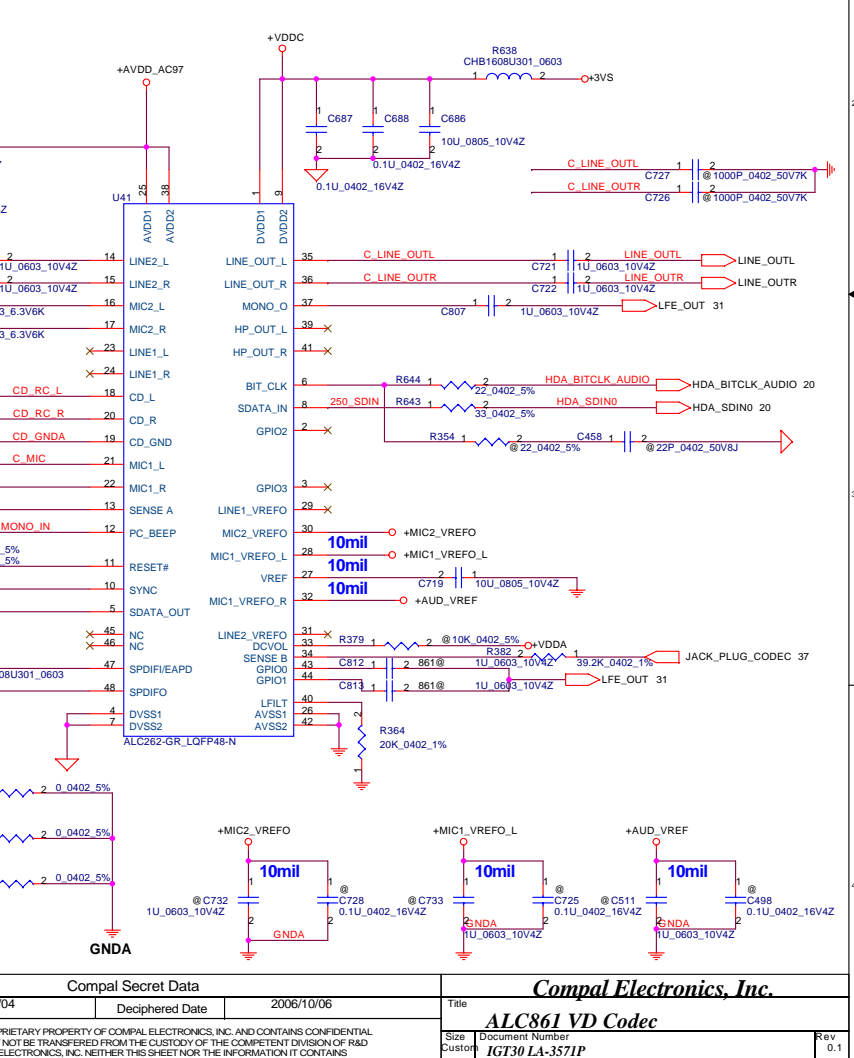
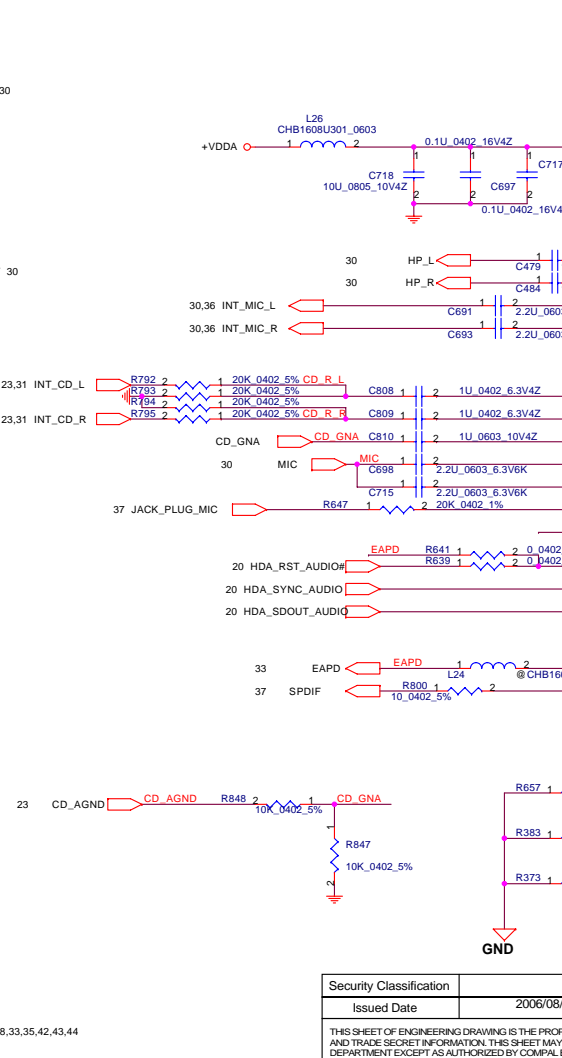
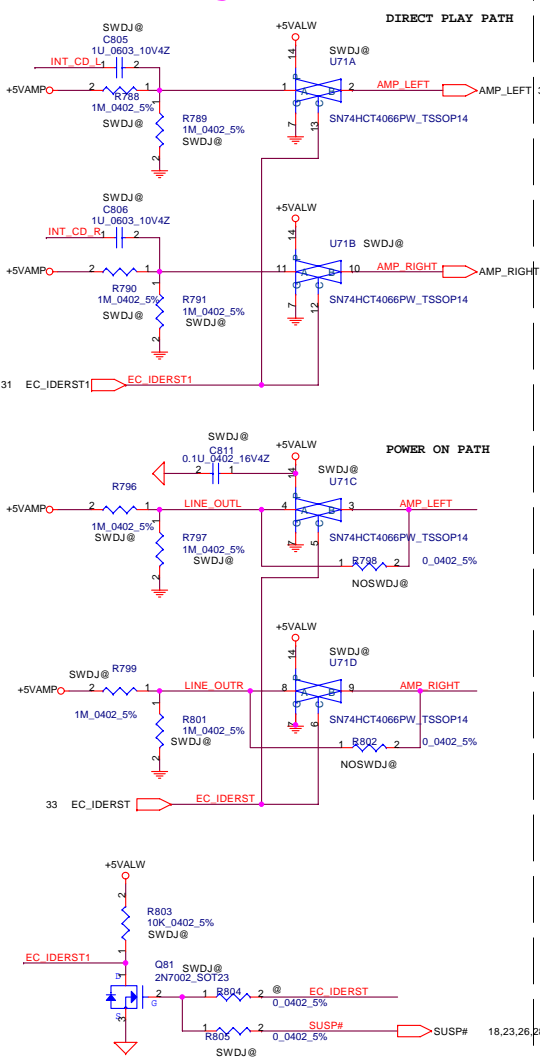
(output = 250 mA)



PC BEEP for DOS mode

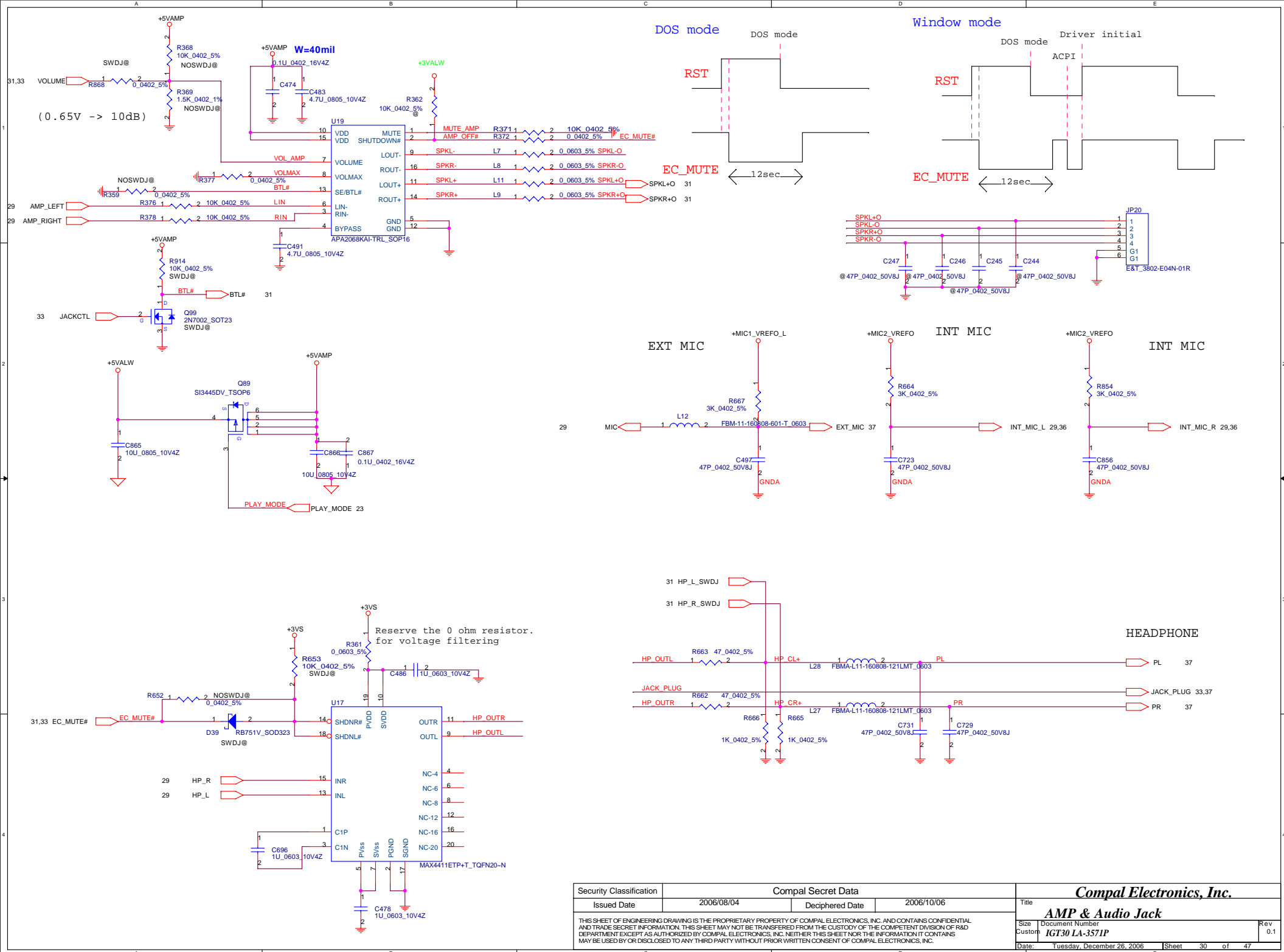
SUB WOOFER SUPPORT	
ALC262	
ALC861D	

SWDJ



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Issued Date	2006/08/04	Deciphered Date	2006/10/06
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Compal Electronics, Inc.	
Title	ALC861 VD Codec
Size	Document Number
Customer	IGT30 LA-3571P
Date	Monday, December 25, 2006
Sheet	29 of 47

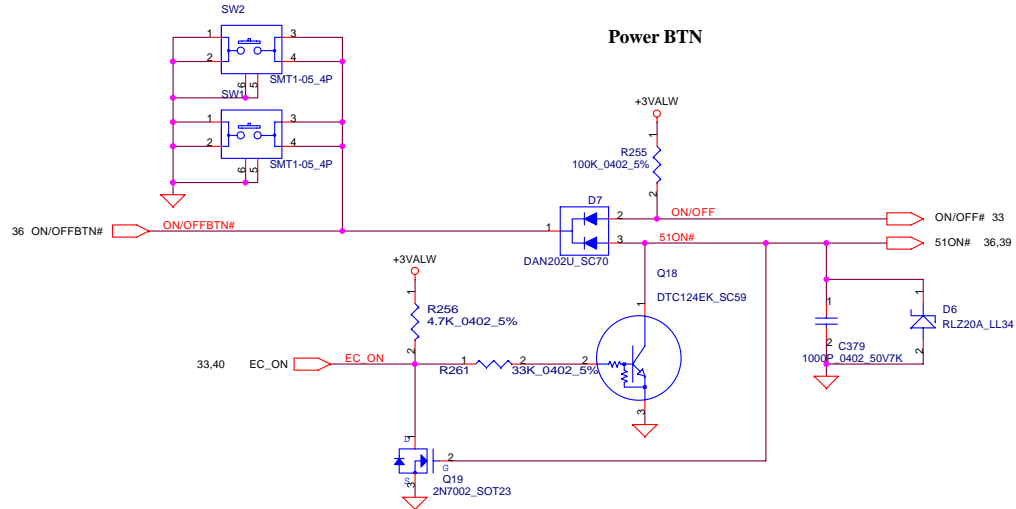
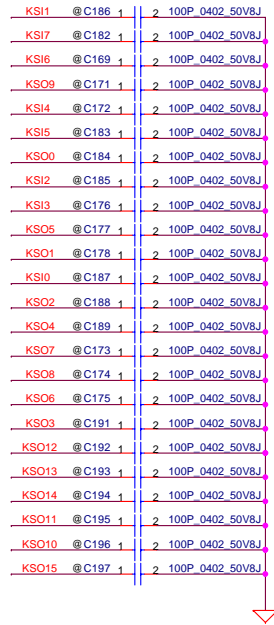
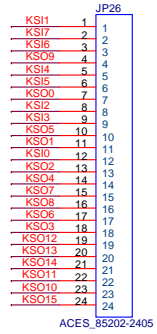
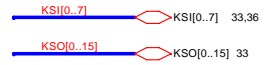


Security Classification	Compal Secret Data	
Issued Date	2006/08/04	Deciphered Date
		2006/10/06

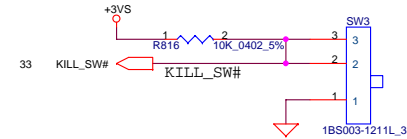
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Compal Electronics, Inc.		
Title	AMP & Audio Jack	
Size	Document Number	Rev
Custom	IGT30 LA-3571P	0.1
Date:	Tuesday, December 26, 2006	Sheet 30 of 47

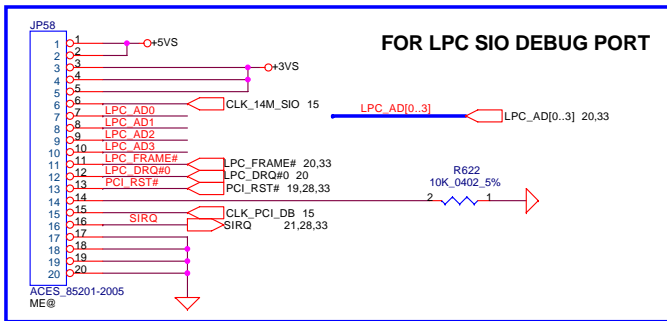
INT_KBD CONN.(TYPE "D" KB)



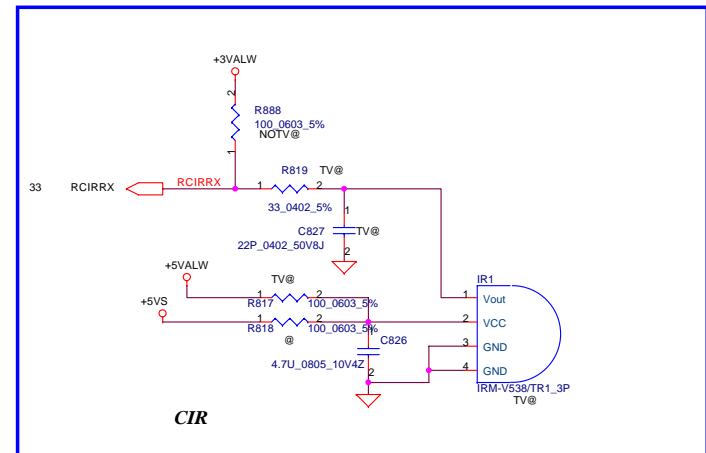
Kill Switch



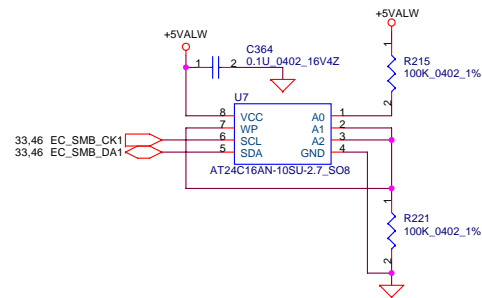
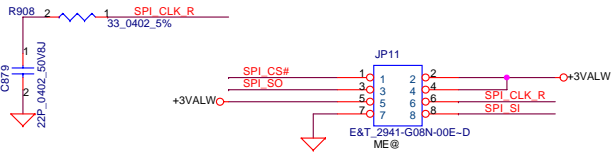
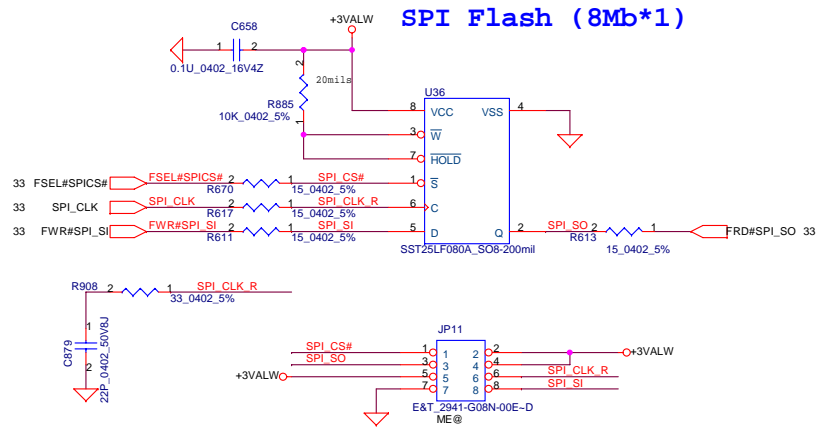
FOR LPC SIO DEBUG PORT



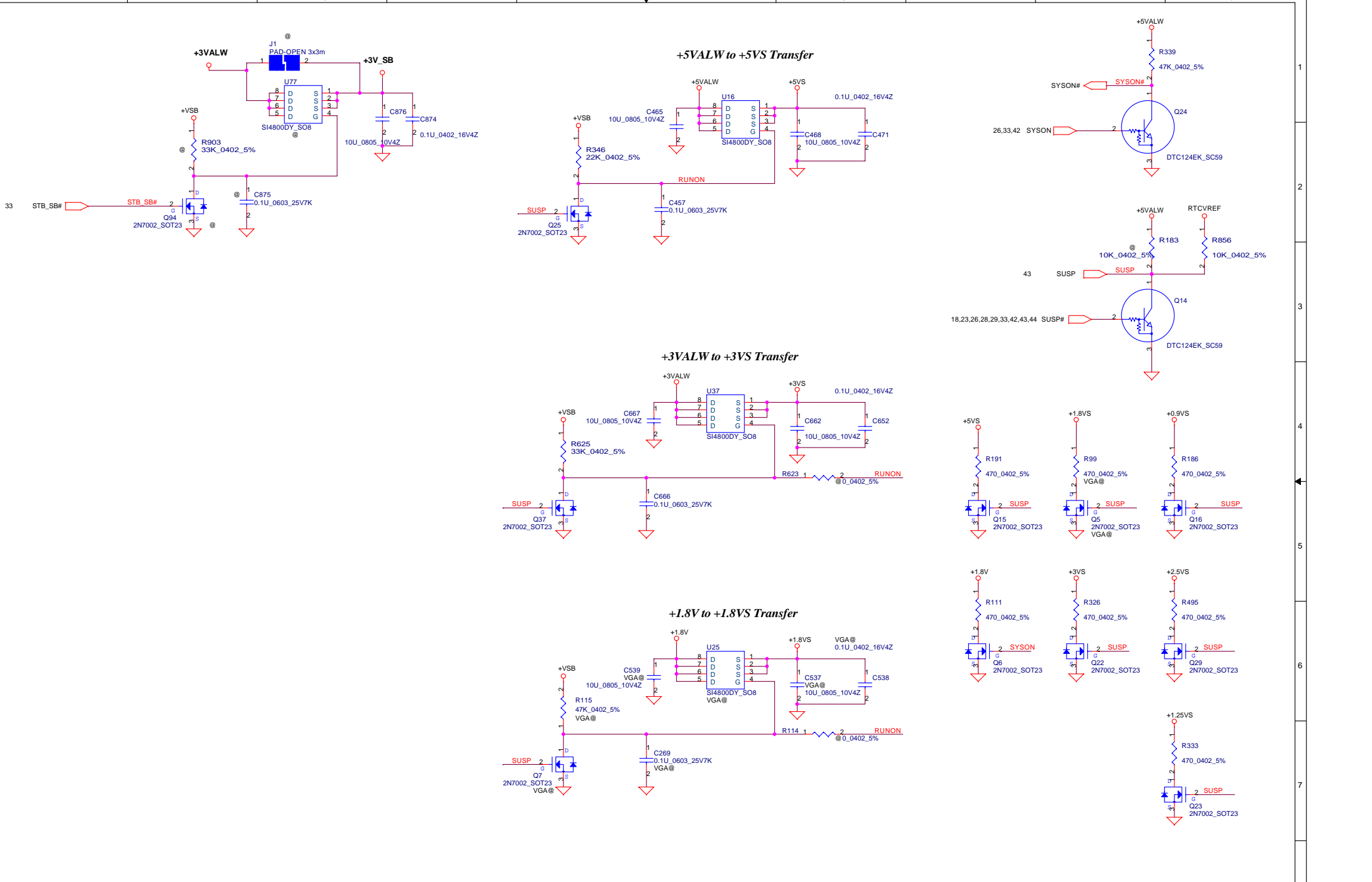
CIR



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Issued Date	2006/08/04	Deciphered Date	2006/10/06	KBD,ON/OFF,TP,LED/B,DEBUG
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Date:	Monday, December 25, 2006	Sheet	32	of 47

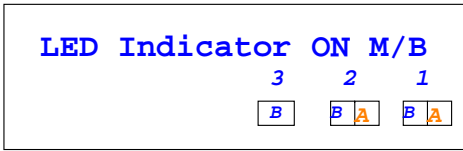


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				Custom	IGT30 LA-3S71P
Date:	Monday, December 25, 2006	Sheet	34	of	47

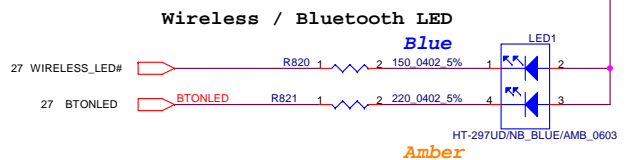


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Compal Electronics, Inc.		
Title	DC/DC Circuit	
Size	Document Number	Rev
Custom	IGT30 LA-3571P	0.1
Date:	Monday, December 25, 2006	Sheet 35 of 47

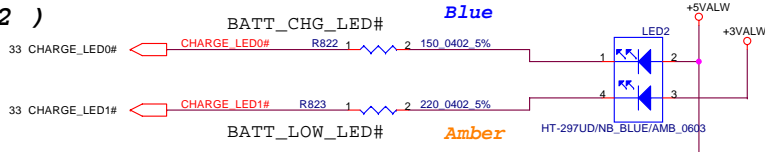


(1)

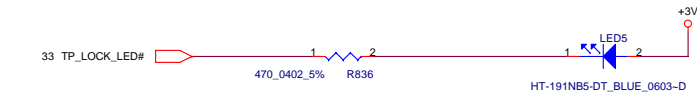
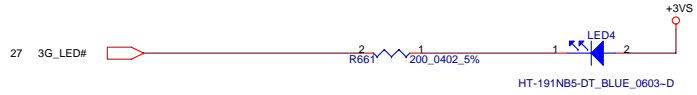
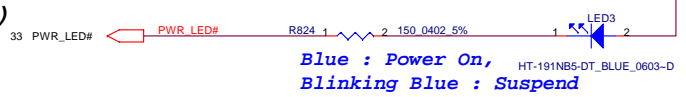


STATUS	
AC	BLUE
Chargin	Blinking Blue
Low BATT	Amber

(2)

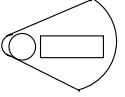


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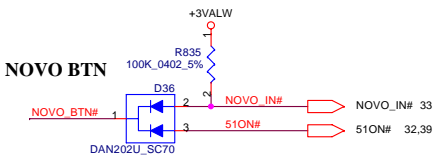
STATUS	
AC	BLUE
Chargin	Blinking Blue
Low BATT	Amber

Dial Wheel

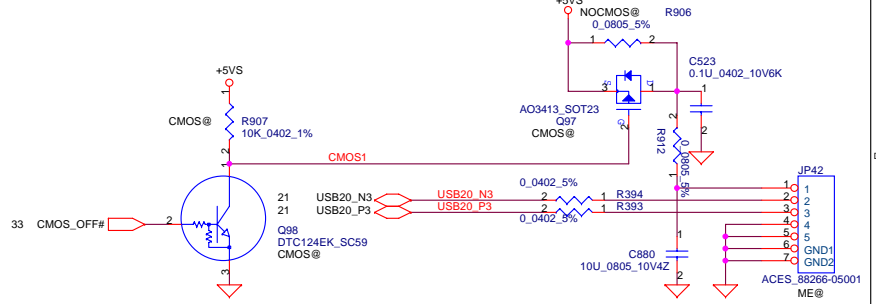


KEY Matrix	K016	K017
KS10	DW-UP	DW-DOWN
KS11	DW-ENTER	MUTE

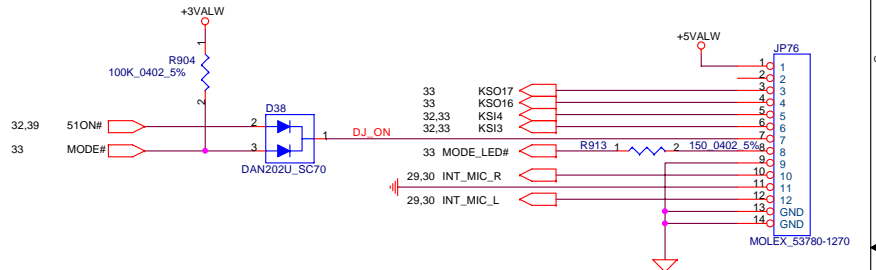
NOVA_BTN#



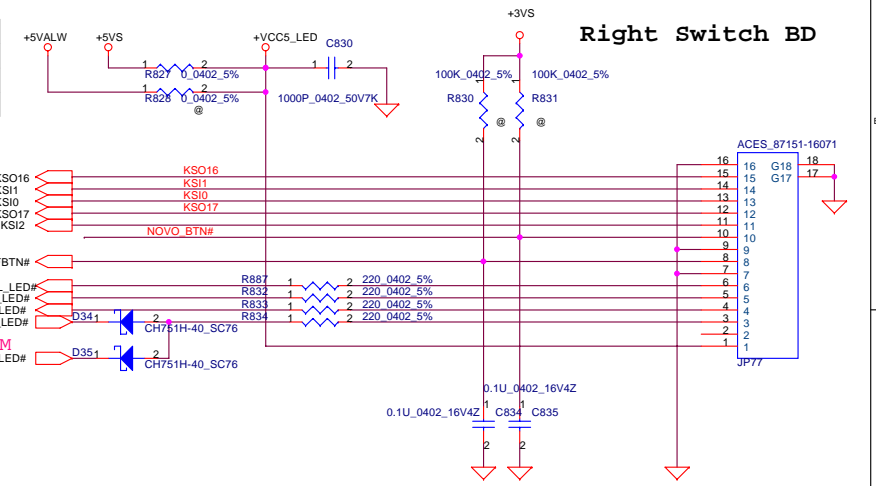
CMOS Camera Conn



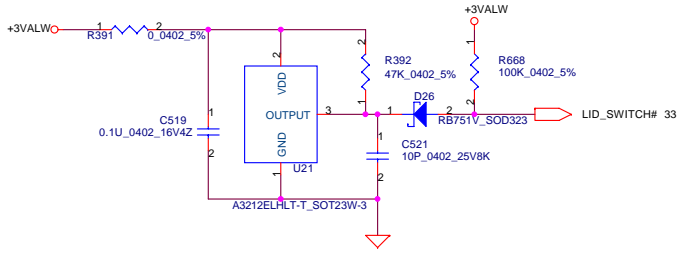
Left Switch BD(AUDIO DJ)



Right Switch BD



C839, C841, C842 For EMI Solution

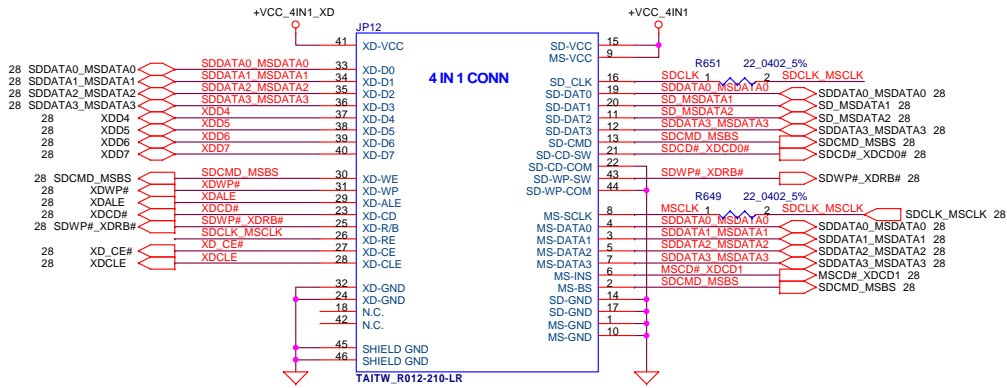


Security Classification	Compal Secret Data
Issued Date	2006/08/04
Deciphered Date	2006/10/06

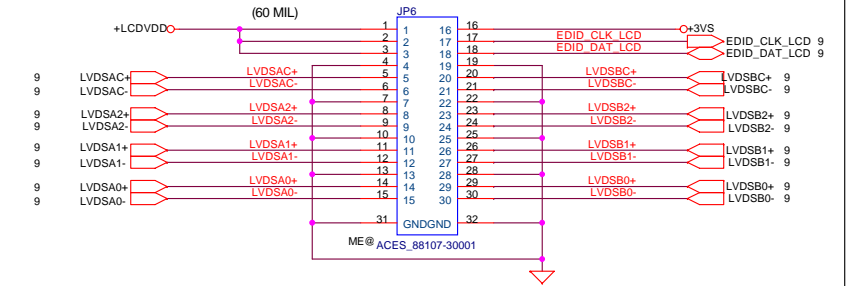
Title		INDICATE LED	
Size	Document Number	Rev	
Custom	IGT30 LA-3571P	0.1	

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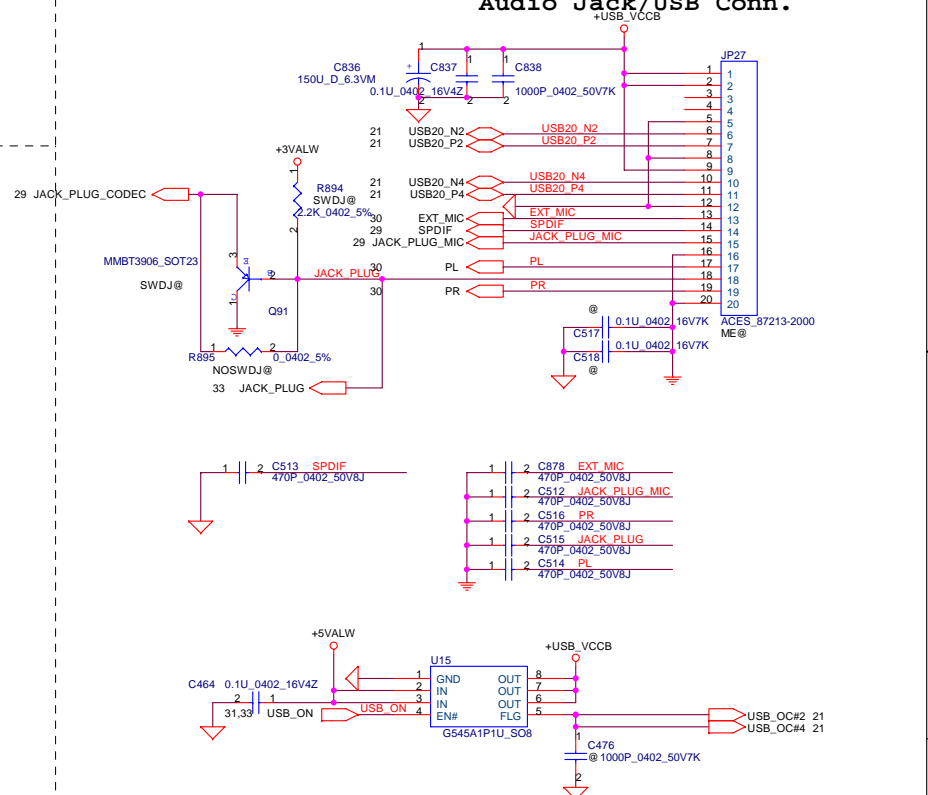
4 in 1 Card Reader



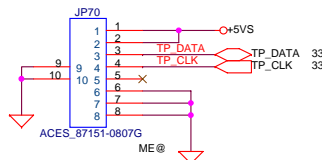
UMA LCD/PANEL Conn.



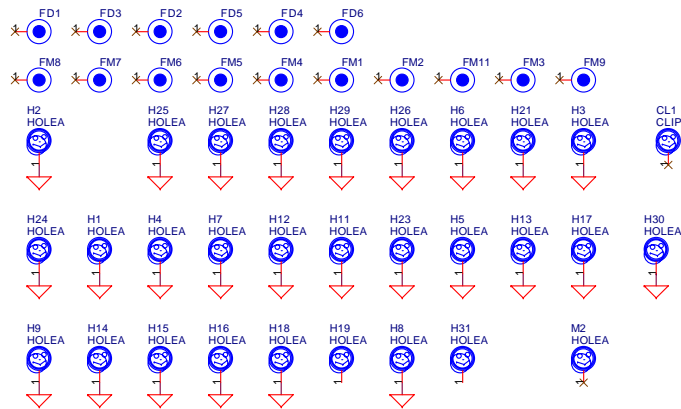
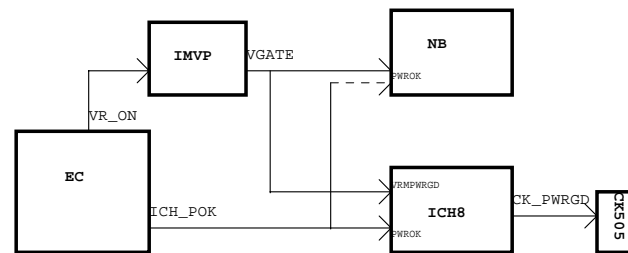
Audio Jack/USB Conn.



T/P Board



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				Custom	IGT30 LA-3571P
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				Sheet	37 of 47
				Rev	0.1



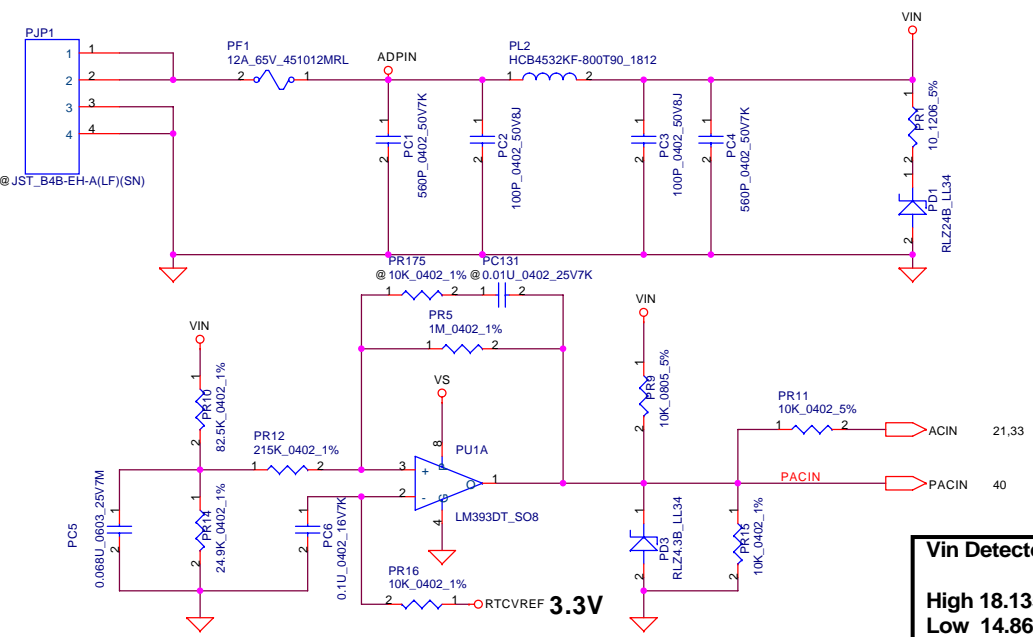
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ACIN

	Min.	typ.	Max.
H->L	13.843V	14.247V	14.636V
L->H	14.936V	15.381V	15.814V

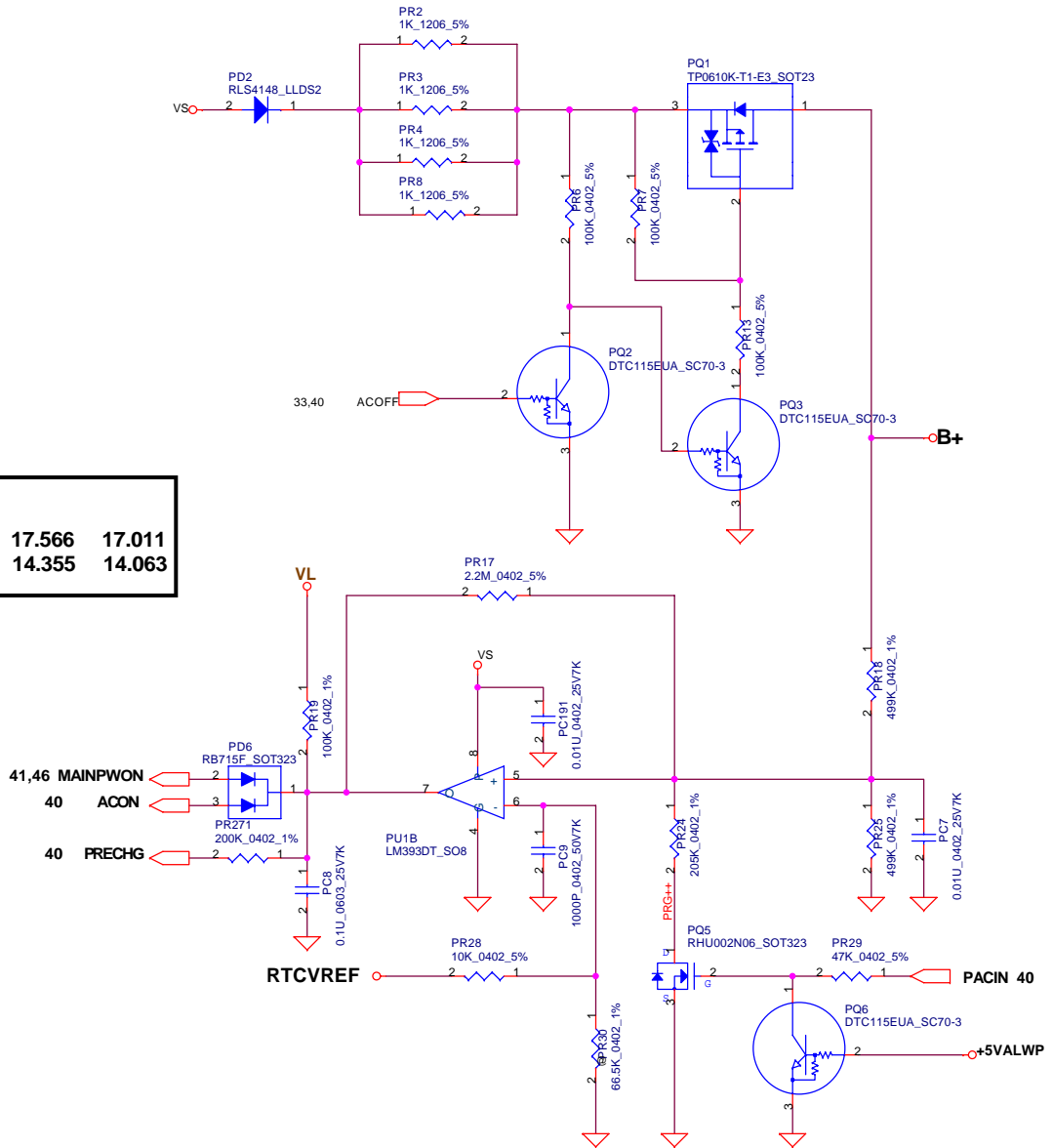
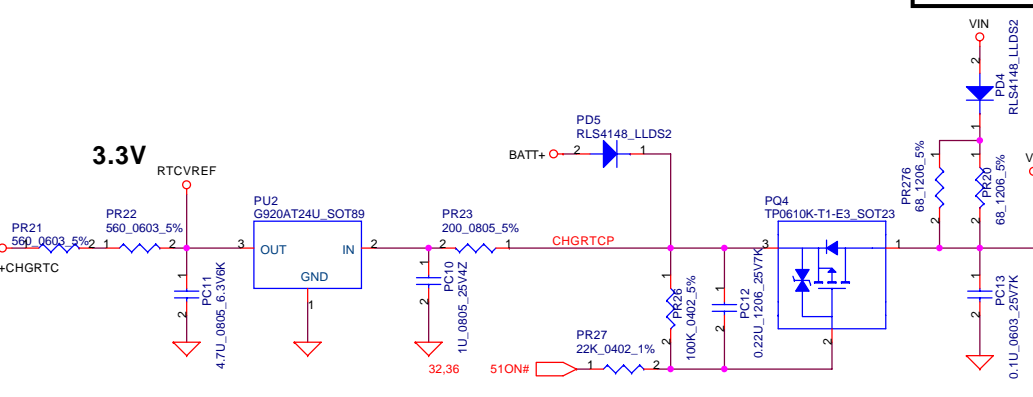
BATT ONLY

	Min.	typ.	Max.
H->L	6.138V	6.214V	6.359V
L->H	7.196V	7.349V	7.505V

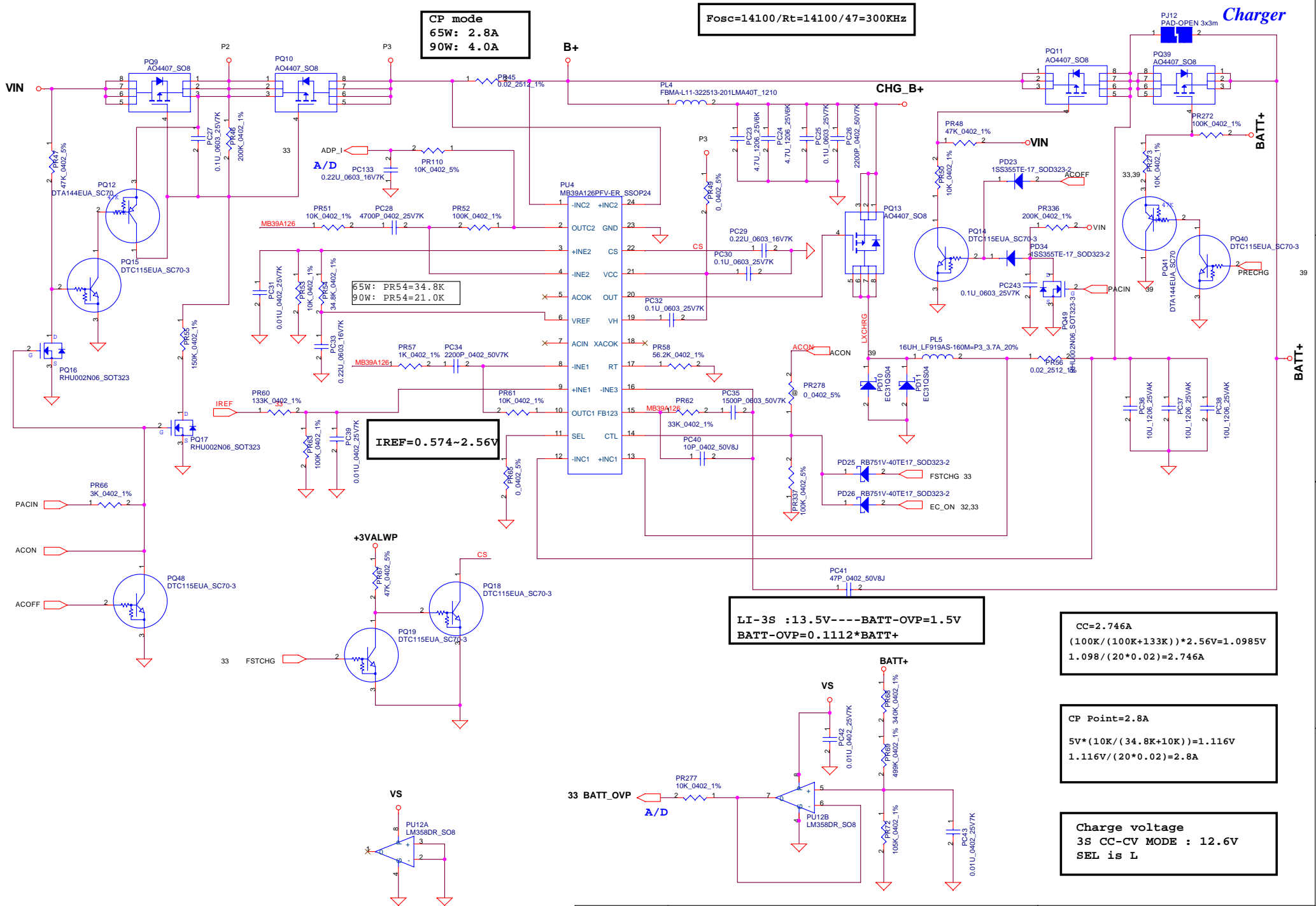


Vin Detector

	High	17.566	17.011
High	18.135	17.566	17.011
Low	14.866	14.355	14.063



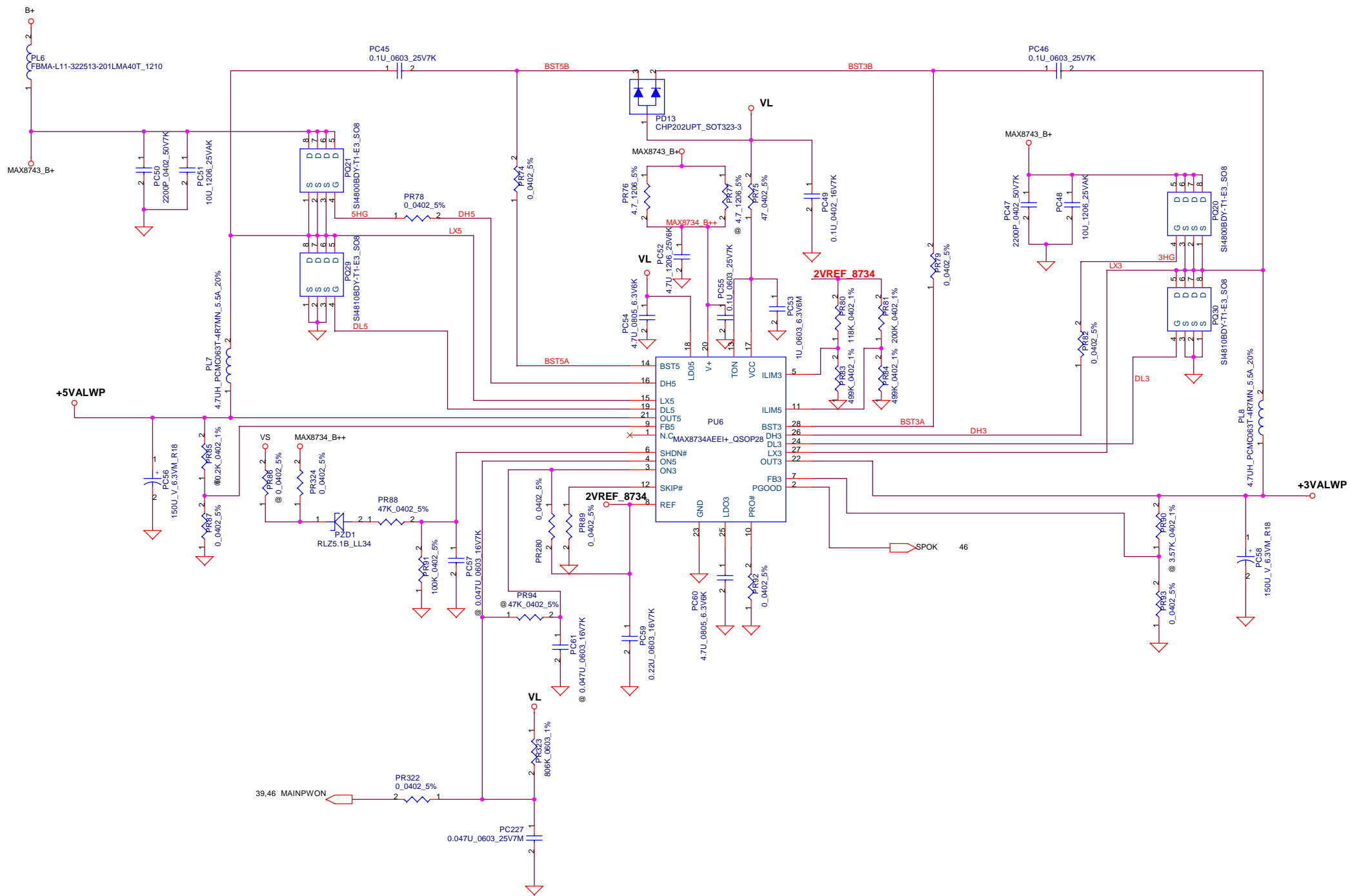
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Issued Date	2006/08/04	Deciphered Date	2006/10/06	Title	DCIN/DETECTOR
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Size	B	Document Number		Rev	0.1
Date:	Monday, December 25, 2006	Sheet	39	of	47



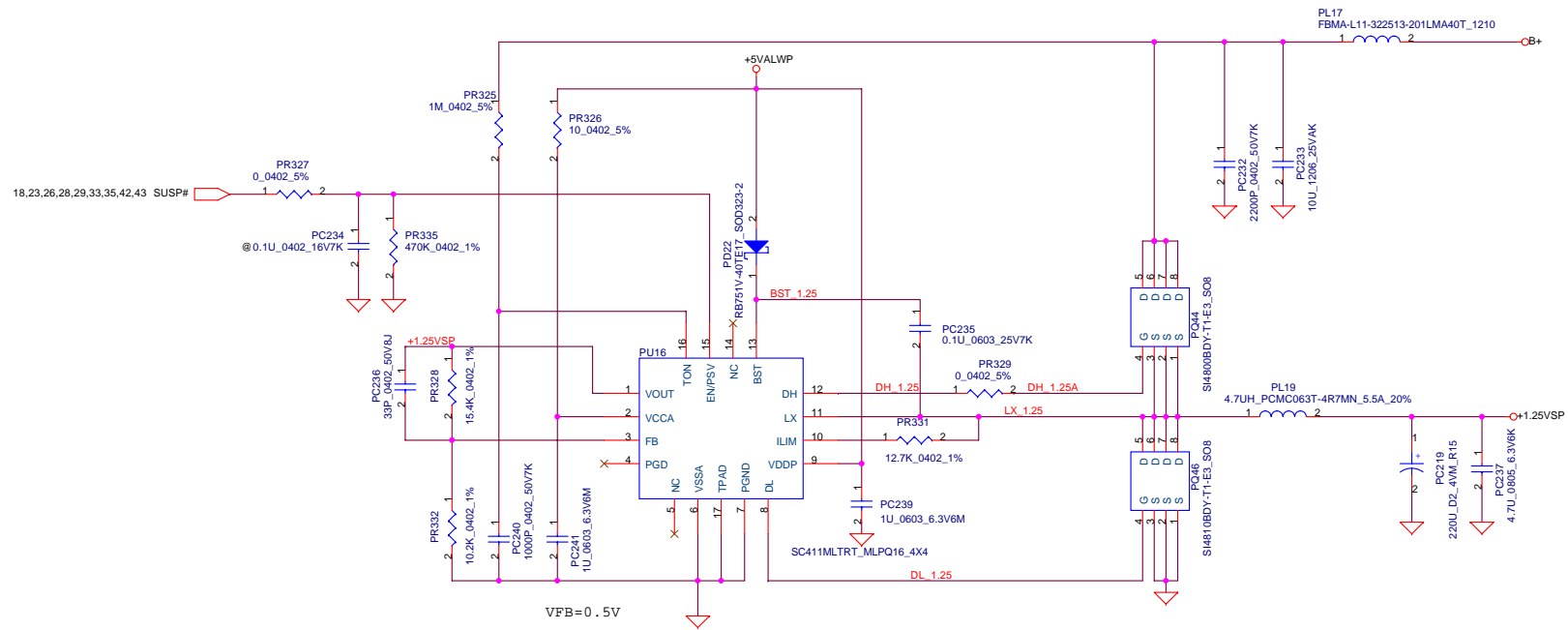
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Issued Date	2006/08/04	Deciphered Date
		2006/10/06

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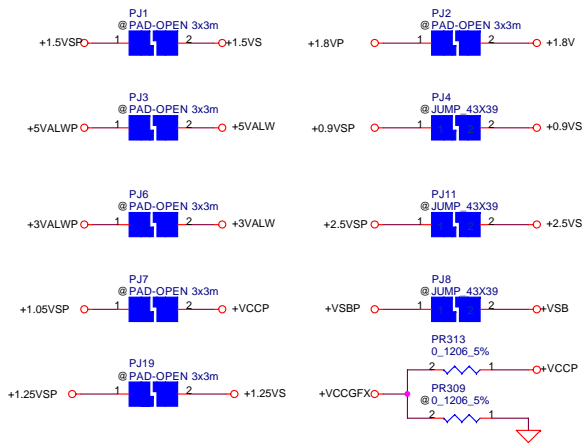
Compal Electronics, Inc.		
CHARGER		
Size	Document Number	Rev
B		0.1
Date:	Monday, December 25, 2006	Sheet 40 of 47



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				Custom	0.1
Date: Monday, December 25, 2006				Sheet	41 of 47

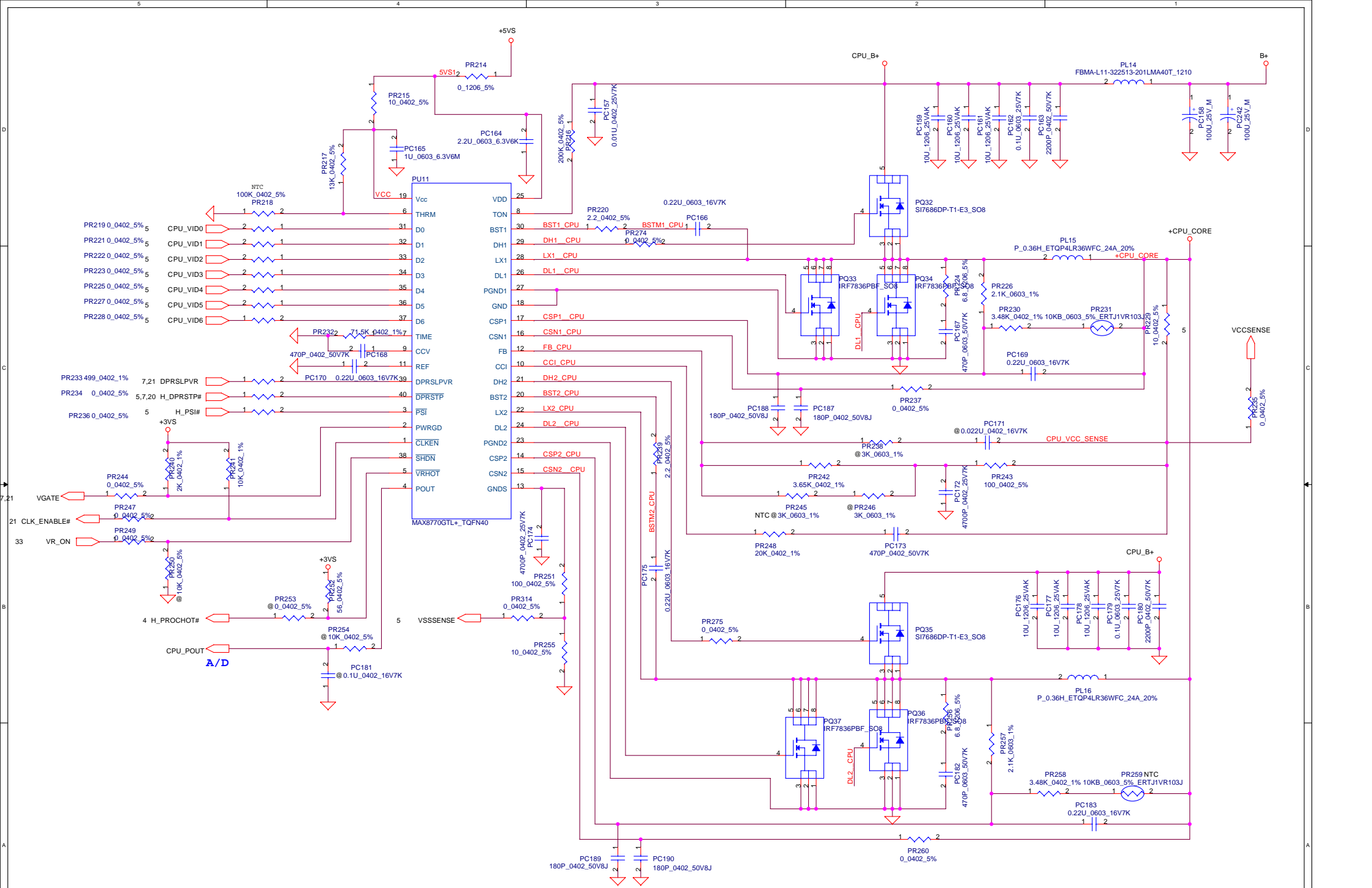


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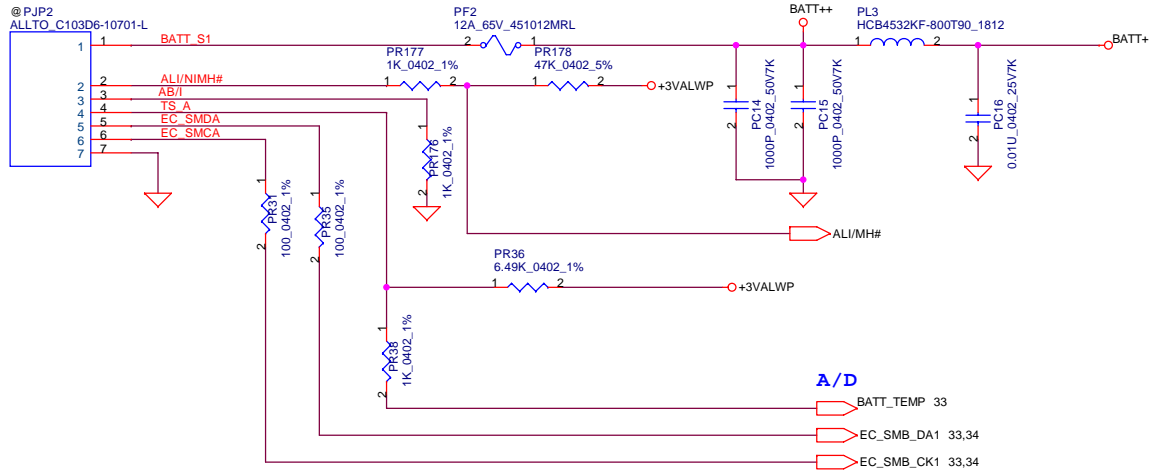
UMA Discrete PR313 PR309

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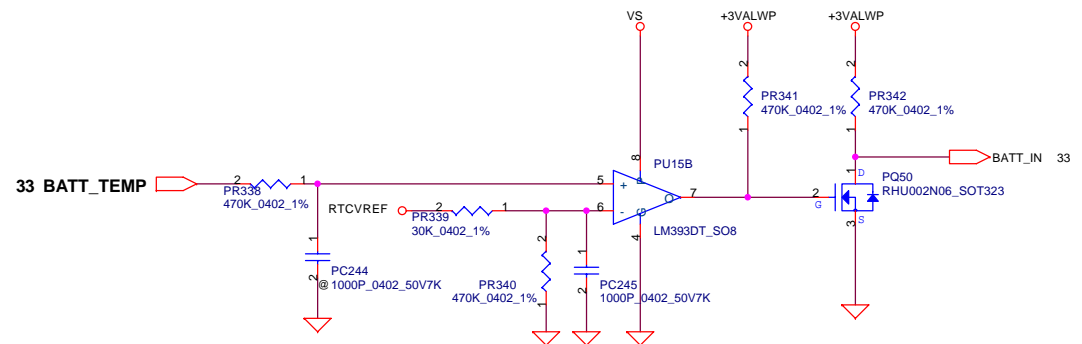
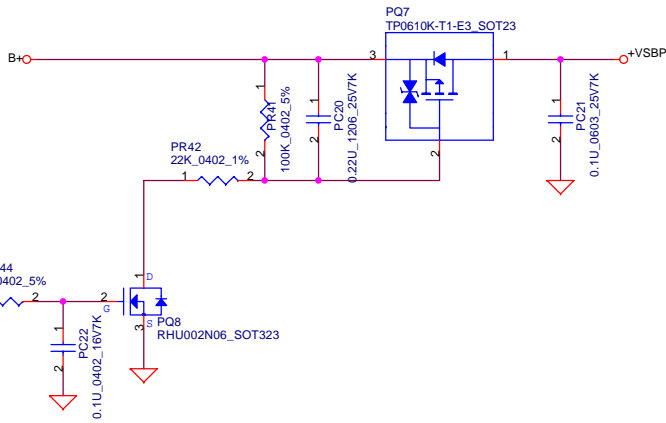
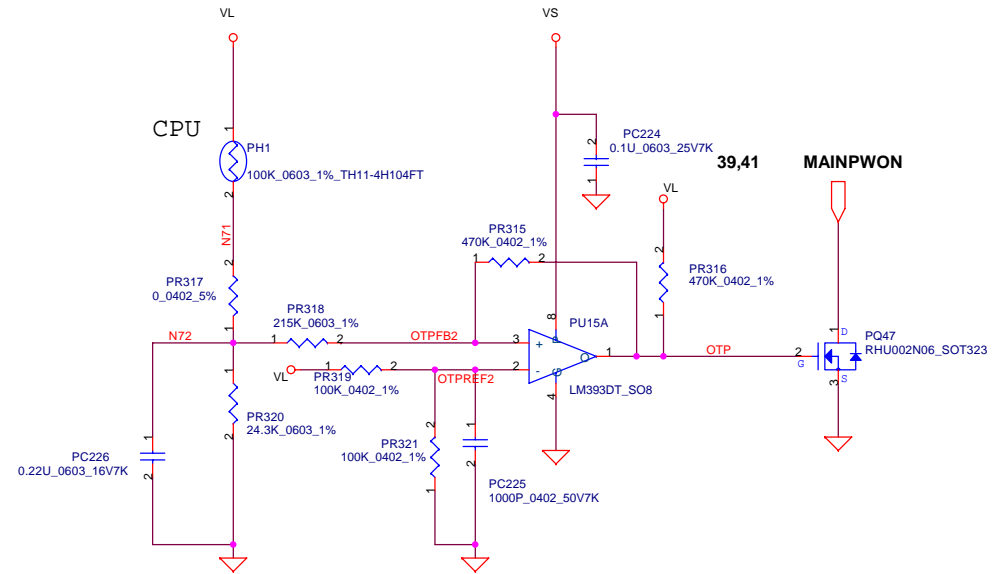


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Compal Electronics, Inc.		
+CPU_CORE		
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PH1 under CPU bottom side :
 CPU thermal protection at 84 degree C
 Recovery at 45 degree C



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Size	B	Document Number		Rev	0.1
Date:	Monday, December 25, 2006	Sheet	46	of	47

Version change list (P.I.R. List)

Item	Fixed Issue	Rev.	PG#	Modify List	B.Ver#	Phase
1	Improve CPU input capcaity noise issue		45	Advence CPU input capacity PC242		
2	Decrease S5 power consumption.		40	Delete PR59、PR64. ADD PD19、PD20.		
3	Protect battery discharge mos damage when plug 15V adapter.		45	Delete PD12. ADD PD21、PD22、PR250、PQ50、PC198..		
4	Improve 1.8v transient response.		42	Change PL10 to 2.2u, PR98 to 30k_0402_1%		
5	Adjust power sequence.		42	For adjust +1.8VSP, Change PR179 to 33k_0402_1% and add PC132 1u_0402_6.3v		
			43	For adjust +1.5VSP, Change PR283 to 3k_0402_1% and add PC194 1u_0402_6.3v For adjust +2.5VSP, Change PR121 to 2.2k_0402_1% and add PC100 1u_0402_6.3v For adjust +0.9VSP, Change PR123 to 10k_0402_1% and add PC103 1u_0402_6.3v		
6	For improve EPA		46	Add PR338, PR339, PR340, PR341, PR342, PC244, PC245, PQ50		

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