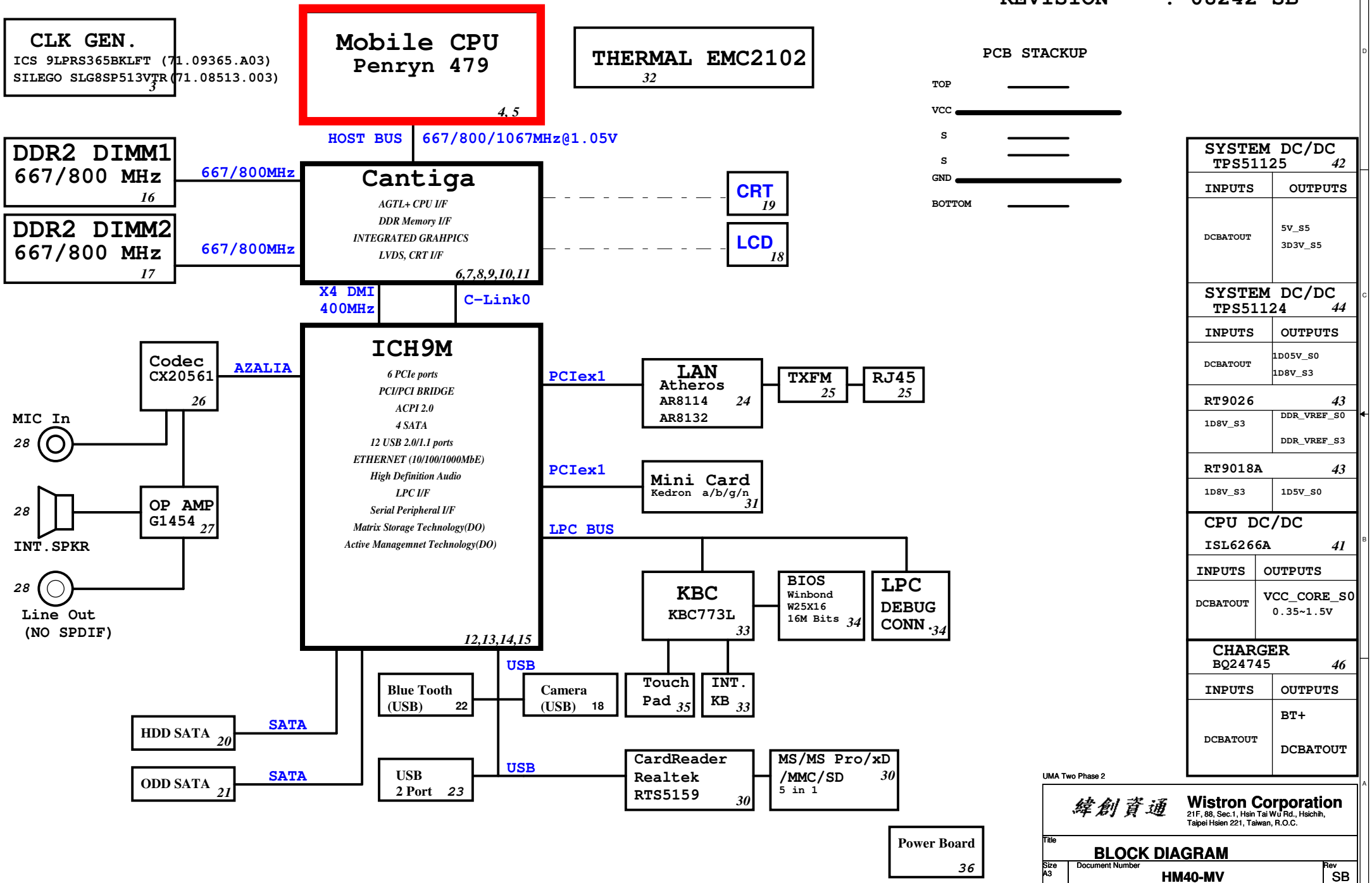
HM40-MV Block Diagram

Project code: 91.4BW01.001
PCB P/N : 48.4BW01.0SB
REVISION : 08242-SB



PCB STACKUP

SYSTEM DC/DC TPS51125 *42*

INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5

SYSTEM DC/DC TPS51124 *44*

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3

RT9026 *43*

1D8V_S3	DDR_VREF_S0 DDR_VREF_S3

RT9018A *43*

1D8V_S3	1D5V_S0

CPU DC/DC ISL6266A *41*

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0.35~1.5V

CHARGER BQ24745 *46*

INPUTS	OUTPUTS
DCBATOUT	BT+ DCBATOUT

UMA Two Phase 2

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Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM
Size: A3 | Document Number: HM40-MV | Rev: SB
Date: Monday, November 24, 2008 | Sheet 1 of 51

ICH9M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4** (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) **1=The iTPM Host Interface is disalbed(default)**
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1= Disabled (default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) **11 = Disabled (default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation(Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	**0 =No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

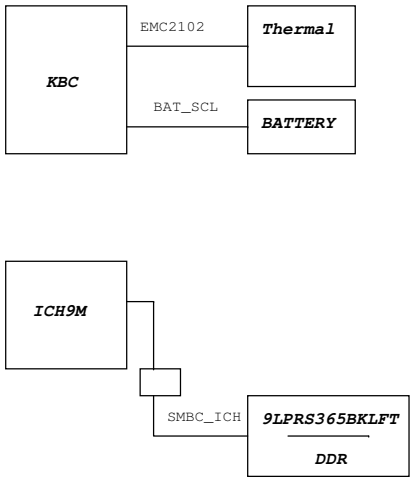
PCIE Routing

LANE1	LAN Atheros AR8114A
LANE2	MiniCard WLAN
LANE3	NC
LANE4	NC
LANE5	NC
LANE6	NC

USB Table

USB	
Pair	Device
0	USB1
1	NC
2	NC
3	MINIC1
4	WEBCAM
5	NC
6	NC
7	Bluetooth
8	NC
9	USB2(High speed)
10	NC
11	CardReader

SMBus



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Title: Reference

Size: A3 | Document Number: HM40-MV | Rev: SB

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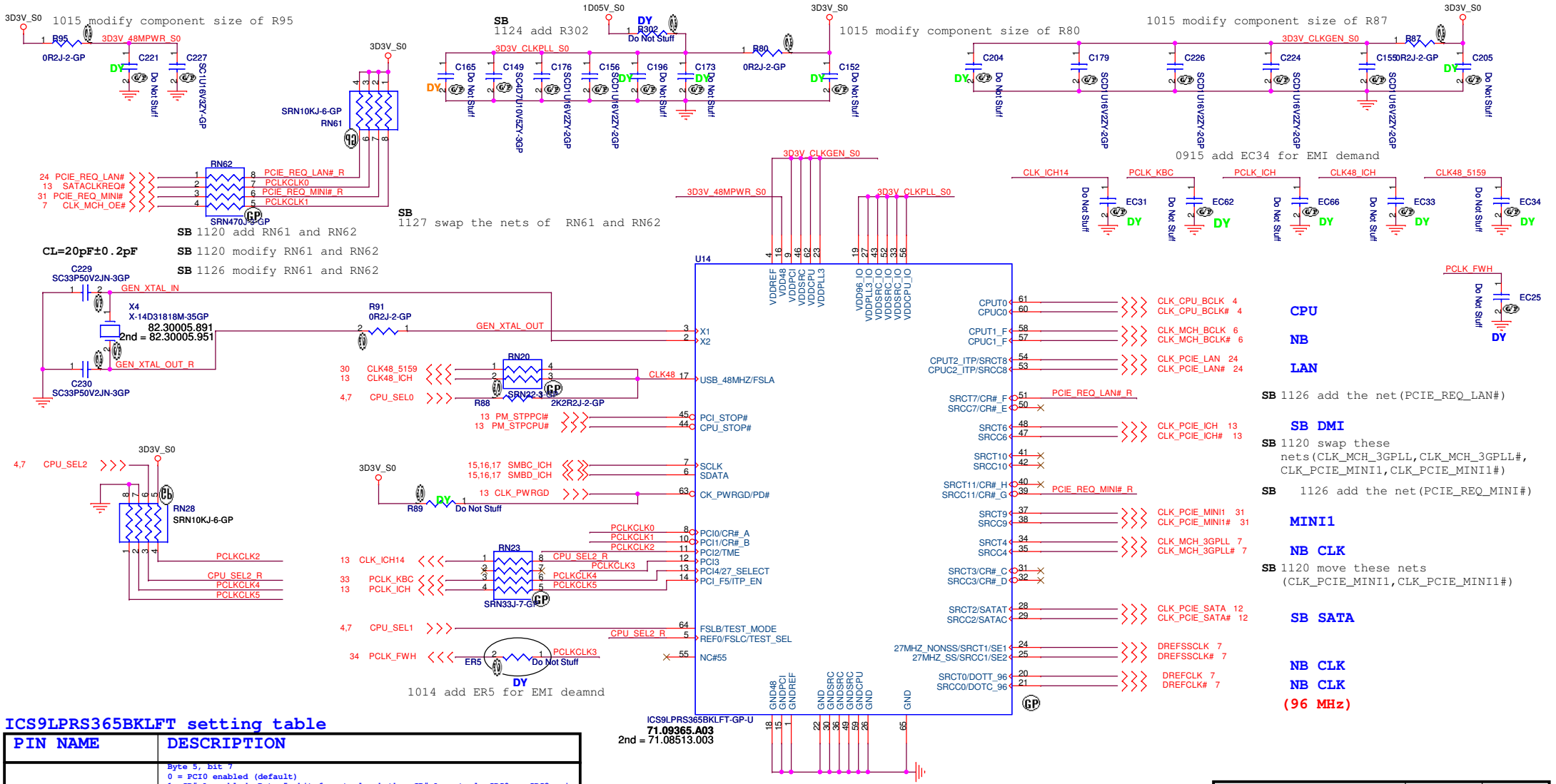

ICS9LPRS365BKLFT setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	3.3V PCI clock output
PCI4/27M_SEL	0 = Pin24 as SRC-1, Pin25 as SRC-1#, Pin20 as DOT96, Pin21 as DOT96# 1 = Pin24 as 27MHz, Pin25 as 27MHz_SS, Pin20 as SRC-0, Pin21 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1= CR#_C controls SRC2 pair

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1= CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7# enabled (default) 1= CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1= CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1= CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1= CR#_H controls SRC10

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1066M

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Title: Clock Generator

Size	Document Number	Rev
	HM40-MV	SB

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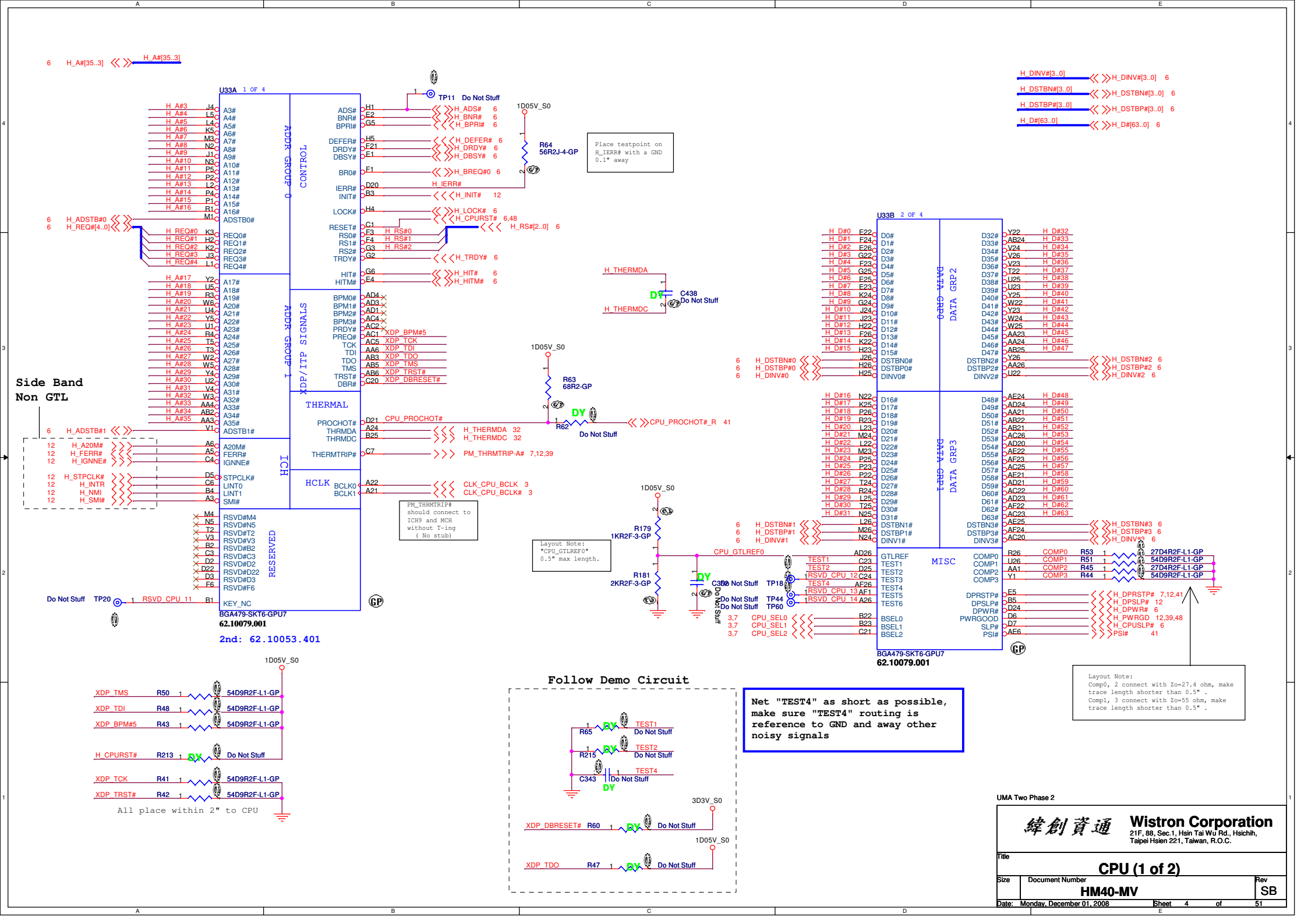
Side Band
Non GTL
U33A 1 OF 4
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERMAL
HCLK
RESERVED
BGA479-SKT6-GPU7
62.10079.001
2nd: 62.10053.401
U33B 2 OF 4
DATA GRP2
DATA GRP0
DATA GRP3
DATA GRP1
MISC
BGA479-SKT6-GPU7
62.10079.001
TP11 Do Not Stuff
TP20 Do Not Stuff
R64 56R2J-4-GP
R63 68R2-GP
R62 Do Not Stuff
C438 Do Not Stuff
R179 1KR2F-3-GP
R181 2KR2F-3-GP
C356 Do Not Stuff
TP18 Do Not Stuff
TP44 Do Not Stuff
TP60 Do Not Stuff
Place testpoint on H_IERR# with a GND 0.1" away
PM_THRMTRIP# should connect to ICH9 and MCH without T-ing (No stub)
Layout Note: "CPU_GTLREF0" 0.5" max length.
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" . Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
Follow Demo Circuit
Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals
All place within 2" to CPU
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Title
CPU (1 of 2)
Size
Document Number
HM40-MV
Rev
SB
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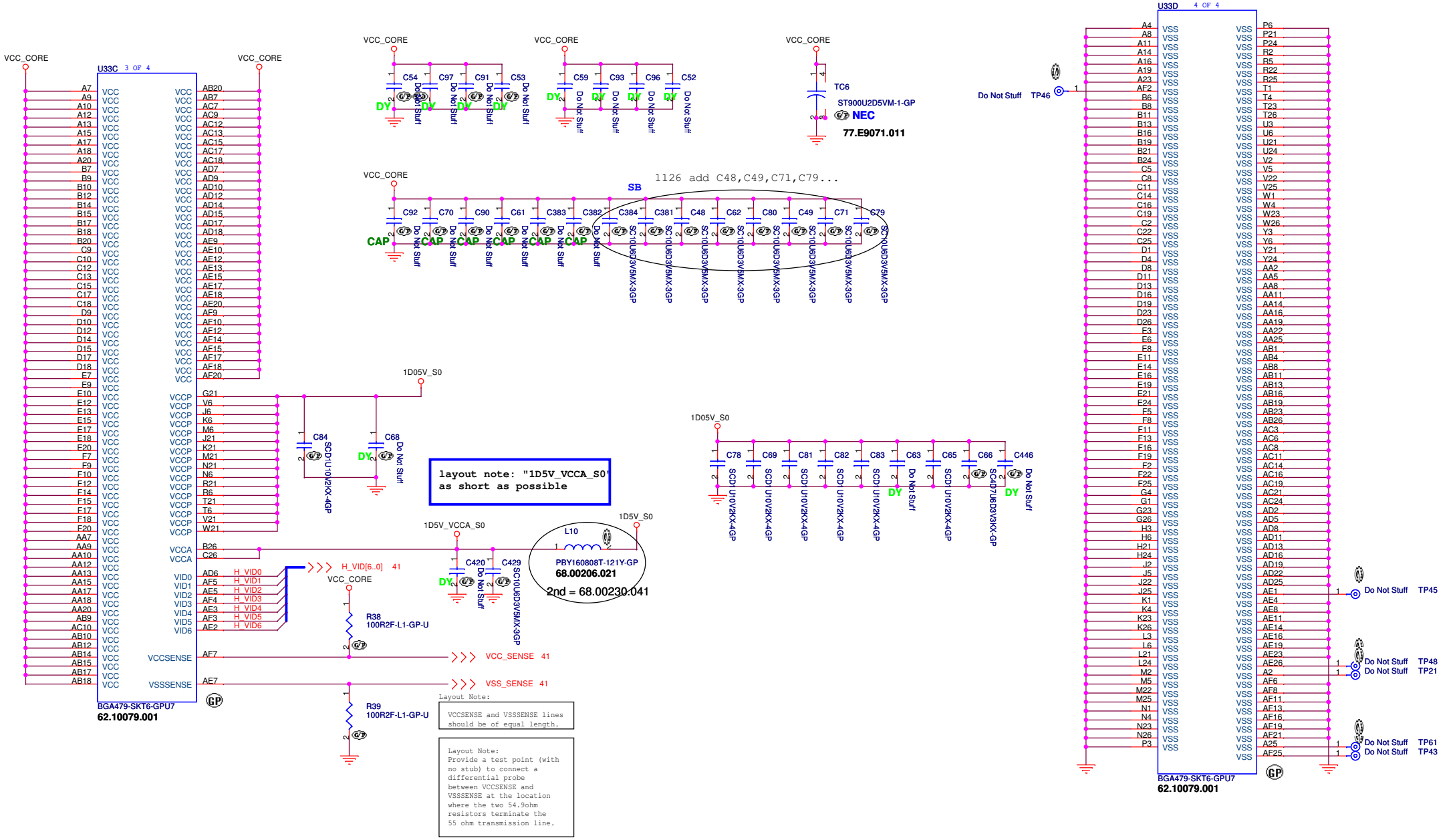

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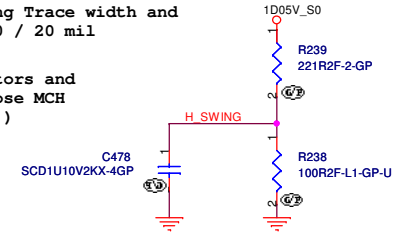
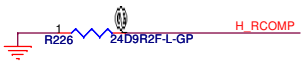
Title	**CPU (2 of 2)**	
Size	Document Number **HM40-MV**	Rev SB
Date: Monday, December 01, 2008	Sheet 5 of 51	

H_SWING routing Trace width and Spacing use 10 / 20 mil

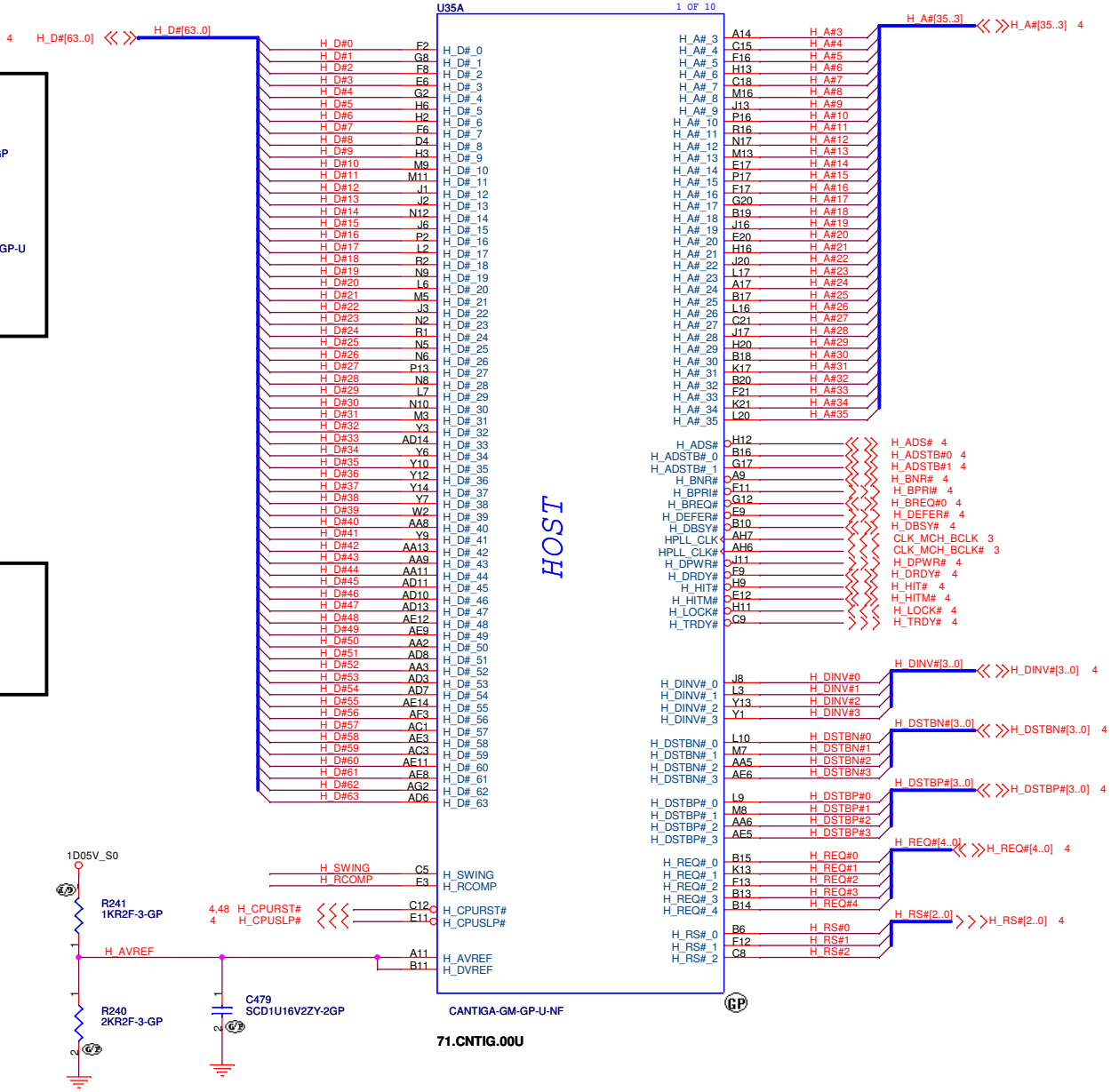
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")



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Title: Cantiga (1 of 6)_HOST

Size | Document Number: HM40-MV | Rev: SB

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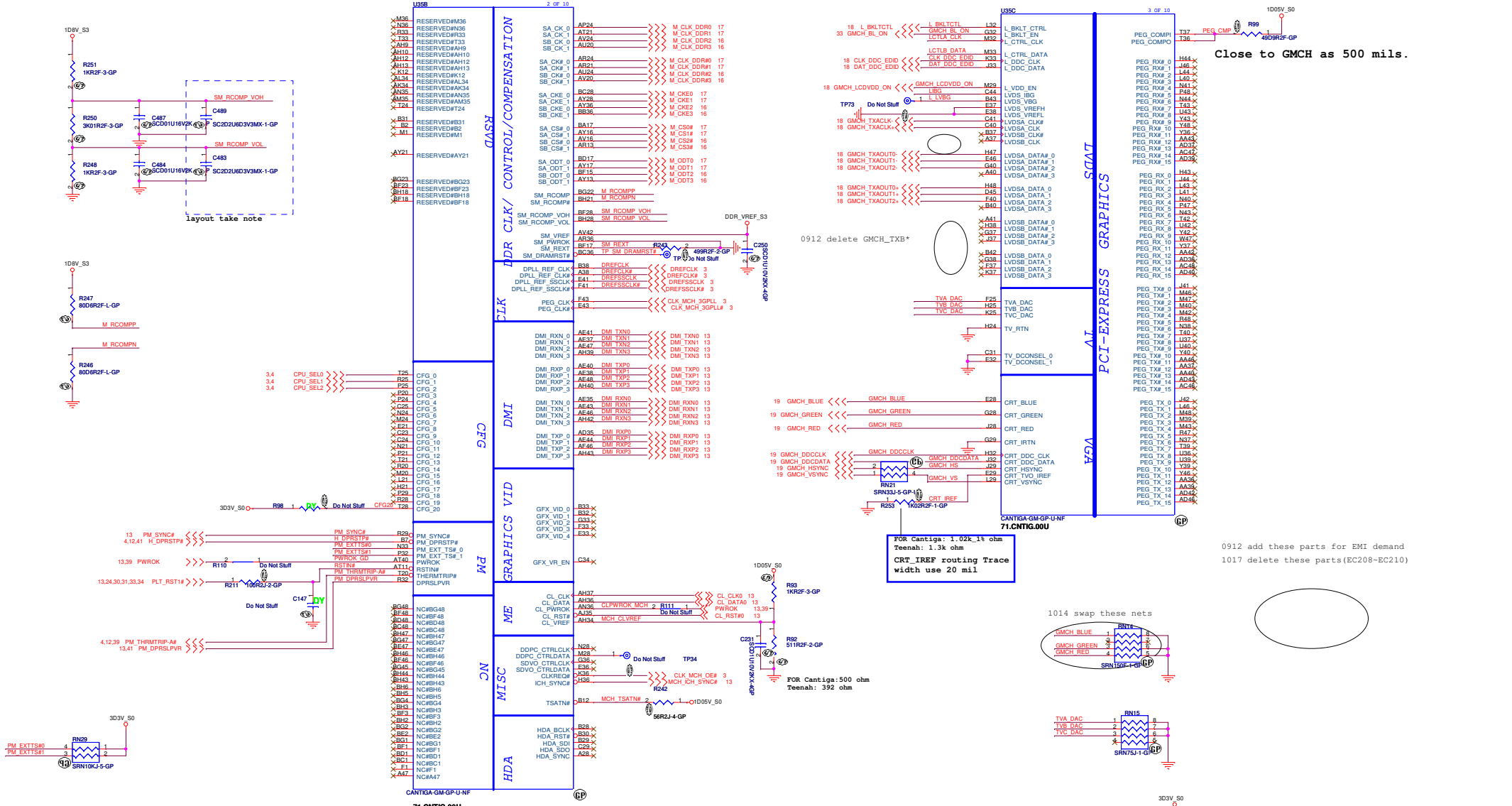

Pin Name	Strap Description	Configuration
CFG20	Digital DisplayPort (SDVO/DP/HDMI) Concurrent with PCIE	Low = Only digital DisplayPort (SDVO/DP/HDMI) or PCIE is operational (default) High = Digital DisplayPort (SDVO/DP/HDMI) and PCIE are operating simultaneously via the PEG port

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Title: Cantiga (2 of 6) DMI/PM/CFG	
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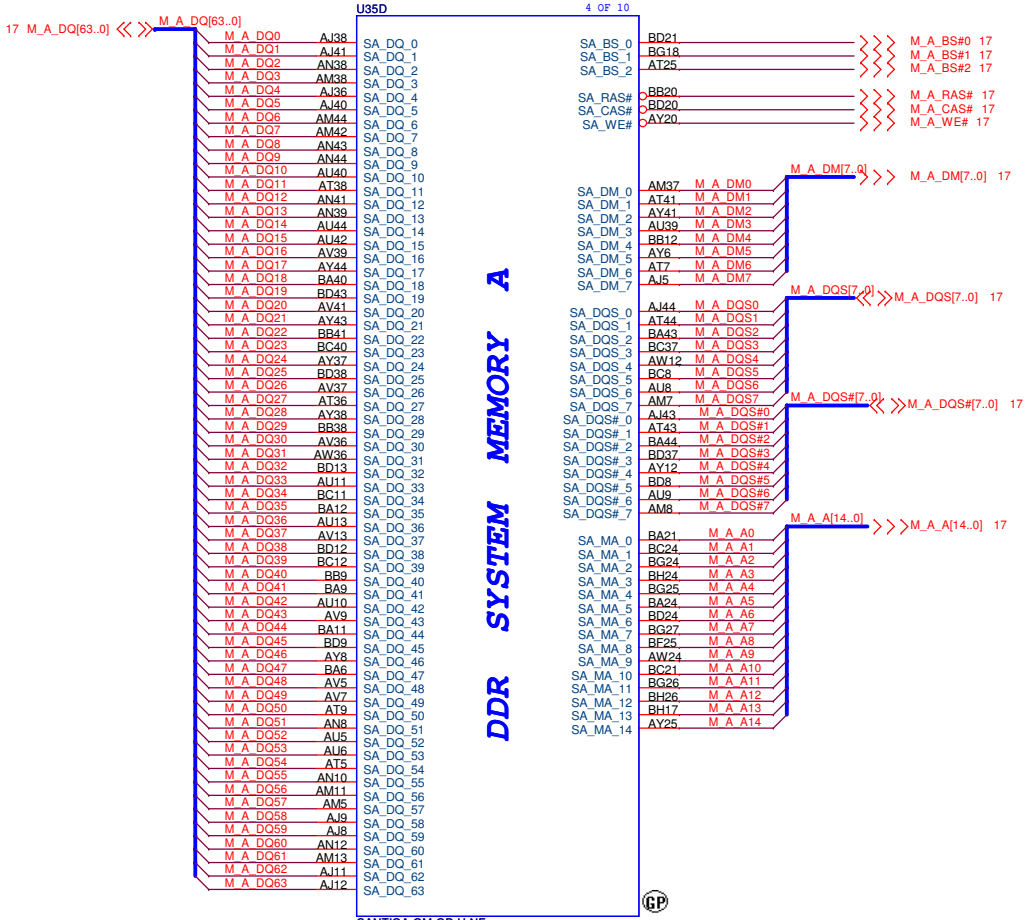
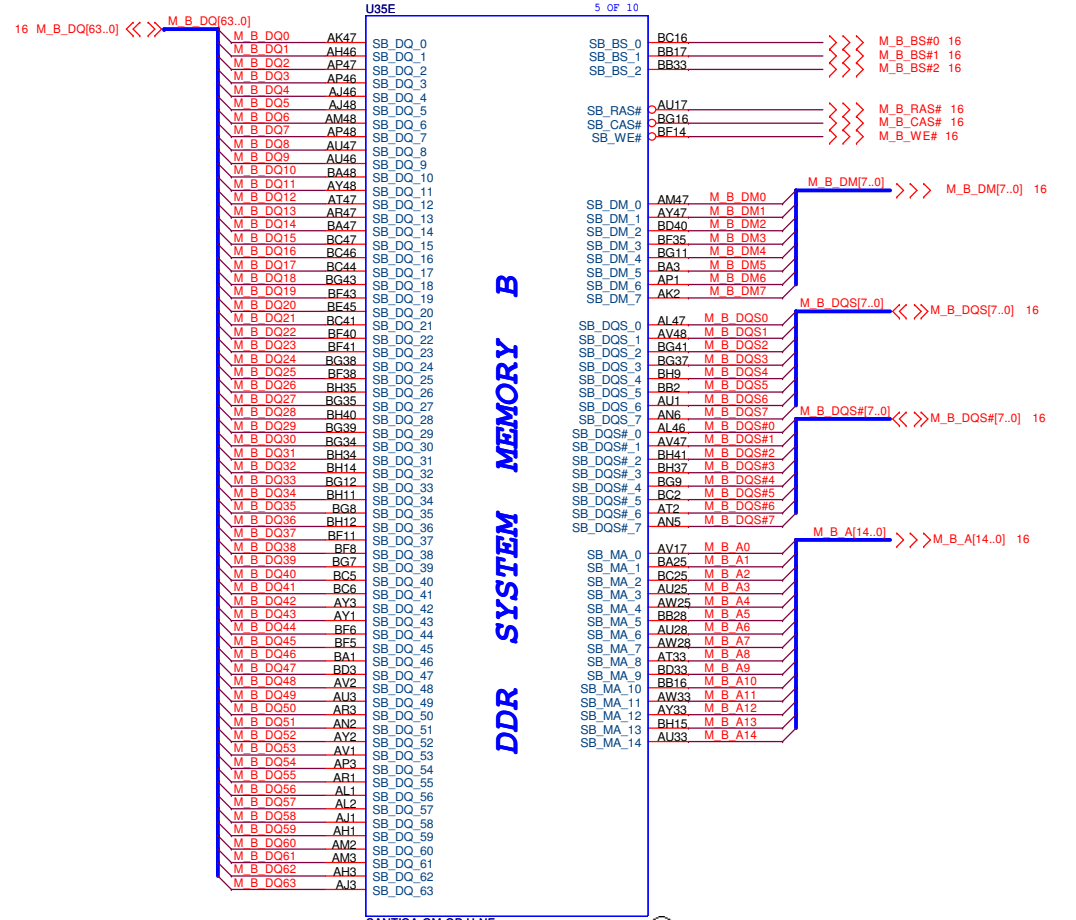


71.CNTIG.00U



71.CNTIG.00U

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Title: Cantiga (3 of 6)_DDR

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667MTS 2400mA
800MTS 3000mA

1D8V_S3

U35G

7 OF 10

VCC_SM
VCC_SM_NC
VCC_AXG
VCC_AXG_SENSE
VSS_AXG_SENSE
VCC_AXG_NCTF
VCC_SM_LF

VCC SM
VCC GFX
VCC GFX NCTF
VCC SM LF

1D05V_S0

SM_LF1_GMCH
SM_LF2_GMCH
SM_LF3_GMCH
SM_LF4_GMCH
SM_LF5_GMCH
SM_LF6_GMCH
SM_LF7_GMCH

TP33 Do Not Stuff
TP32 Do Not Stuff

CANTIGA-GM-GP-U-NF
71.CNTIG.00U

place near Cantiga

Place CAP where LVDS and DDR2 taps

FOR VCC SM

Place on the Edge

SB 1118 delete TC27

Coupling CAP 370 mils from the Edge

Coupling CAP

Do Not Stuff

U35F

6 OF 10

VCC CORE

VCC NCTF

POWER

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Title: Cantiga (4 of 6)_POWER

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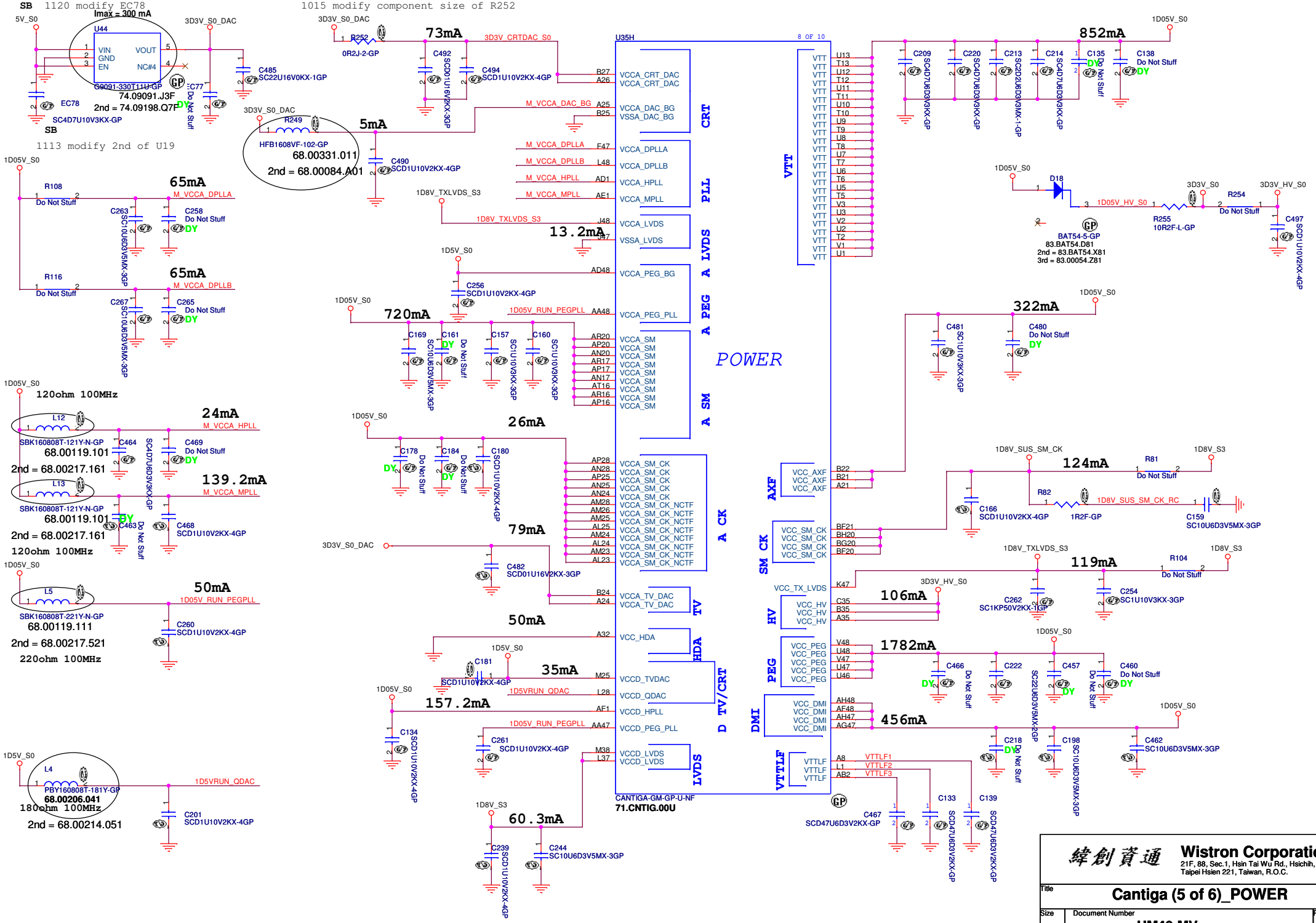
SB 1120 modify EC78

1015 modify component size of R252

1113 modify 2nd of U19



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Title	Cantiga (5 of 6)_POWER	
Size	Document Number: HM40-MV	Rev: SB
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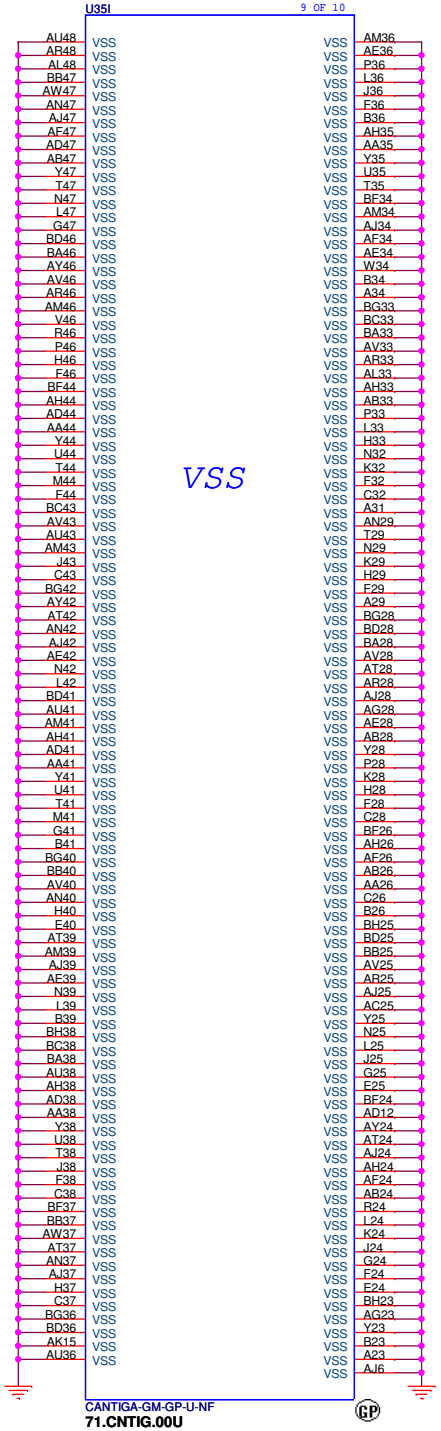

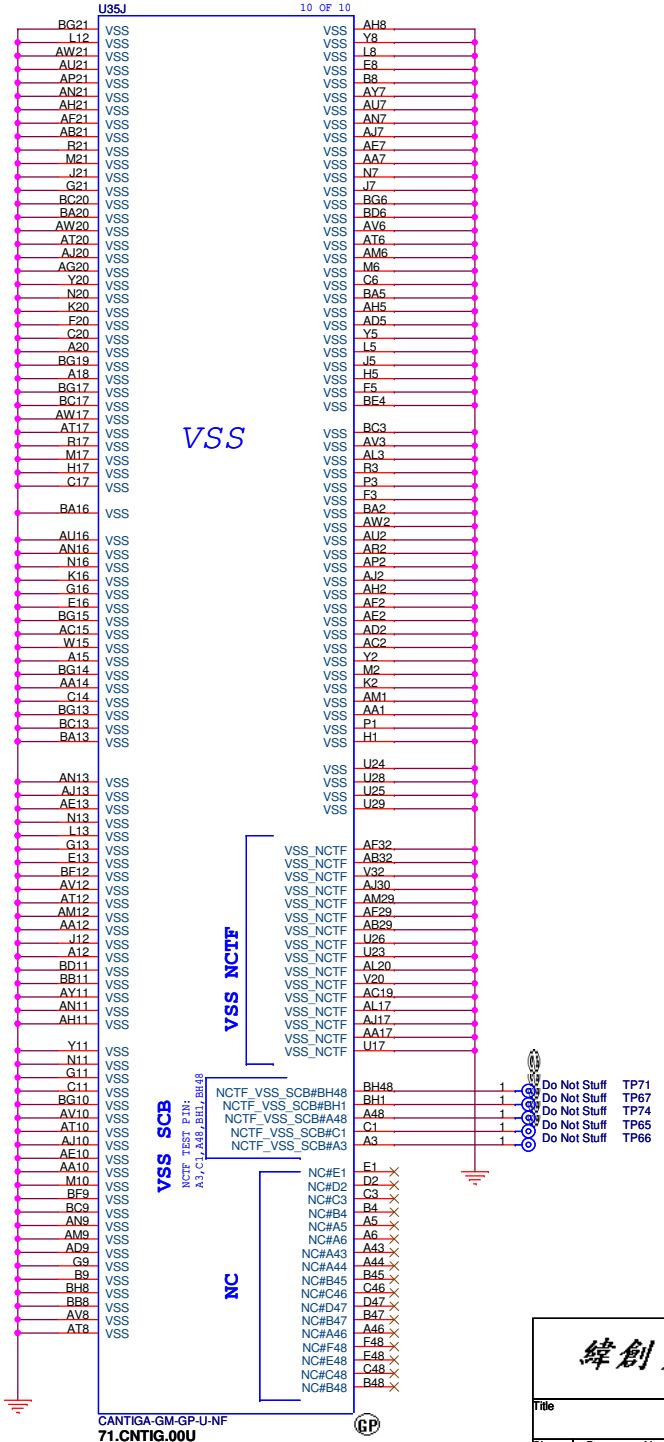

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Title: Cantiga (6 of 6)

Size | Document Number: HM40-MV | Rev: SB

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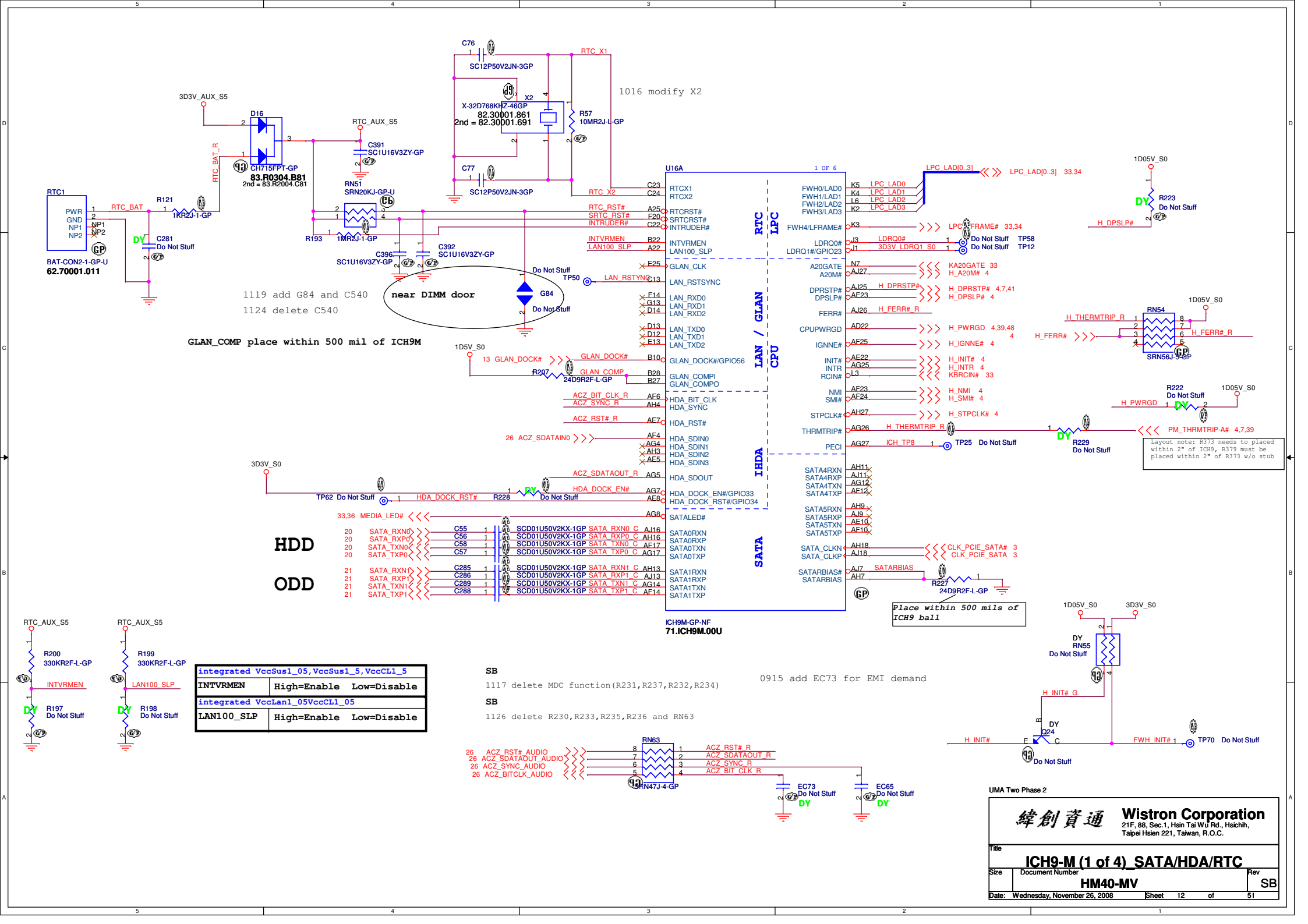
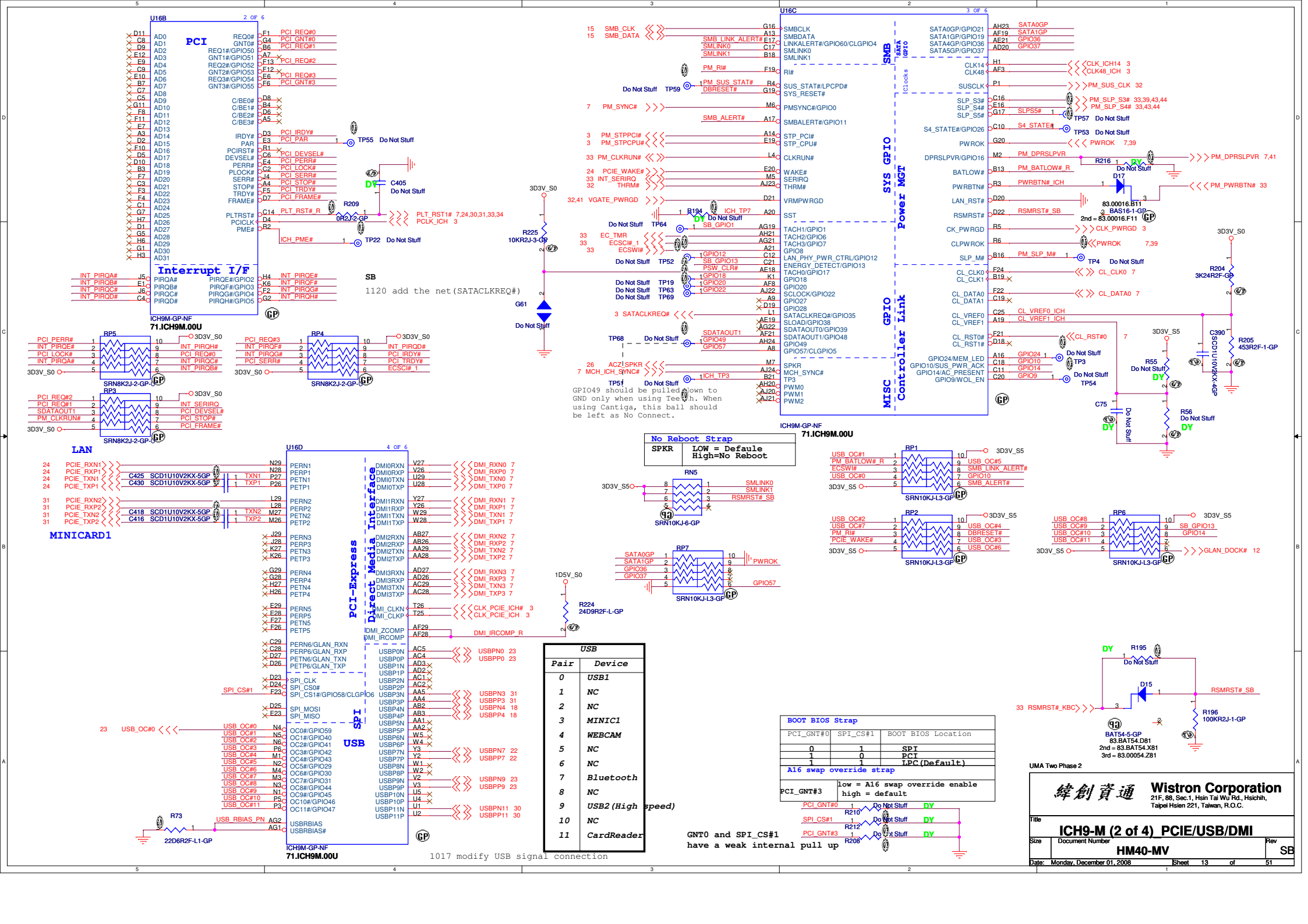
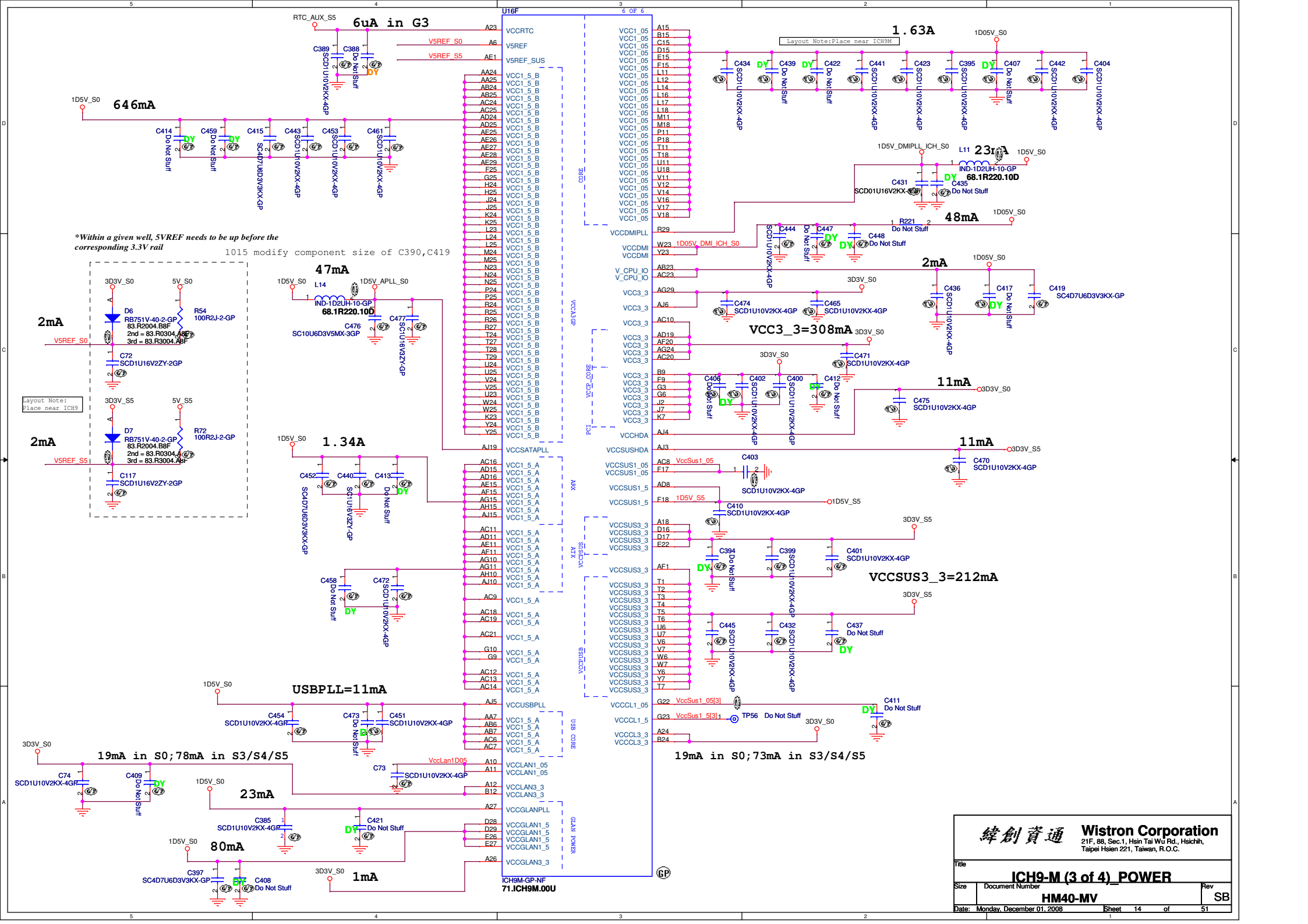
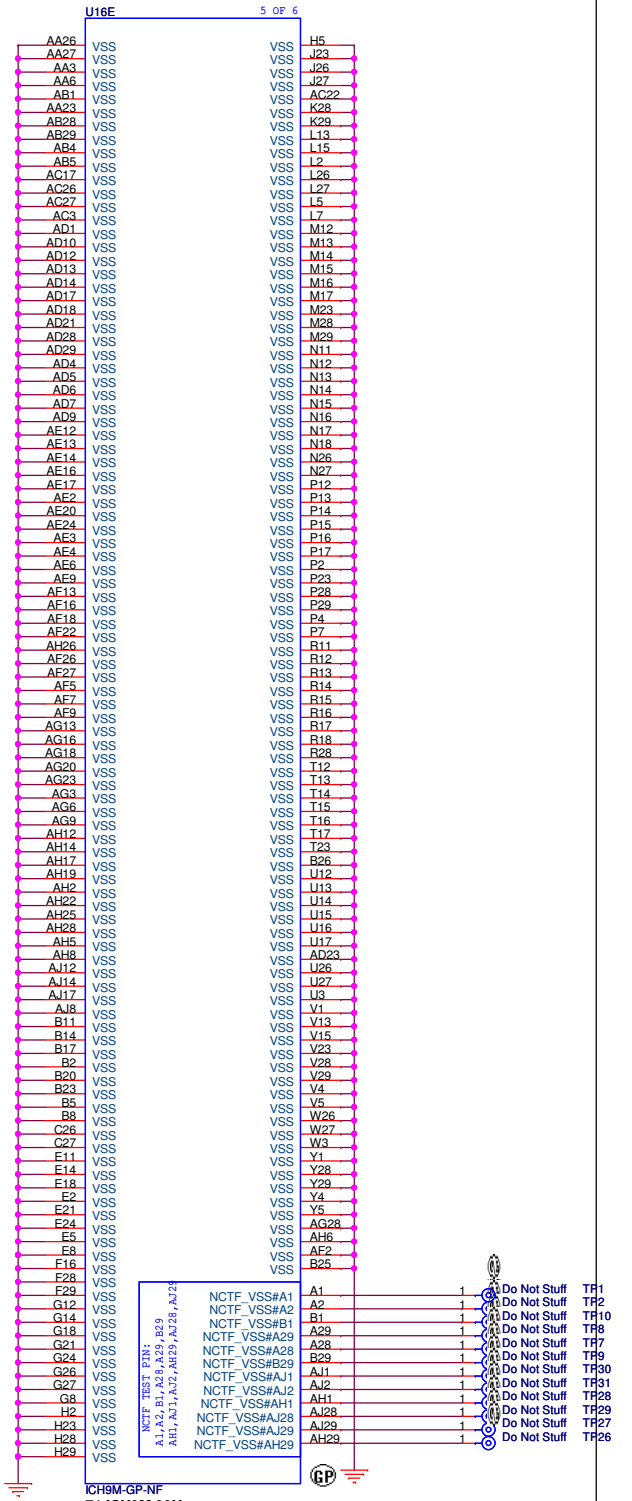
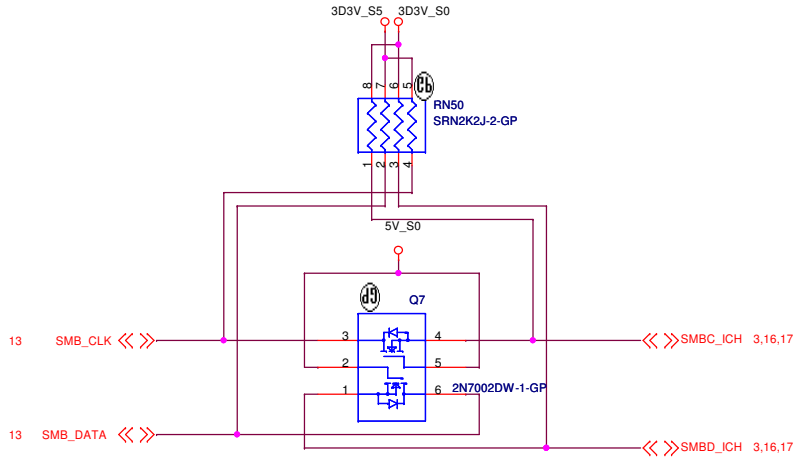

RTC1
BAT-CON2-1-GP-U
62.70001.011
RTC_BAT
R121
1KR2J-1-GP
C281
Do Not Stuff
D16
CH715FPT-GP
83.R0304.B81
2nd = 83.R2004.C81
3D3V_AUX_S5
RTC_AUX_S5
C391
SC1U16V3ZY-GP
RN51
SRN20KJ-GP-U
R193
1MR2J-1-GP
C396
SC1U16V3ZY-GP
C392
SC1U16V3ZY-GP
C76
SC12P50V2JN-3GP
C77
SC12P50V2JN-3GP
X2
X-32D768KHZ-46GP
82.30001.861
2nd = 82.30001.691
R57
10MR2J-L-GP
1016 modify X2
1119 add G84 and C540
1124 delete C540
near DIMM door
G84
Do Not Stuff
TP50
GLAN_COMP place within 500 mil of ICH9M
U16A
1 OF 6
RTCX1
RTCX2
RTCRST#
SRTCRST#
INTRUDER#
INTVRMEN
LAN100_SLP
GLAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
GLAN_DOCK#/GPIO56
GLAN_COMPI
GLAN_COMPO
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
A20GATE
A20M#
DPRSTP#
DPSLP#
FERR#
CPUPWRGD
IGNNE#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THRMTRIP#
PECI
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
SATA_CLKN
SATA_CLKP
SATARBIAS#
SATARBIAS
ICH9M-GP-NF
71.ICH9M.00U
LPC_LAD[0..3]
LPC_FRAME#
LDRQ0#
3D3V_LDRQ1_S0
Do Not Stuff
TP58
TP12
KA20GATE
H_A20M#
H_DPRSTP#
H_DPSLP#
H_FERR#_R
H_PWRGD
H_IGNNE#
H_INIT#
H_INTR
H_NMI
H_SMI#
H_STPCLK#
H_THERMTRIP_R
TP25
ICH_TP8
CLK_PCIE_SATA#
CLK_PCIE_SATA
SATARBIAS
R227
24D9R2F-L-GP
Place within 500 mils of ICH9 ball
1D05V_S0
R223
Do Not Stuff
RN54
SRN56J-3-GP
R222
Do Not Stuff
R229
Do Not Stuff
PM_THRMTRIP-A# 4,7,39
Layout note: R373 needs to placed within 2" of ICH9, R379 must be placed within 2" of R373 w/o stub
HDD
ODD
SCD01U50V2KX-1GP
SATA_RXN0_C
SATA_RXP0_C
SATA_TXN0_C
SATA_TXP0_C
SATA_RXN1_C
SATA_RXP1_C
SATA_TXN1_C
SATA_TXP1_C
MEDIA_LED#
HDA_DOCK_RST#
HDA_DOCK_EN#
ACZ_BIT_CLK_R
ACZ_SYNC_R
ACZ_RST#_R
ACZ_SDATAIN0
ACZ_SDATAOUT_R
R207
24D9R2F-L-GP
R228
TP62
R200
330KR2F-L-GP
R199
330KR2F-L-GP
R197
Do Not Stuff
R198
Do Not Stuff
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN
High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP
High=Enable Low=Disable
SB
1117 delete MDC function(R231,R237,R232,R234)
SB
1126 delete R230,R233,R235,R236 and RN63
0915 add EC73 for EMI demand
RN63
SMN47J-4-GP
ACZ_RST# R
ACZ_SDATAOUT_R
ACZ_SYNC_R
ACZ_BIT_CLK_R
EC73
Do Not Stuff
EC65
Do Not Stuff
RN55
Do Not Stuff
H_INIT#_G
Q24
FWH_INIT#
TP70
Do Not Stuff
UMA Two Phase 2
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-M (1 of 4)_SATA/HDA/RTC
Size
Document Number
HM40-MV
Rev
SB
Date: Wednesday, November 26, 2008
Sheet 12 of 51


U16B
PCI
Interrupt I/F
ICH9M-GP-NF
71.ICH9M.00U
SB
1120 add the net(SATACLKREQ#)
U16C
SMB
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
ICH9M-GP-NF
71.ICH9M.00U
No Reboot Strap
SPKR
LOW = Defaule
High=No Reboot
GPIO49 should be pulled down to GND only when using Teefnth. When using Cantiga, this ball should be left as No Connect.
LAN
MINICARD1
U16D
PCI-Express
Direct Media Interface
SPI
USB
ICH9M-GP-NF
71.ICH9M.00U
1017 modify USB signal connection
USB
Pair
Device
0
USB1
1
NC
2
NC
3
MINIC1
4
WEBCAM
5
NC
6
NC
7
Bluetooth
8
NC
9
USB2 (High speed)
10
NC
11
CardReader
GNT0 and SPI_CS#1 have a weak internal pull up
BOOT BIOS Strap
PCI_GNT#0
SPI_CS#1
BOOT BIOS Location
0
1
SPI
1
0
PCI
1
1
LPC (Default)
A16 swap override strap
PCI_GNT#3
low = A16 swap override enable
high = default
UMA Two Phase 2
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-M (2 of 4) PCIE/USB/DMI
Size
Document Number
HM40-MV
Rev
SB
Date: Monday, December 01, 2008
Sheet 13 of 51


6uA in G3
646mA
1.63A
23mA
48mA
2mA
47mA
1.34A
VCC3_3=308mA
11mA
11mA
2mA
VCCSUS3_3=212mA
USBPLL=11mA
19mA in S0;78mA in S3/S4/S5
23mA
80mA
1mA
19mA in S0;73mA in S3/S4/S5
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
1015 modify component size of C390,C419
Layout Note:Place near ICH9M
Layout Note: Place near ICH9
U16F
6 OF 6
ICH9M-GP-NF
71.ICH9M.00U
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-M (3 of 4)_POWER
Size
Document Number
HM40-MV
Rev
SB
Date: Monday, December 01, 2008
Sheet 14 of 51



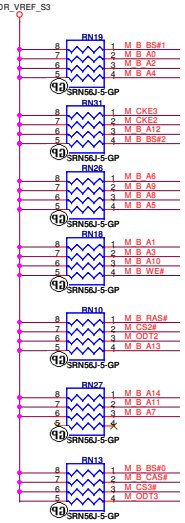


SMBUS

緯創資通	**Wistron Corporation**
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**ICH9-M (4 of 4)**
Size	Document Number: **HM40-MV** — Rev: SB
Date: Monday, December 01, 2008	Sheet 15 of 51

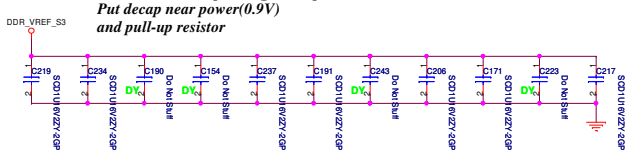
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor



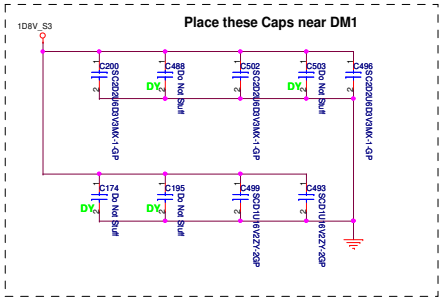
Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor



High 9.2mm

62.10017.A71
2nd = 62.10017.B51
3rd = 62.10017.K51



緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

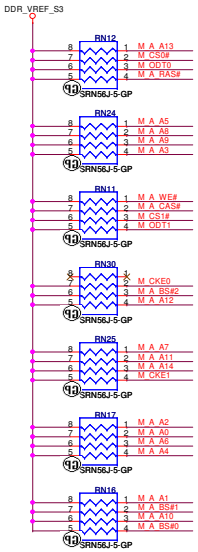
Title: **DDR2 Socket 0 (DM1)**

Size	Document Number	Rev
	HM40-MV	SB

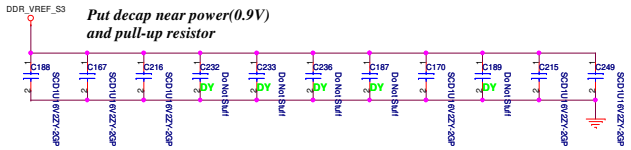
Date: Monday, December 01, 2008 Sheet 16 of 51

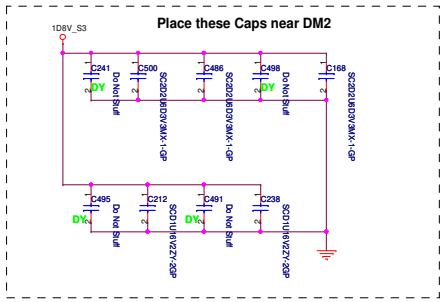
PARALLEL TERMINATION

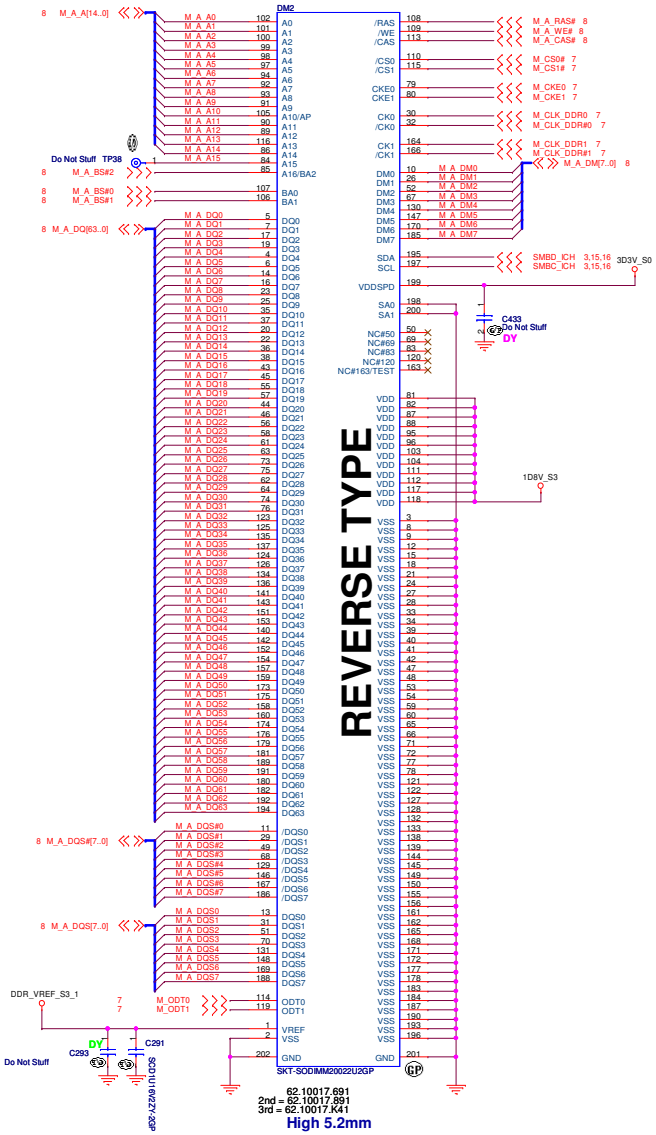
Put decap near power(0.9V) and pull-up resistor



Decoupling Capacitor







緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR2 Socket 1 (DM2)

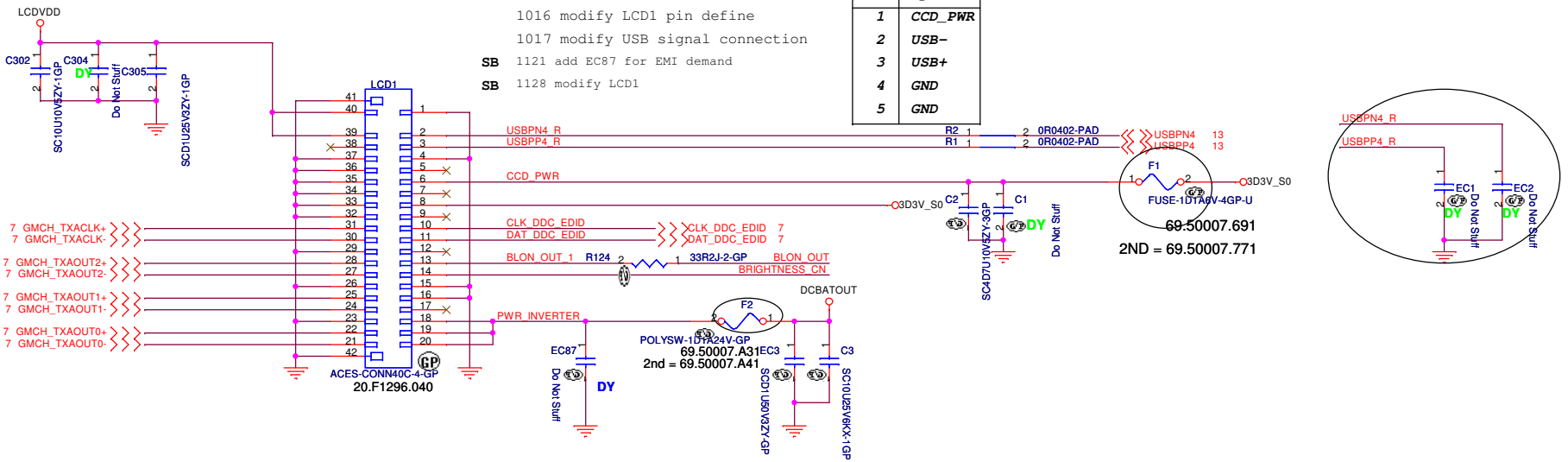
Size | Document Number: HM40-MV | Rev: SB

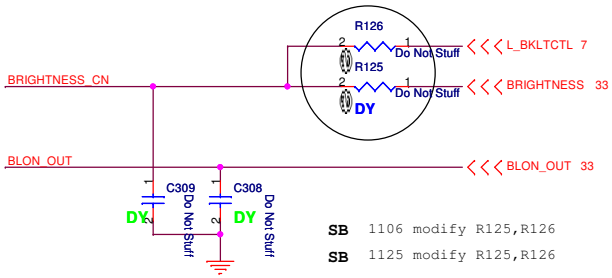
Date: Monday, December 01, 2008 | Sheet 17 of 51

LCD/CCD CONN

1015 modify F1
1015 modify LCD1 pin define
1016 modify LCD1 pin define
1017 modify USB signal connection
SB 1121 add EC87 for EMI demand
SB 1128 modify LCD1

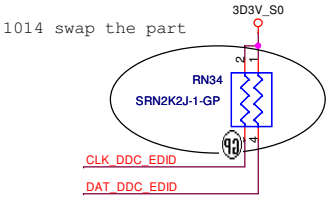
CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND



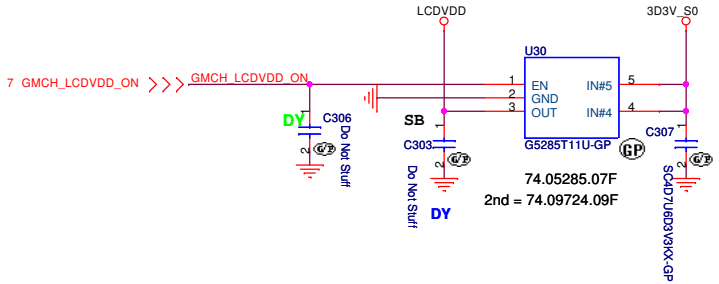


SB 1106 modify R125,R126
SB 1125 modify R125,R126

1014 swap the part



Layout 40 mil



1015 modify component size of C303,C307

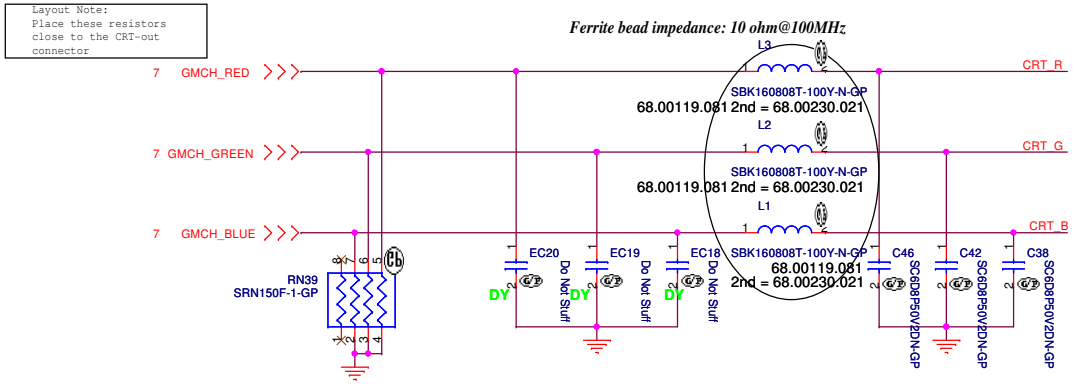
UMA Two Phase 2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD CONN
Size | Document Number: HM40-MV | Rev: SB
Date: Friday, November 28, 2008 | Sheet 18 of 51

Layout Note:
Place these resistors close to the CRT-out connector

Ferrite bead impedance: 10 ohm@100MHz

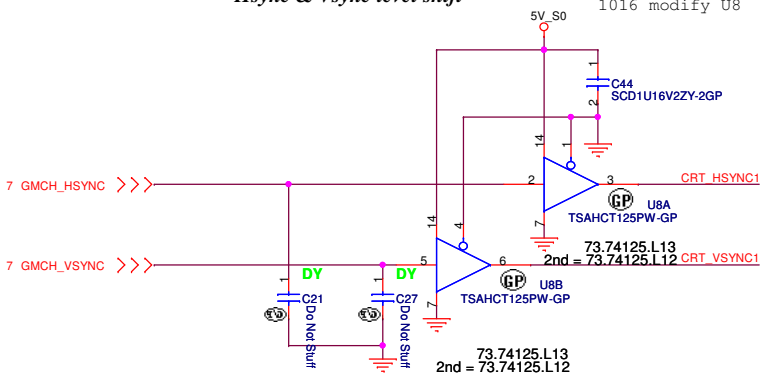


1016 modify L1,L2 and L3

Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

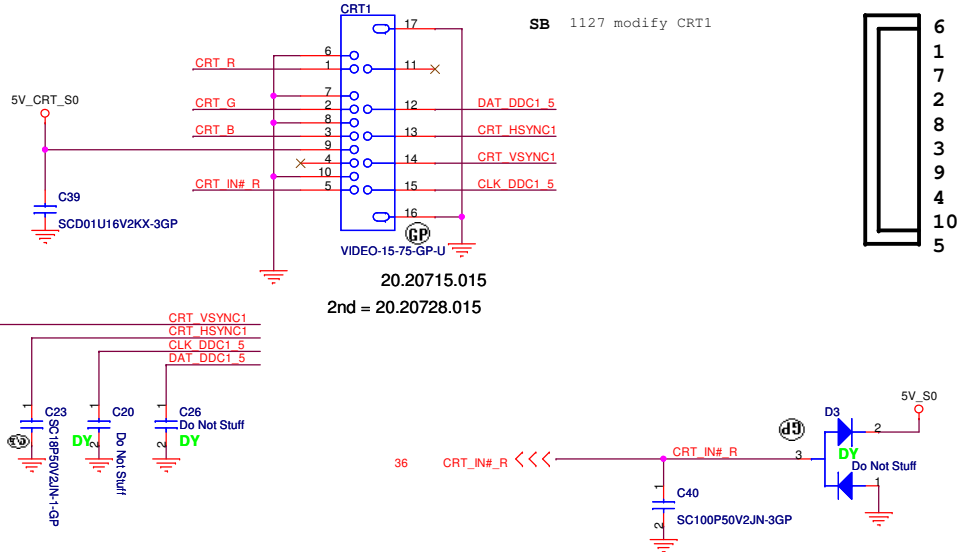
Hsync & Vsync level shift

1016 modify U8

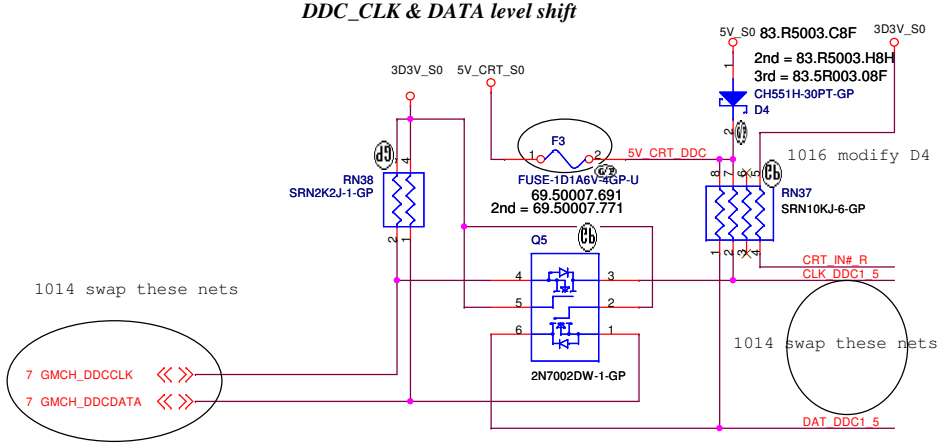


CRT I/F & CONNECTOR

SB 1127 modify CRT1



DDC_CLK & DATA level shift



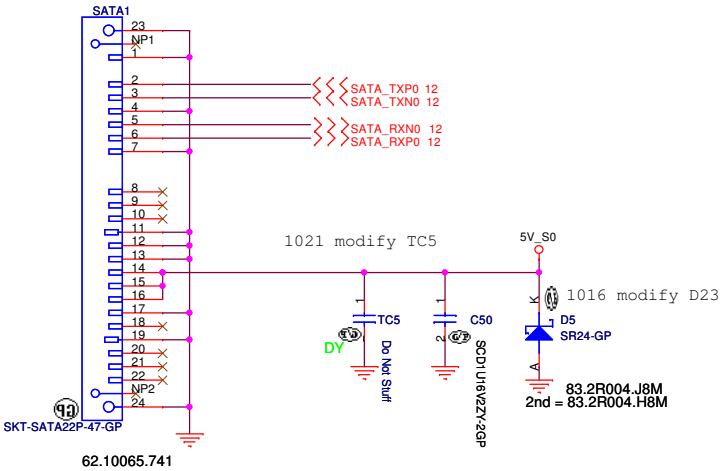
UMA Two Phase 2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	**CRT Connector**	
Size	Document Number **HM40-MV**	Rev SB
Date: Monday, December 01, 2008	Sheet 19 of 51	

SATA Connector

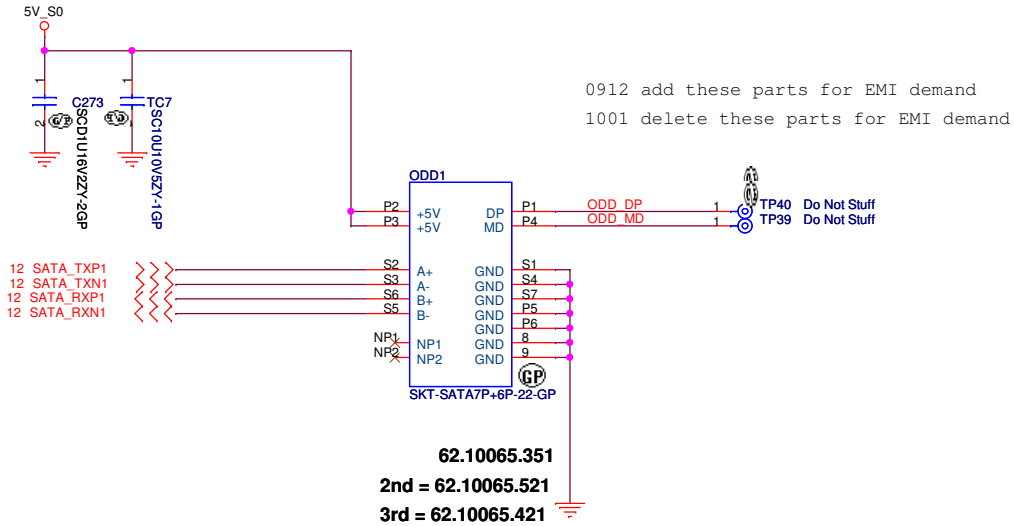
0912 add these parts for EMI demand
1001 delete these parts for EMI demand
1021 modify SATA1



UMA Two Phase 2

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: HDD		
Size	Document Number: HM40-MV	Rev: SB
Date: Monday, December 01, 2008	Sheet 20 of 51	

SATA ODD Connector



UMA Two Phase 2

緯創資通 **Wistron Corporation**
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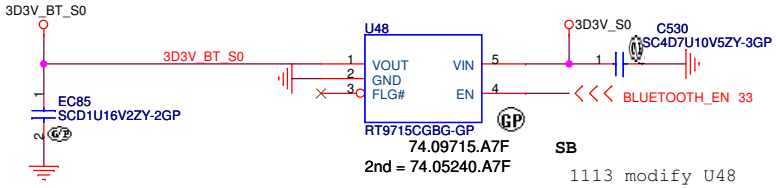
Taipei Hsien 221, Taiwan, R.O.C.

Title		
ODD		
Size	Document Number	Rev
	HM40-MV	SB
Date: Monday, December 01, 2008	Sheet 21 of 51	

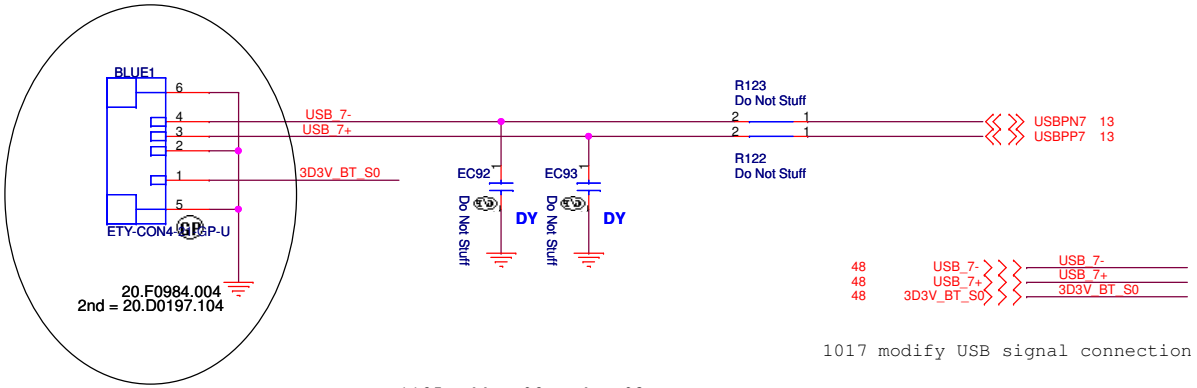
BLUETOOTH MODULE

1.5A / High Active Voltage 2V



1113 modify U48

EC21 put near BLUE1 / all USB put one choke near connector by EMI request



1017 modify USB signal connection

SB 1125 add EC92 and EC93

0930 modify BLUE1

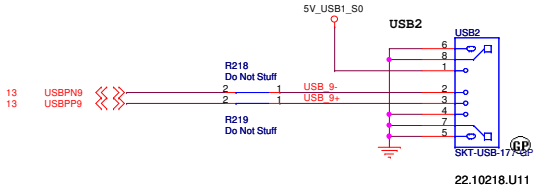
1017 modify BLUE1

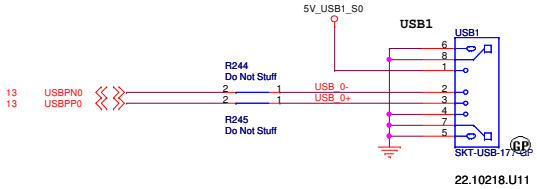
UMA Two Phase 2

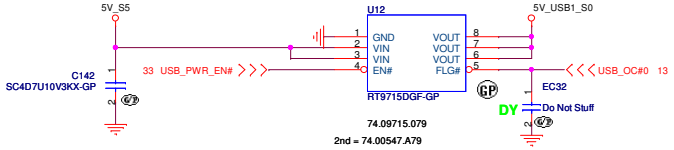
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: **Bluetooth**		
Size	Document Number: **HM40-MV**	Rev: SB
Date: Wednesday, November 26, 2008	Sheet 22 of 51	

1017 modify USB signal connection

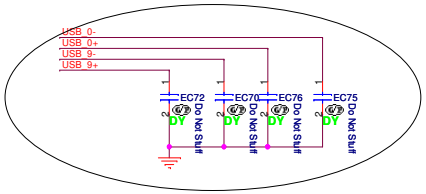
1021 modify and swap these parts(USB1 and USB2)



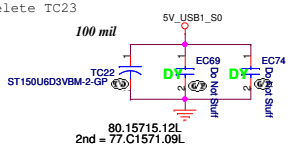




0912 add these parts for EMI demand



1021 delete TC23



UMA Two Phase 2

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**USB**
Size	Document Number: **HM40-MV** — Rev: SB
Date: Monday, December 01, 2008	Sheet 23 of 51

1015 modify component size of R69

Close to AR8114 Pin2

AR8132 use 0 ohm resiter

AR8114A Atheros suggestion change to Bead
60 ohms/100Mhz 500mA (68.60090.0D1)

FOR AR8114A LAN_ACT_LED is high enable pin

1016 modify RN53 and U10

1001 modify RN9

1014 swap these nets

1126 add R303,R304

1113 modify C103 and C106

AR8114 use 0ohm resister
AR8132 Atheros suggest to change 4.7uH choke

1015 modify component size of R79

1016 modify Q8

1128 Add L19

Close to AR8114 Pin1

Close to AR8114 Pin6

Atheros suggestion change to Bead
60 ohms/100Mhz 500mA (68.60090.0D1)

UMA Two Phase 2

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Atheros AR8114/8132

Size: A3 | Document Number: HM40-MV | Rev: SB

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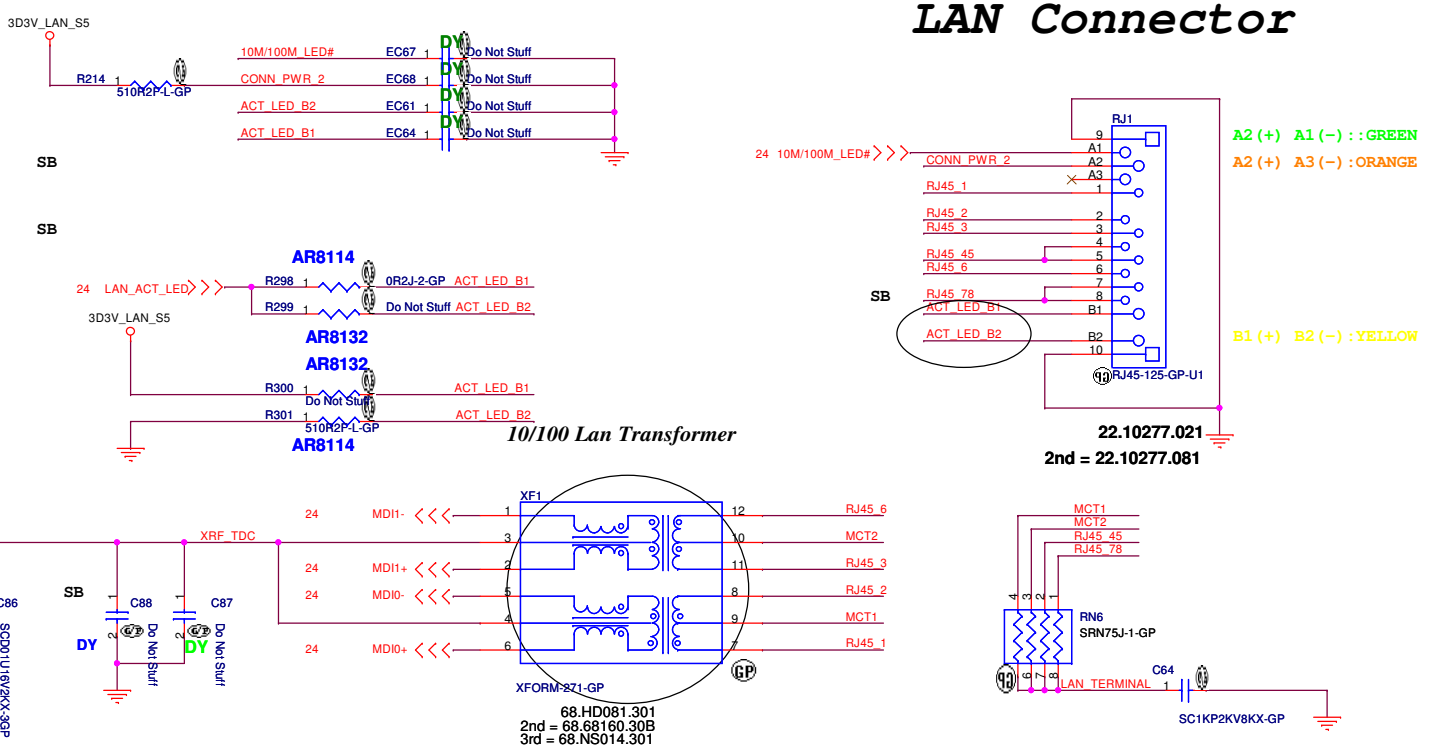
LAN Connector



1016 modify XF1

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

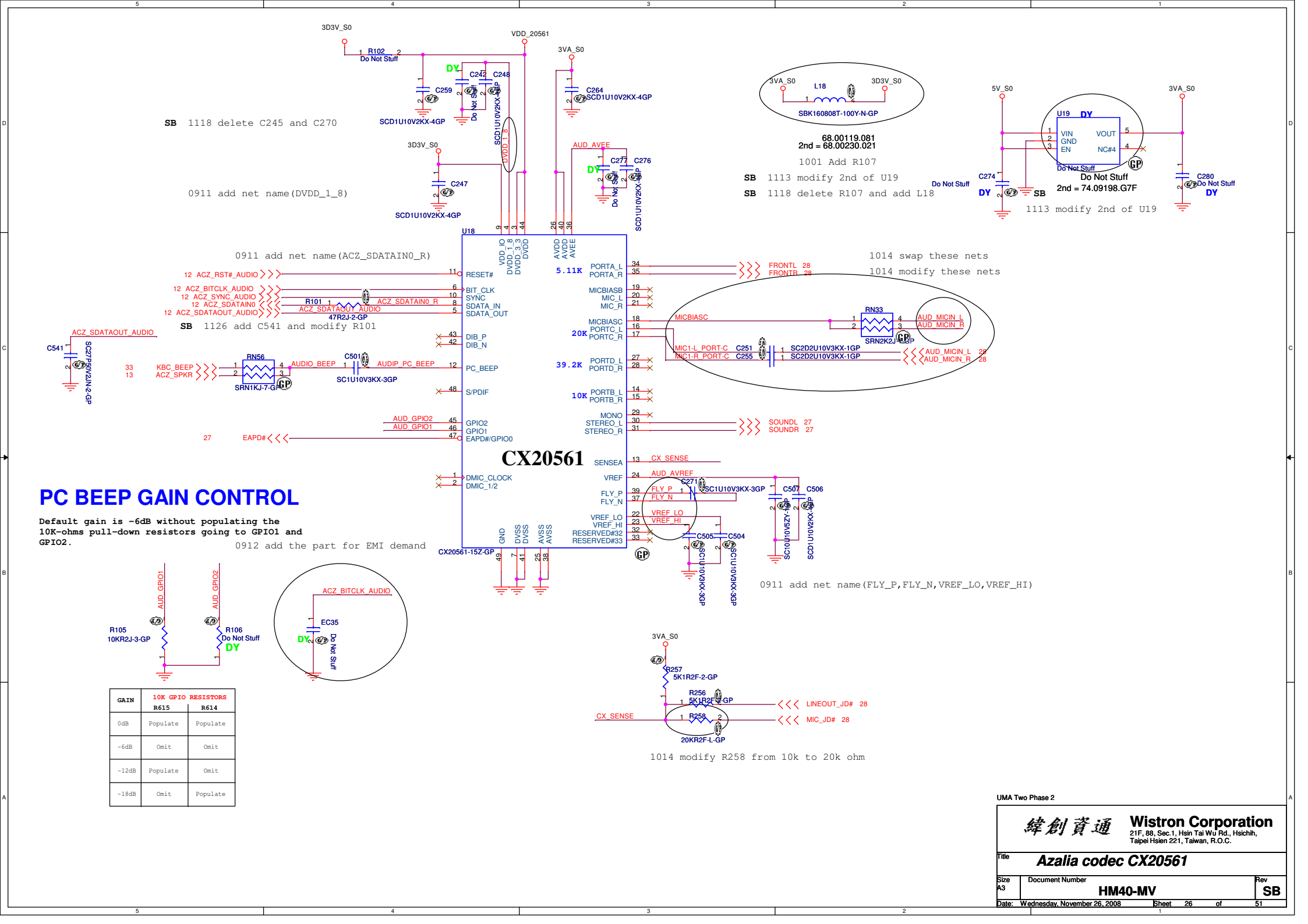
UMA Two Phase 2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN Connector**

Size	Document Number	Rev
A3	HM40-MV	SB

Date: Monday, December 01, 2008 Sheet 25 of 51



GAIN	10K GPIO RESISTORS	
	R615	R614
0dB	Populate	Populate
-6dB	Omit	Omit
-12dB	Populate	Omit
-18dB	Omit	Populate

UMA Two Phase 2

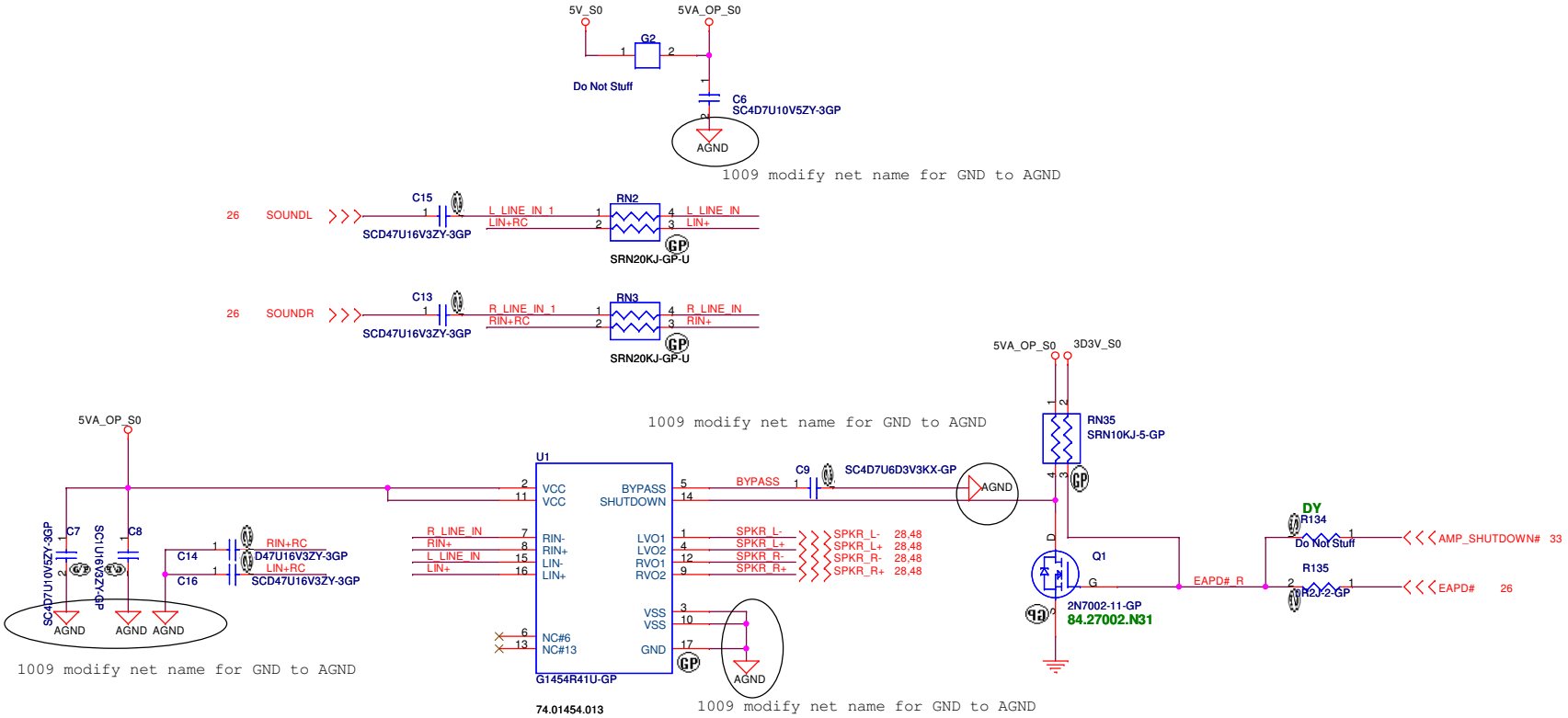
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

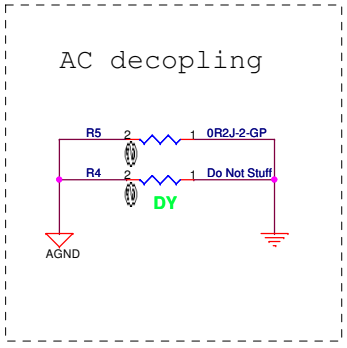
Title: Azalia codec CX20561

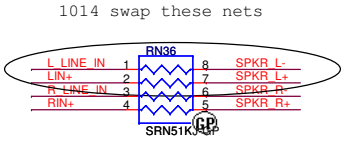
Size	Document Number	Rev
A3	HM40-MV	SB

Date: Wednesday, November 26, 2008 Sheet 26 of 51

AUDIO OP AMPLIFIER



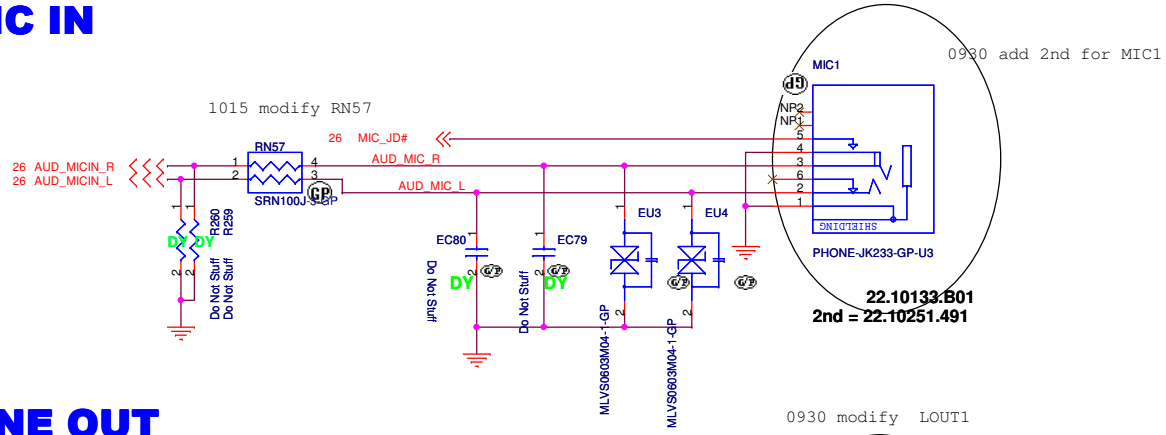




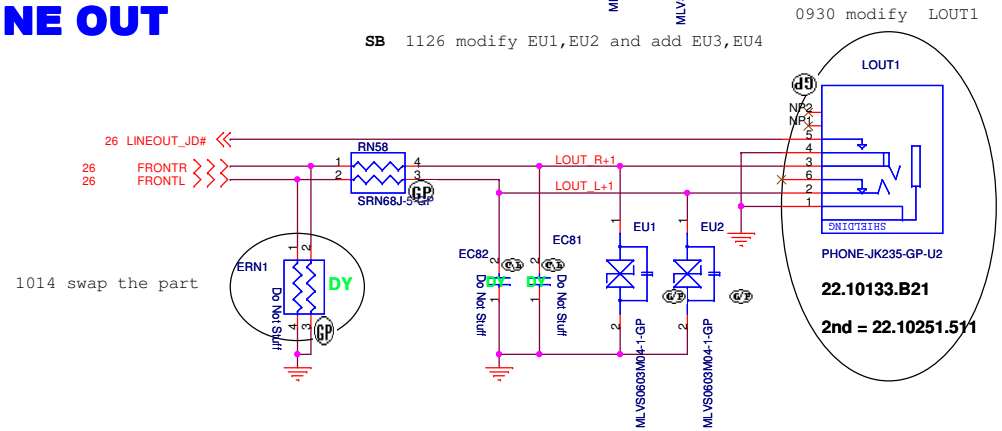
UMA Two Phase 2

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**AUDIO AMP**
Size	Document Number: HM40-MV — Rev: SB
Date: Monday, December 01, 2008	Sheet 27 of 51

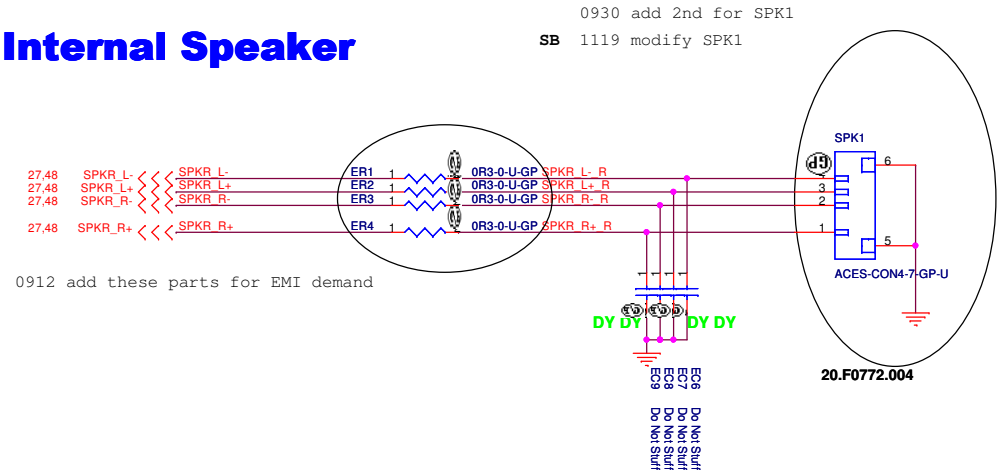
MIC IN



LINE OUT



Internal Speaker



UMA Two Phase 2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO JACK

Size | Document Number: HM40-MV | Rev: SB

Date: Monday, December 01, 2008 | Sheet 28 of 51

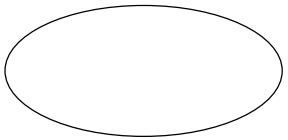
MDC 1.5 CONN

0912 add the part for EMI demand

1002 modify MDC1

SB

1112 delete MDC function



UMA Two Phase 2

緯創資通 Wistron Corporation
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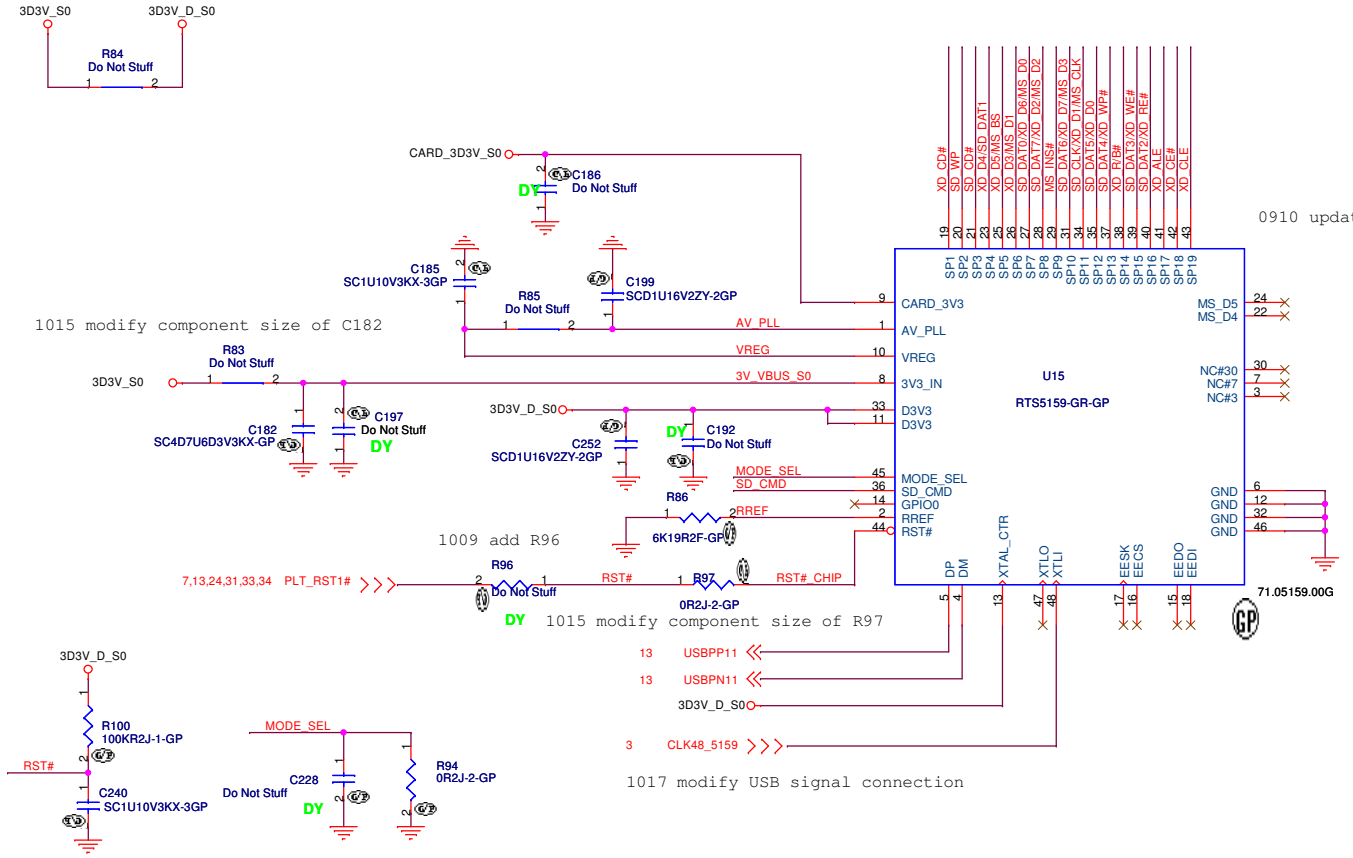
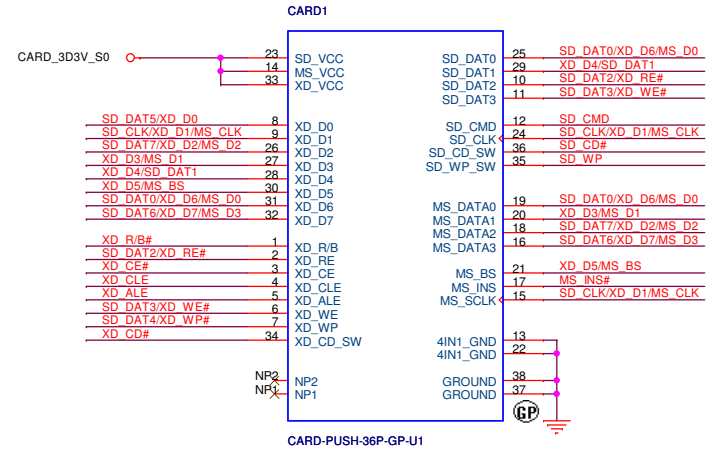
Taipei Hsien 221, Taiwan, R.O.C.

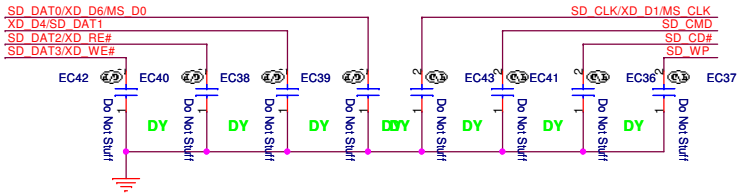
Title		
MDC		
Size	Document Number	Rev
	HM40-MV	SB
Date: Monday, November 24, 2008	Sheet 29 of 51	

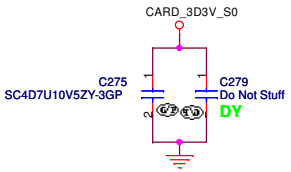


5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)

1009 modify this net
1013 modify card1







UMA Two Phase 2

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: CARD READER- RTS5159

Size	Document Number	Rev
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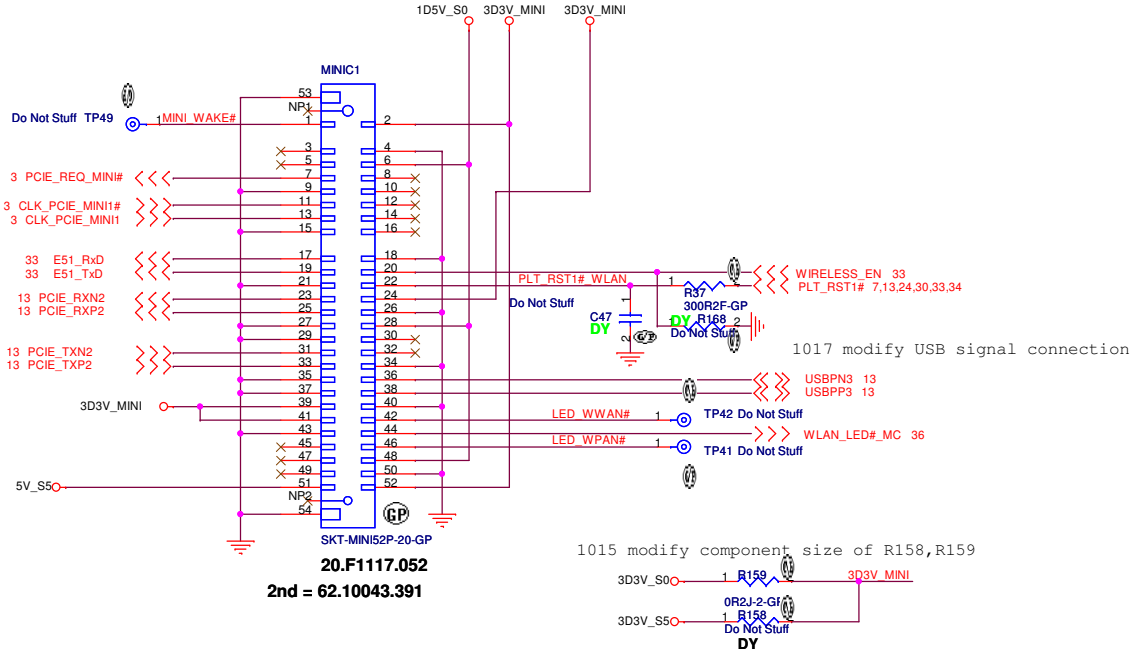
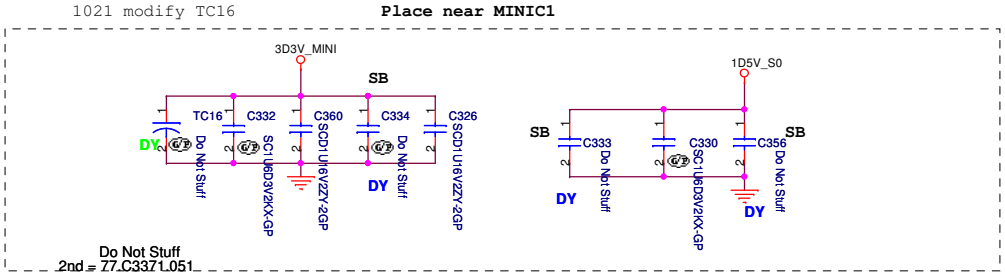
Date: Monday, December 01, 2008 Sheet 30 of 51

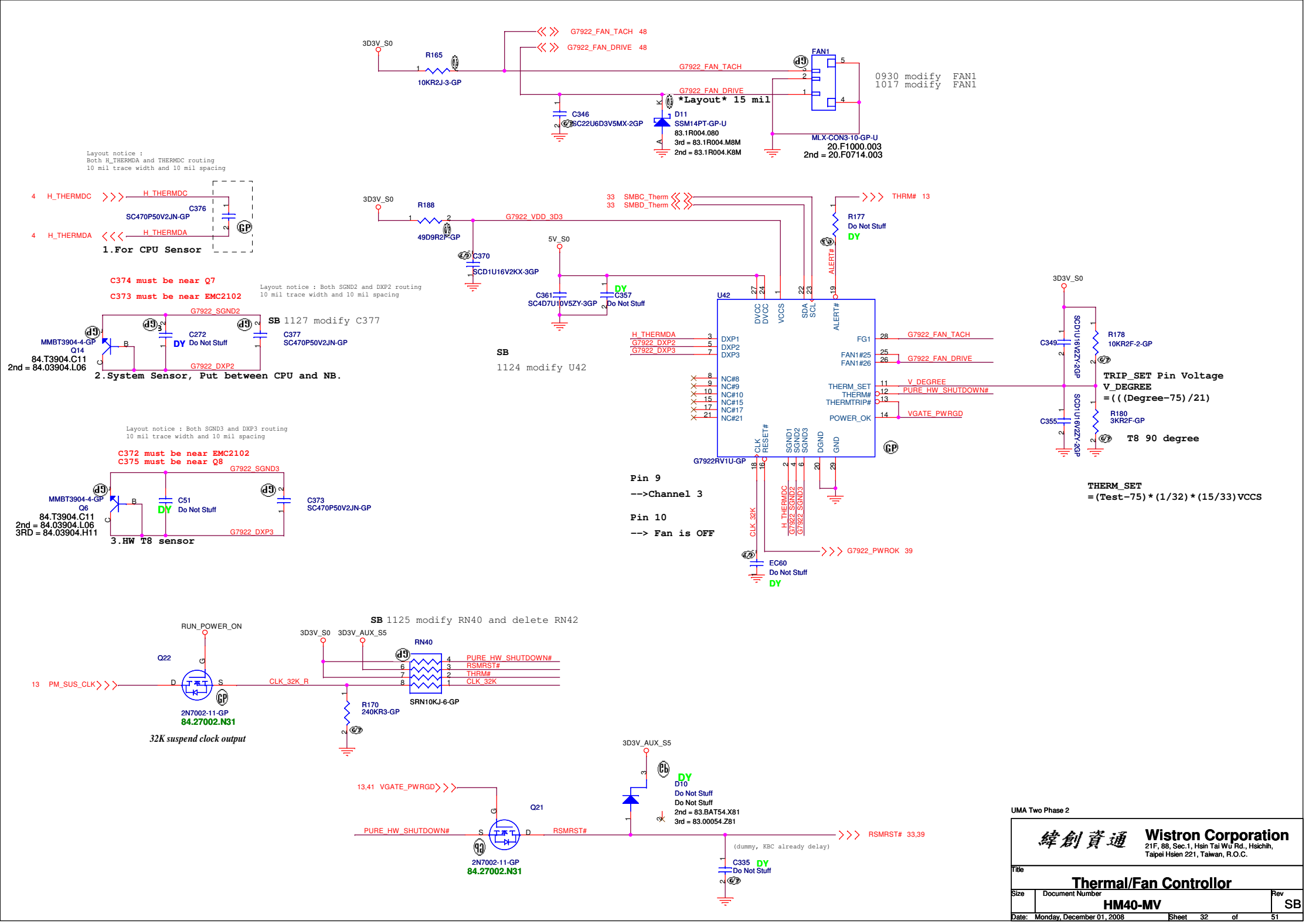
Mini Card Connector(WLAN)





UMA Two Phase 2

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**MINI CARD**
Size	Document Number: **HM40-MV** — Rev: SB
Date: Monday, December 01, 2008	Sheet 31 of 51



UMA Two Phase 2

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor

Size	Document Number	Rev
	HM40-MV	SB

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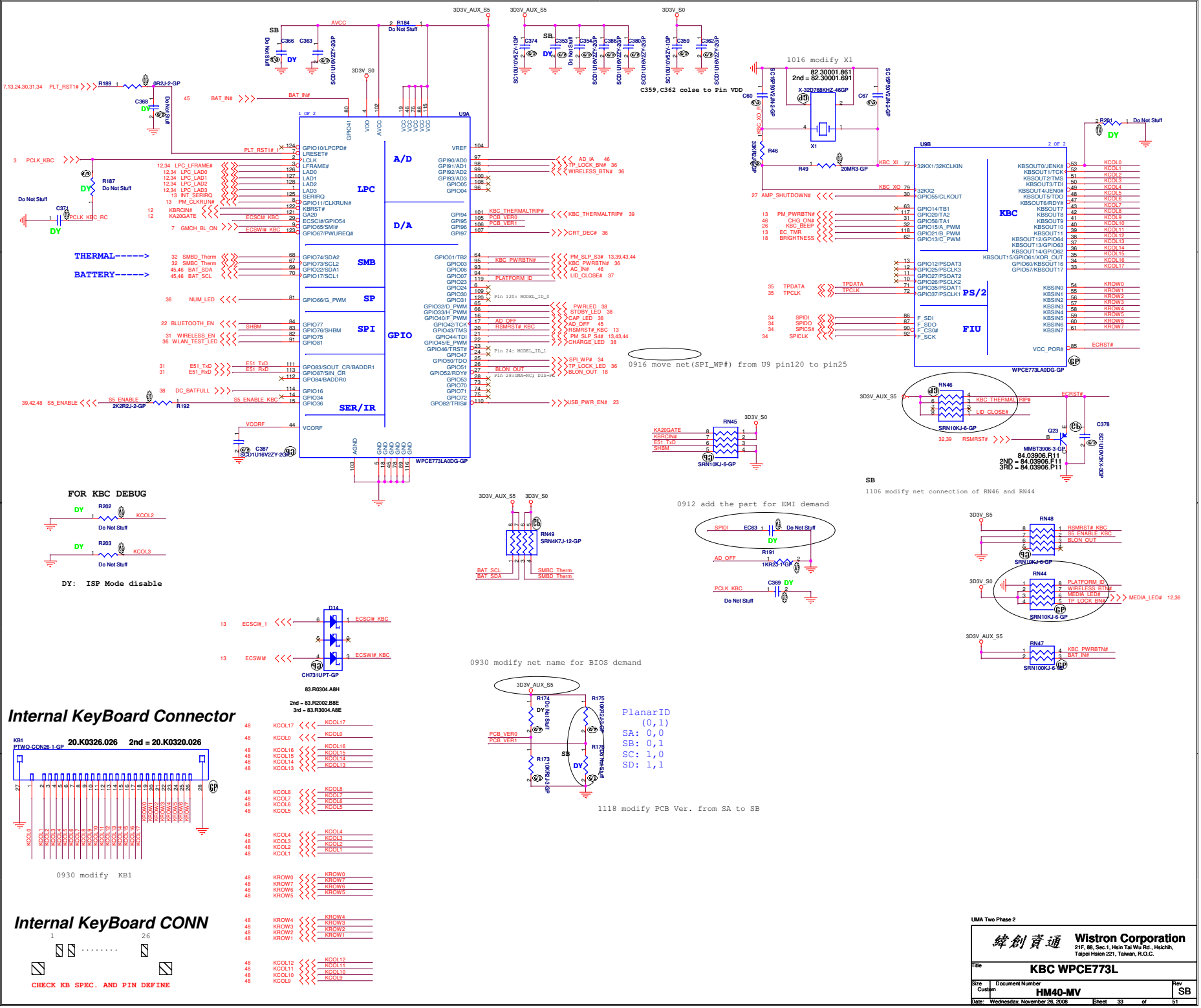
U9A
WPCE773LA0DG-GP
A/D
D/A
LPC
SMB
SP
SPI
GPIO
SER/IR
U9B
KBC
PS/2
FIU
WPCE773LA0DG-GP
1016 modify X1
82.30001.861
2nd = 82.30001.691
X-32768KHZ-48GP
C359,C362 colse to Pin VDD
0916 move net(SPI_WP#) from U9 pin120 to pin25
1106 modify net connection of RN46 and RN44
0912 add the part for EMI demand
0930 modify net name for BIOS demand
1118 modify PCB Ver. from SA to SB
PlanarID
(0,1)
SA: 0,0
SB: 0,1
SC: 1,0
SD: 1,1
FOR KBC DEBUG
DY: ISP Mode disable
Internal KeyBoard Connector
20.K0326.026 2nd = 20.K0320.026
0930 modify KB1
Internal KeyBoard CONN
CHECK KB SPEC. AND PIN DEFINE
83.R0304.ABH
2nd = 83.R2002.B8E
3rd = 83.R3004.ABE
UMA Two Phase 2
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC WPCE773L
HM40-MV
SB
Wednesday, November 26, 2008
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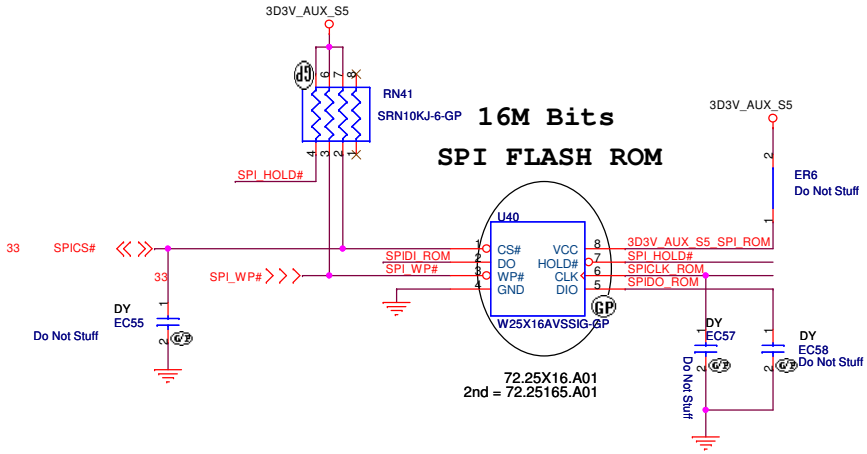
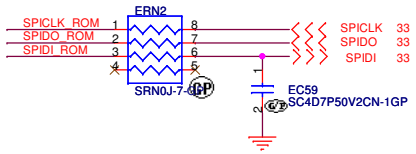
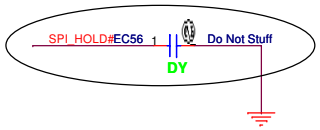


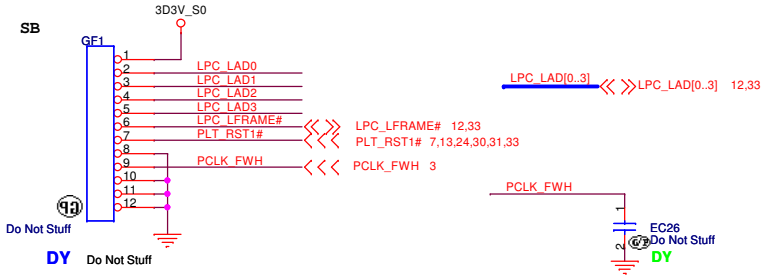


GOLDEN FINGER FOR DEBUG BOARD

1013 modify U40 from 72.25X16.001 to 72.25X16.A01

0912 add the part for EMI demand





UMA Two Phase 2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	**BIOS/GOLDEN FINGER**	
Size	Document Number **HM40-MV**	Rev SB
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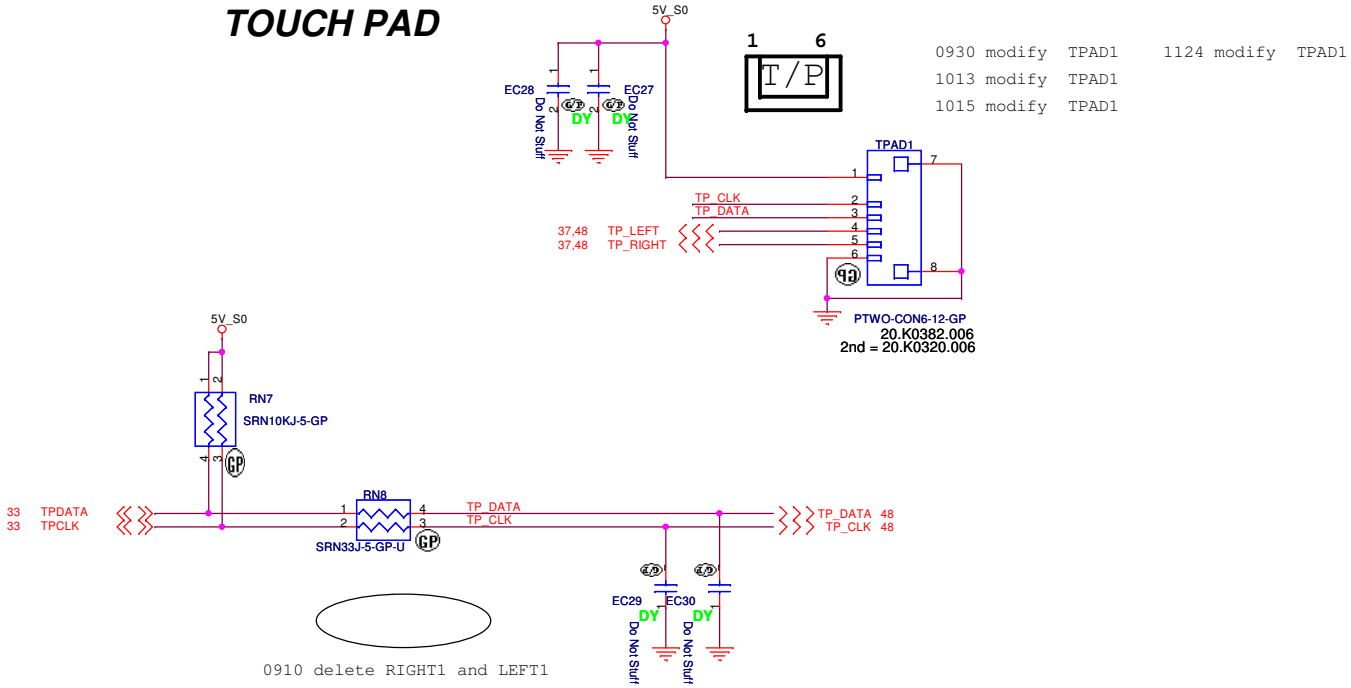
TOUCH PAD



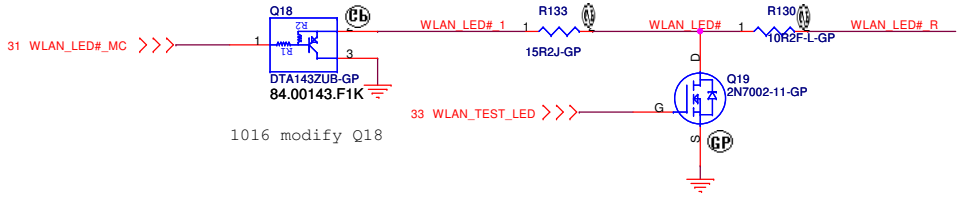
0910 delete RIGHT1 and LEFT1

0930 modify TPAD1 1124 modify TPAD1
1013 modify TPAD1
1015 modify TPAD1

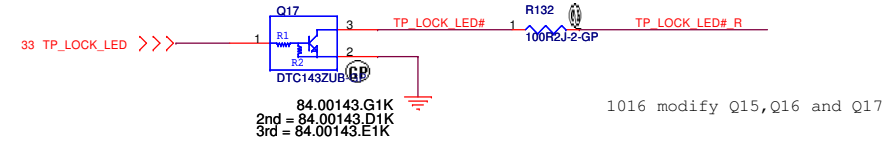
UMA Two Phase 2

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Touch pad		
Size	Document Number: HM40-MV	Rev: SB
Date: Monday, December 01, 2008	Sheet 35 of 51	

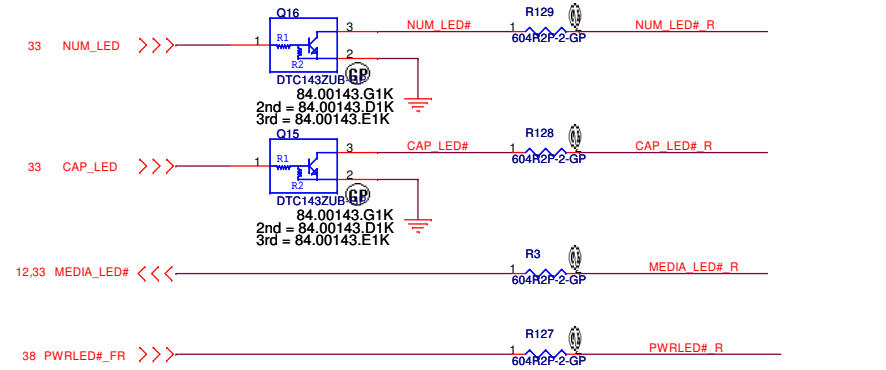
SB 1119 modify R130 and R133



1016 modify Q18

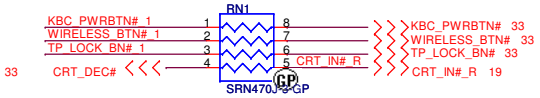


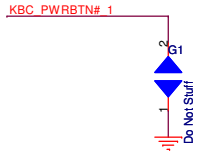
1016 modify Q15,Q16 and Q17



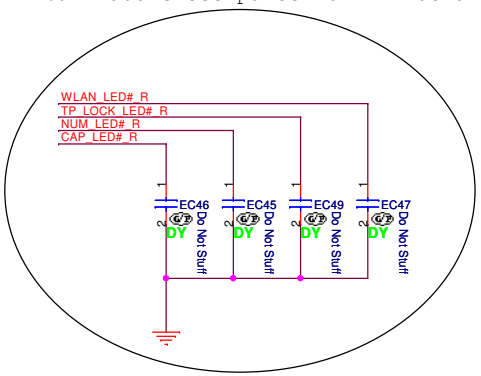
SB

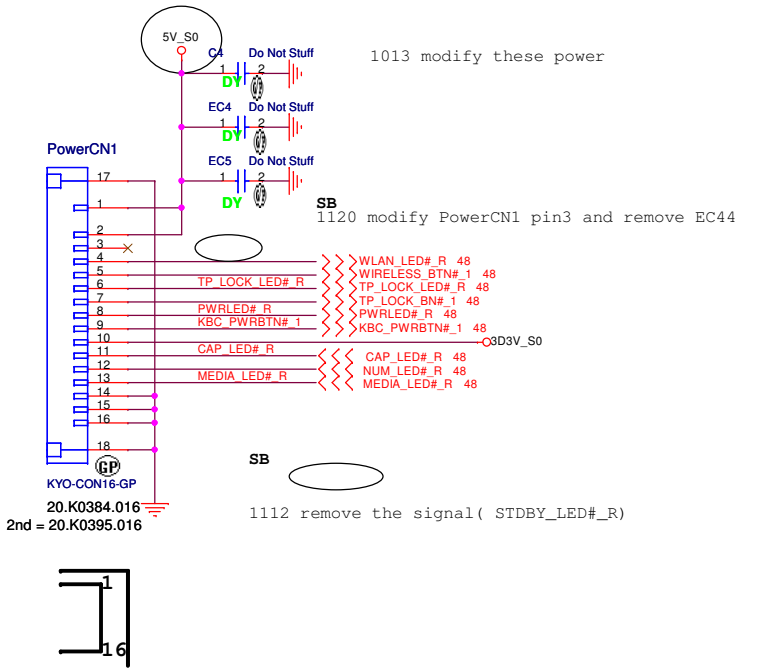
1112 remove these signals(STDBY_LED#_FR and STDBY_LED#_R) and R131





0912 add these parts for EMI demand





1013 modify these power

SB

1120 modify PowerCN1 pin3 and remove EC44

SB

1112 remove the signal(STDBY_LED#_R)

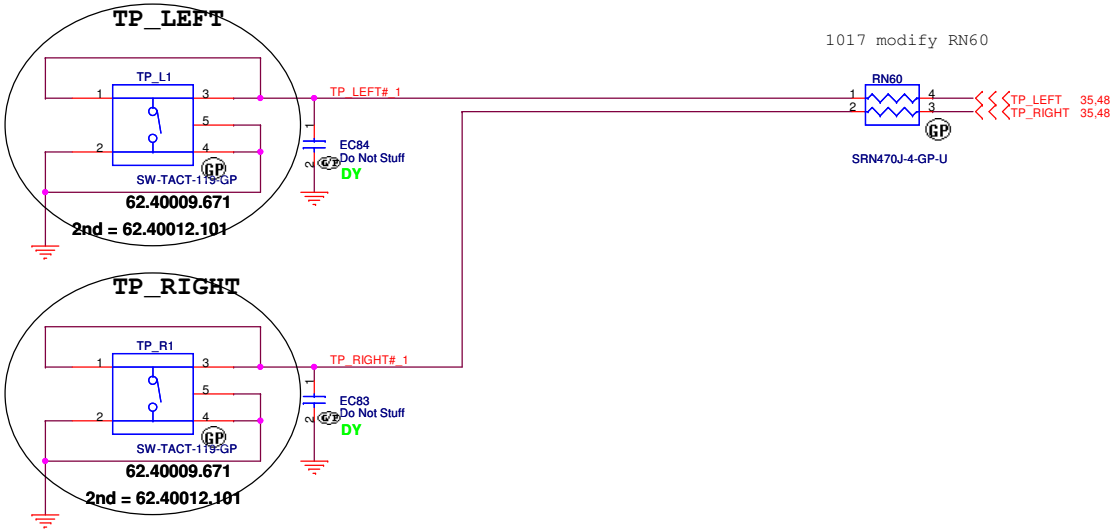
UMA Two Phase 2

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

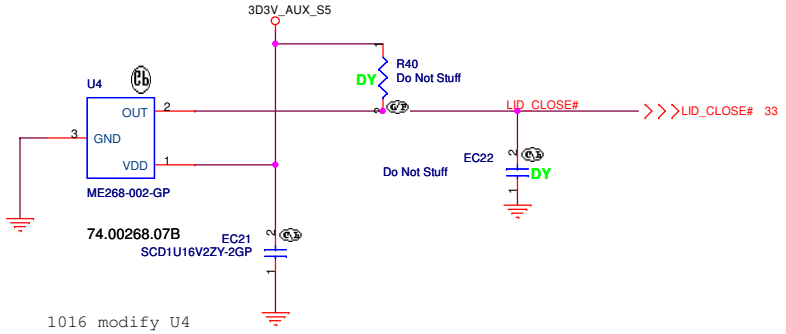
Title: Power Board

Size | Document Number: HM40-MV | Rev: SB

Date: Wednesday, November 26, 2008 | Sheet 36 of 51



Cover Up Switch



1016 modify U4
1017 modify U4

1017 add U61,R52,EC24 and EC23
1020 delete U61,R52,EC24 and EC23

UMA Two Phase 2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	**SWITCHS**	
Size	Document Number **HM40-MV**	Rev SB
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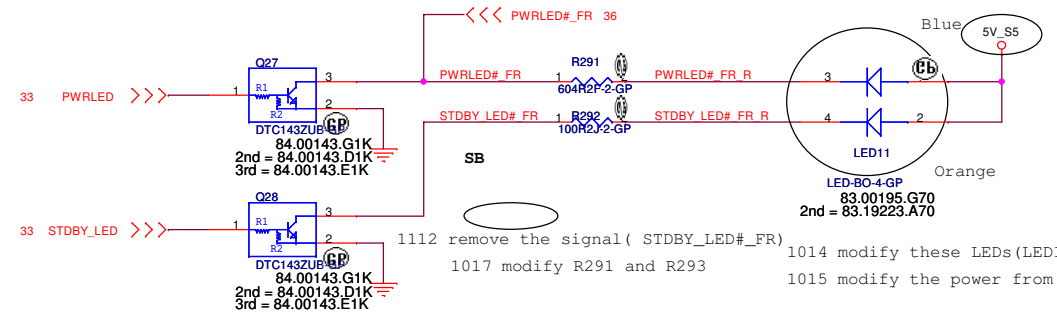
1015 modify the power from 3D3V_S5 to 5V_S5

SB 1106 modify LED11

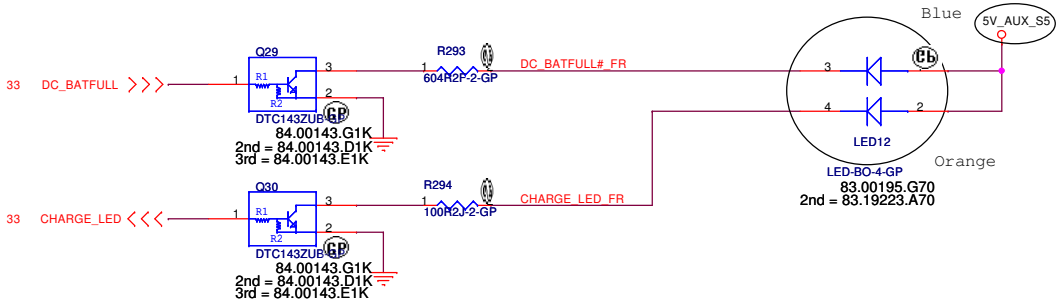


1112 remove the signal(STDBY_LED#_FR)

1017 modify R291 and R293

1014 modify these LEDs(LED11,LED12)

1015 modify the power from 3D3V_S5 to 5V_S5



SB 1106 modify LED12

1106 modify LED power from 5V_S5 to 5V_AUX_S5

1016 modify Q27~Q30

UMA Two Phase 2

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
LED		
Size	Document Number	Rev
	HM40-MV	SB
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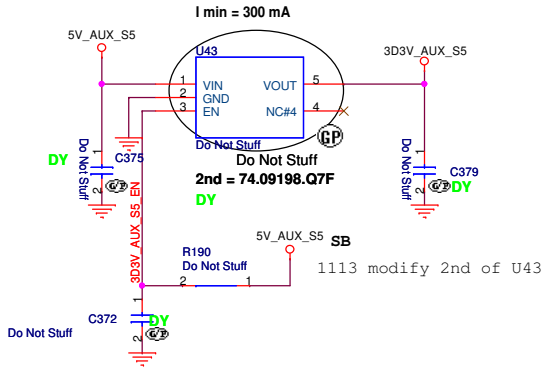
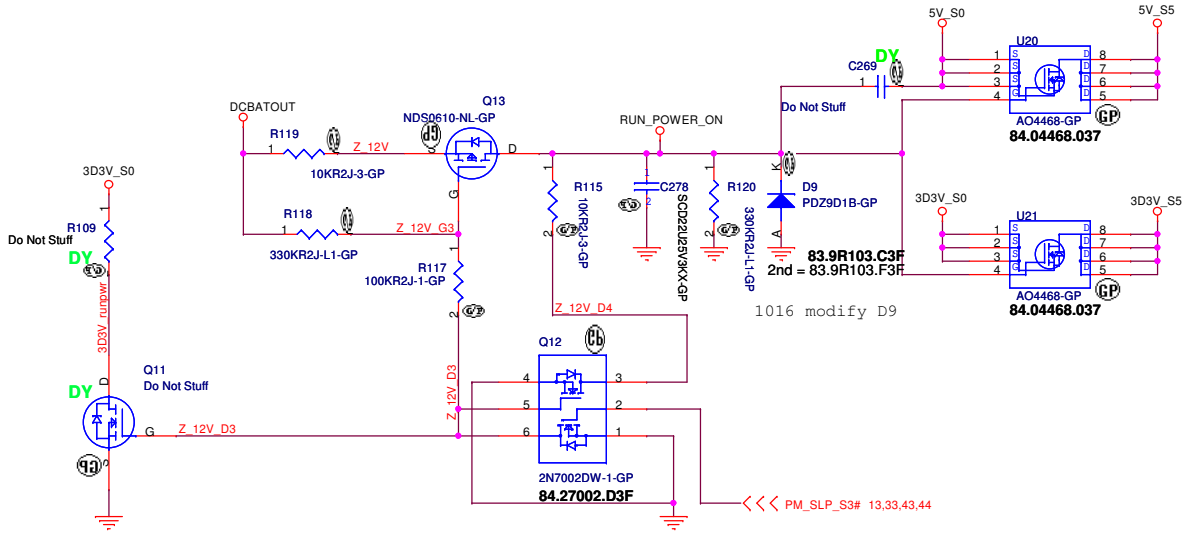
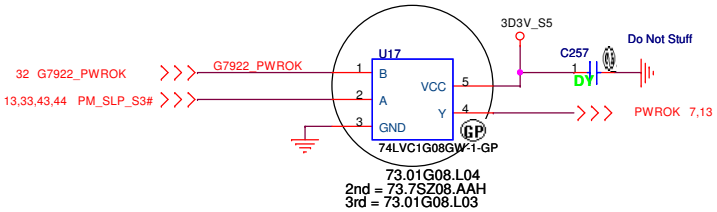
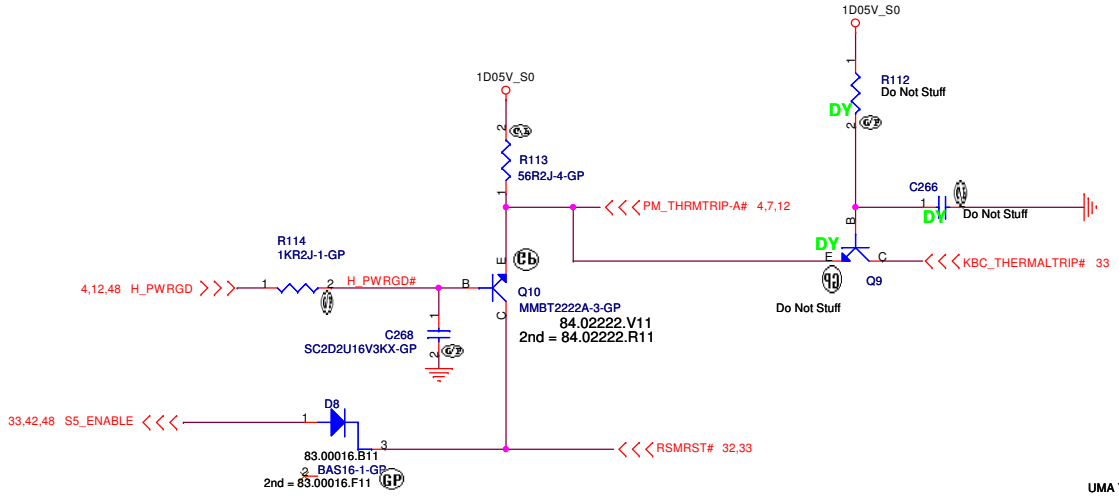
Aux Power 3D3V_AUX_S5



Run Power







UMA Two Phase 2

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RUN POWER and 3D3V_AUX_S5

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CPU_CORE
ISL6266A

VID0
VID1
VID2
VID3
VID4
VID5
VID6
CPUCORE_ON
VCC_SENSE
VSS_SENSE
DCBATOUT_6266A
5V_S0
3D3V_S0

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)
VID6(I / 3.3V)

Input Signal
EN (I / 3.3V)

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

Input Power
VCC(I)
VCC(I)
VCC(I)

Output Signal
PGOOD

Output Power
VCC_CORE_PWR(O)

VGATE_PWRGD
VCC_CORE(Imax=38A)

TPS51125
5V/3D3V

DCBATOUT_51125
S5_ENABLE
ALW_PWRGD_3V_5V

Input Power
VIN

Input Signal
EN0

Output Signal
PGOOD

Output Power
5V(O)
3D3V(O)
5V(O)
3D3V(O)

5V_S5 (6A)
3D3V_S5 (6A)
5V_AUX_S5
3D3V_AUX_S5

RT9018A
1D5V_S0

1D8V_S3
PM_SLP_S3#

VIN
EN
1D5V(O)
PGOOD

1D5V_S0 (2.5A)
CPUCORE_ON

RT9026
0D9V_S0

5V_S5
1D8V_S3
PM_SLP_S4#

VIN
VLDOIN
S3
S5
VTT
VTTREF

0D9V_S3 (1A)
0D9V_S3_1

TPS51124
1D8V/1D05V

5V_S5
DCBATOUT_51124
PM_SLP_S4#
PM_SLP_S3#
CPUCORE_ON

Input Power
VDD
VCC

Input Signal
EN1
EN2

Output Signal
PGOOD1
PGOOD2

Output Power
1D8V (O)
1D05V(O)

1D8V_S3 (10A)
1D05V_S0 (15A)

Adapter

AD_OFF
AD_JK
5V_AUX_S5

Input Signal
(I)

Input Power
VCC(I)
VCC(I)

Output Signal
(O)

Output Power
VCC(O)

AD_IN#
AD+

Charger BQ24745

CHG_ON#
24750_CELLS
AD+

Input Signal
CHGEN#
CELLS

Input Power
ACN

Output Signal
ACGOOD#
SRSET

Output Power
VOUT (O)
VOUT (O)

AC_IN#
AD_IA
BT+
DCBATOUT

UMA Two Phase 2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Sequence Logic**

Size	Document Number	Rev
B	HM40-MV	SB

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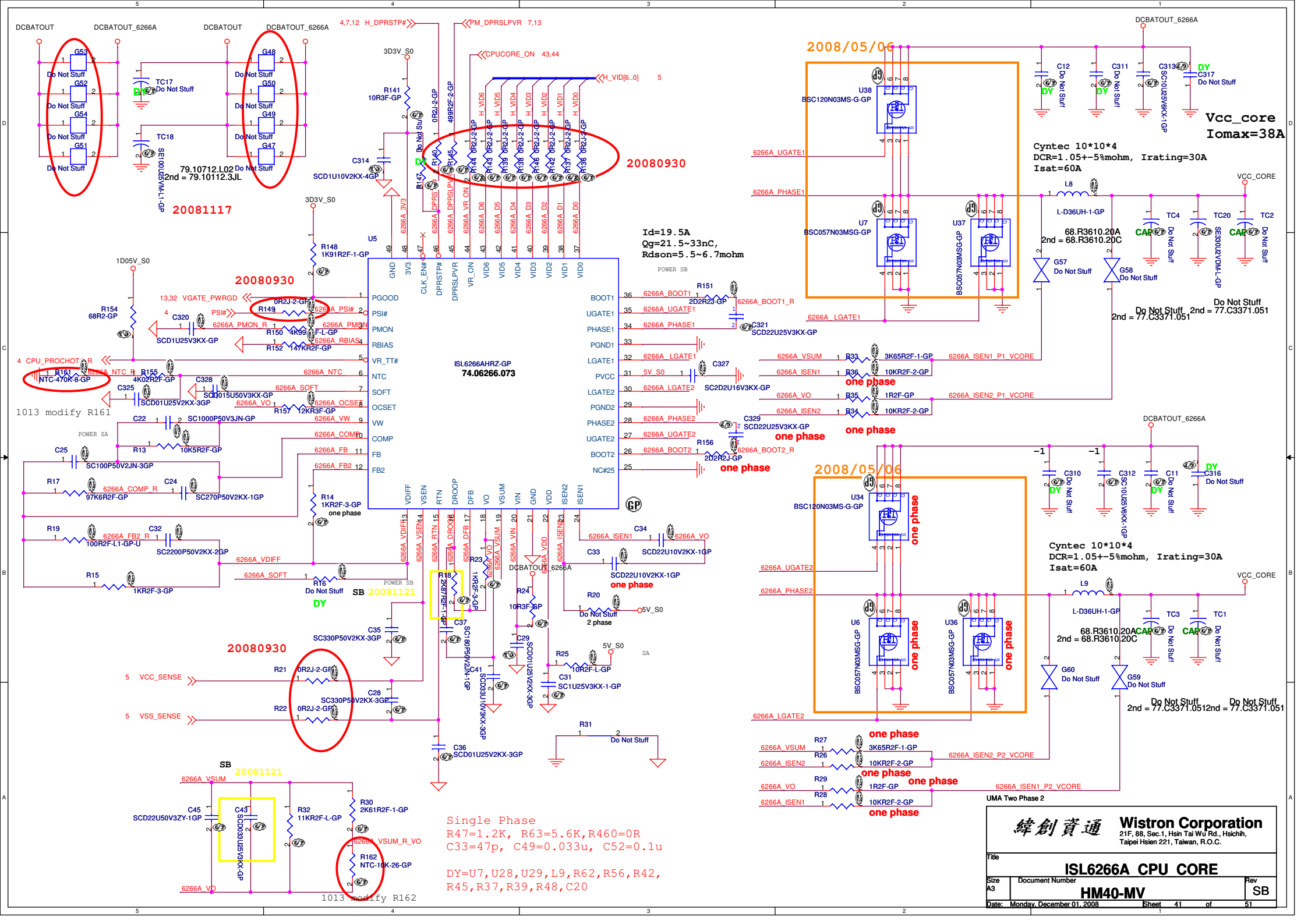
DCBATOUT
DCBATOUT_6266A
DCBATOUT
DCBATOUT_6266A
4,7,12 H_DPRSTP#
PM_DPRSLPVR 7,13
CPUCORE_ON 43,44
H_VID[6..0] 5
3D3V_S0
20080930
20081117
79.10712.L02
2nd = 79.10112.3JL
Id=19.5A
Qg=21.5~33nC,
Rdson=5.5~6.7mohm
ISL6266AHRZ-GP
74.06266.073
1013 modify R161
1013 modify R162
20081121
SB
DY
2008/05/06
Vcc_core
Iomax=38A
Cyntec 10*10*4
DCR=1.05+-5%mohm, Irating=30A
Isat=60A
68.R3610.20A
2nd = 68.R3610.20C
one phase
2 phase
Do Not Stuff
2nd = 77.C3371.051
UMA Two Phase 2
Single Phase
R47=1.2K, R63=5.6K,R460=0R
C33=47p, C49=0.033u, C52=0.1u
DY=U7,U28,U29,L9,R62,R56,R42,
R45,R37,R39,R48,C20
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL6266A_CPU_CORE
Size A3
Document Number HM40-MV
Rev SB
Date: Monday, December 01, 2008
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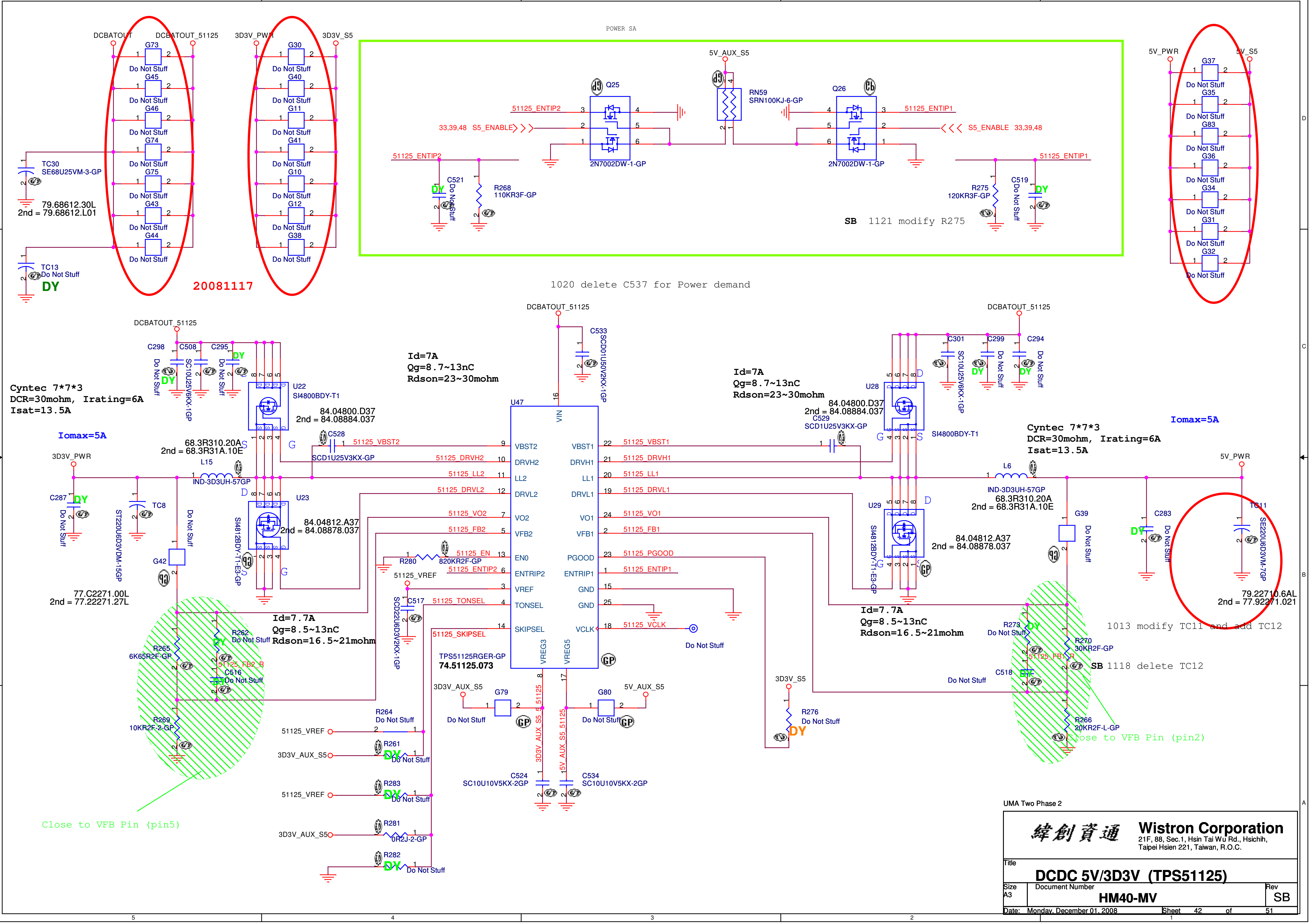

POWER SA
DCBATOUT
DCBATOUT_51125
3D3V_PWR
3D3V_S5
5V_PWR
5V_S5
5V_AUX_S5
Do Not Stuff
20081117
TC30 SE68U25VM-3-GP
79.68612.30L
2nd = 79.68612.L01
TC13 Do Not Stuff
DY
Q25 2N7002DW-1-GP
Q26 2N7002DW-1-GP
RN59 SRN100KJ-6-GP
51125_ENTIP2
51125_ENTIP1
33,39,48 S5_ENABLE
S5_ENABLE 33,39,48
R268 110KR3F-GP
R275 120KR3F-GP
C521
C519
SB 1121 modify R275
1020 delete C537 for Power demand
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
Iomax=5A
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
U22 SI4800BDY-T1
U28 SI4800BDY-T1
U23 SI4812BDY-T1-E3-GP
U29 SI4812BDY-T1-E3-GP
84.04800.D37
2nd = 84.08884.037
84.04812.A37
2nd = 84.08878.037
L15 IND-3D3UH-57GP
L6 IND-3D3UH-57GP
68.3R310.20A
2nd = 68.3R31A.10E
U47 TPS51125RGER-GP
74.51125.073
VIN VBST2 DRVH2 LL2 DRVL2 VO2 VFB2 EN0 ENTRIP2 VREF TONSEL SKIPSEL VREG3 VREG5
VBST1 DRVH1 LL1 DRVL1 VO1 VFB1 PGOOD ENTRIP1 GND VCLK
51125_VBST2 51125_DRVH2 51125_LL2 51125_DRVL2 51125_VO2 51125_FB2 51125_EN 51125_ENTIP2 51125_VREF 51125_TONSEL 51125_SKIPSEL
51125_VBST1 51125_DRVH1 51125_LL1 51125_DRVL1 51125_VO1 51125_FB1 51125_PGOOD 51125_ENTIP1 51125_VCLK
C533 SCD01U50V2KX-1GP
C528 SCD1U25V3KX-GP
C529 SCD1U25V3KX-GP
C298 C508 C295 SC10U25V6KX-1GP
C301 C299 C294 SC10U25V6KX-1GP
C287 TC8 ST220U6D3VDM-15GP
77.C2271.00L
2nd = 77.22271.27L
TC11 SE220U6D3VM-7GP
79.22710.6AL
2nd = 77.92271.021
1013 modify TC11 and add TC12
SB 1118 delete TC12
R280 820KR2F-GP
C517 SCD22U6D3V2KX-1GP
R265 6K65R2F-GP
R269 10KR2F-2-GP
R262 Do Not Stuff
C516 Do Not Stuff
51125_FB2_R
R270 30KR2F-GP
R266 20KR2F-L-GP
R273 Do Not Stuff
C518 Do Not Stuff
51125_FB1_R
R276 Do Not Stuff
G39 G42 G79 G80
3D3V_AUX_S5
C524 SC10U10V5KX-2GP
C534 SC10U10V5KX-2GP
R264 Do Not Stuff
R261 Do Not Stuff
R283 Do Not Stuff
R281 0R2J-2-GP
R282 Do Not Stuff
51125_VREF
Close to VFB Pin (pin5)
Close to VFB Pin (pin2)
UMA Two Phase 2
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
DCDC 5V/3D3V (TPS51125)
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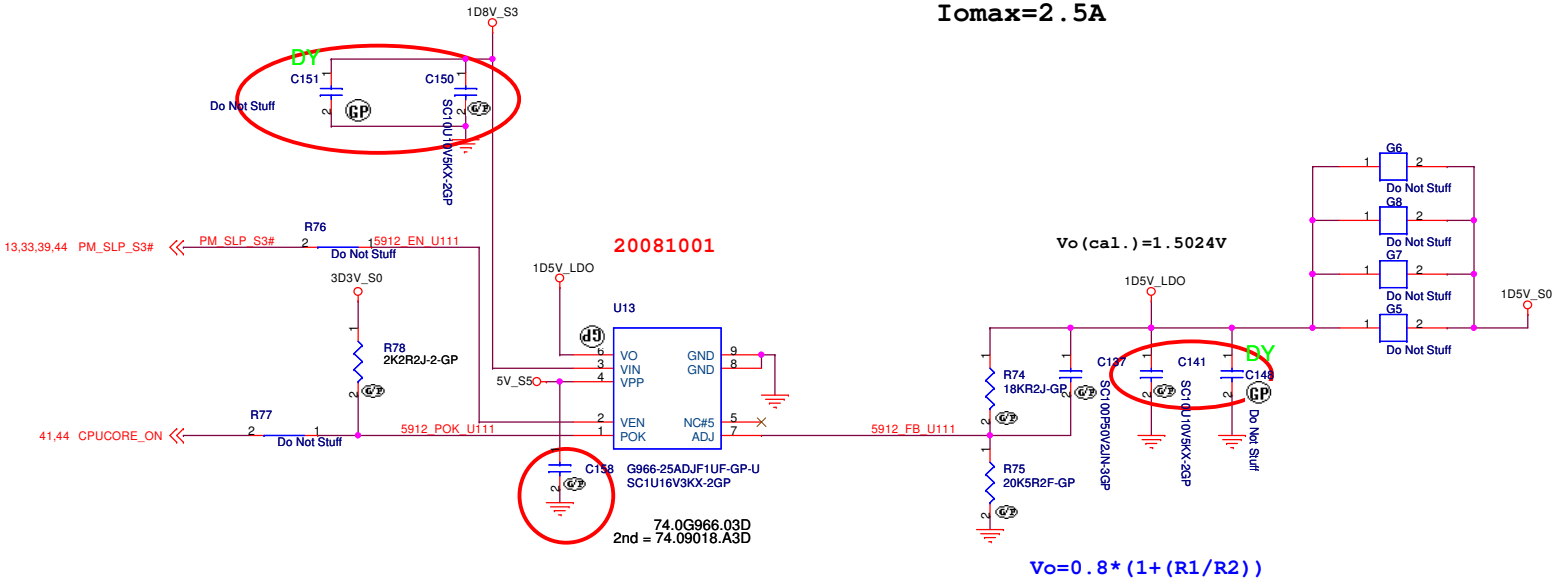
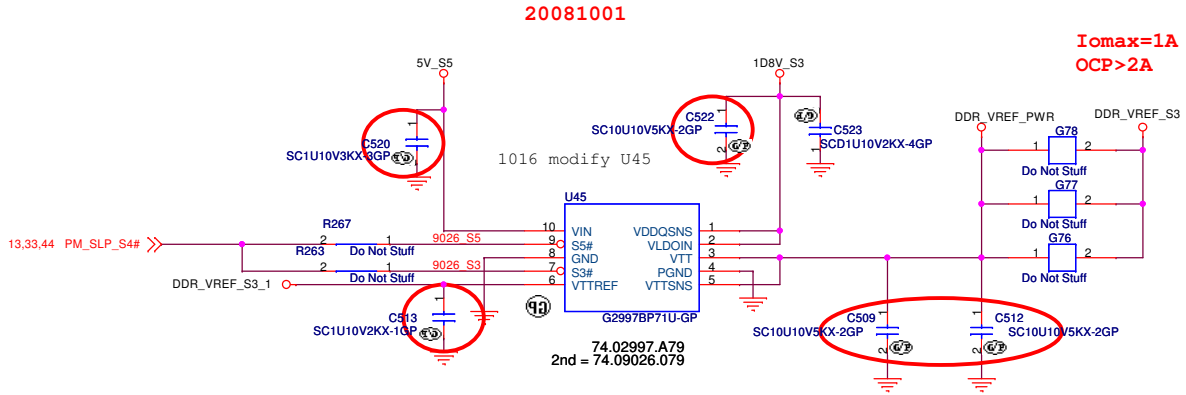
1D5V_S0
Iomax=2.5A





UMA Two Phase 2

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	1D5V & 0D9V	
Size A3	Document Number HM40-MV	Rev SB
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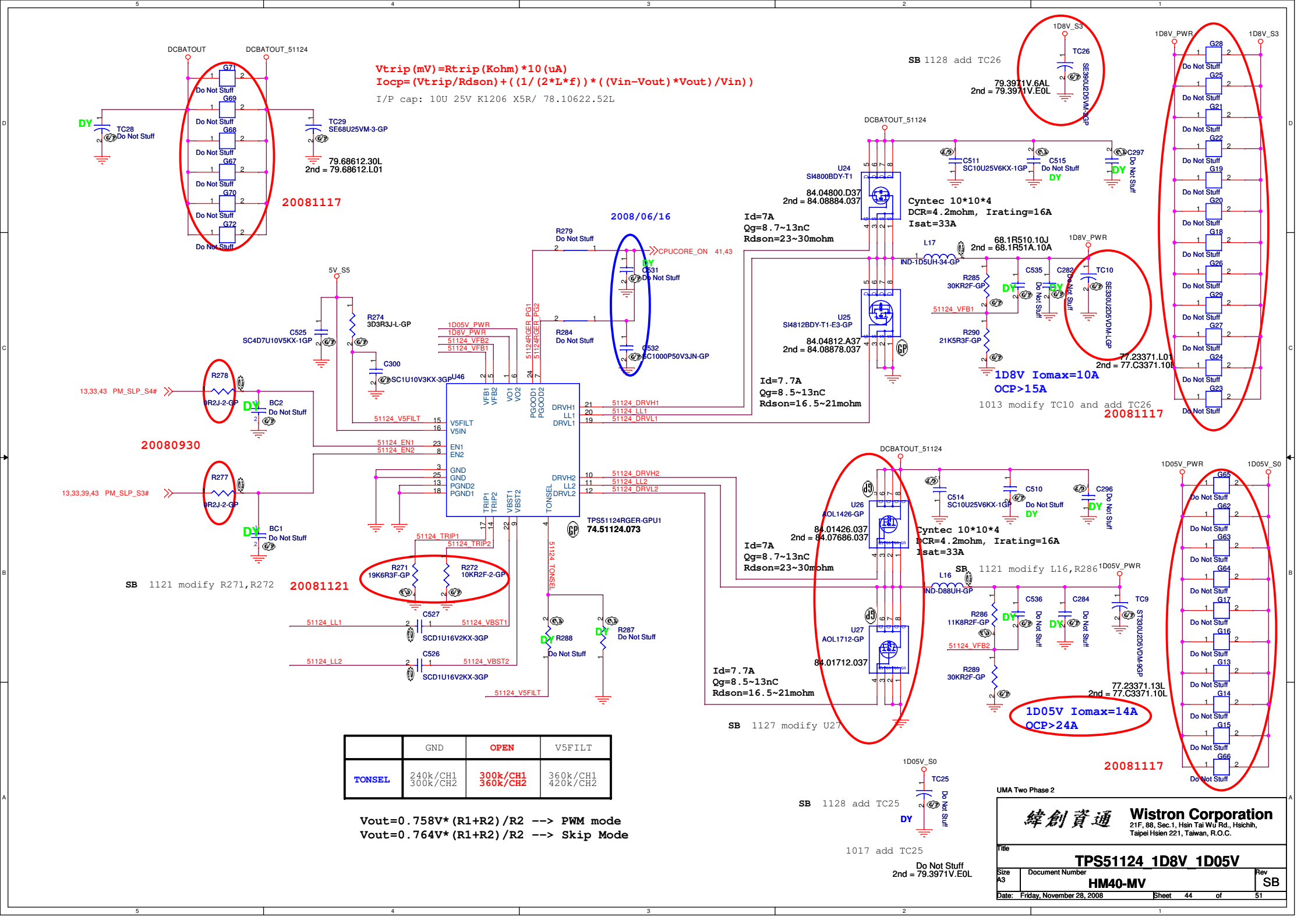
Vtrip(mV)=Rtrip(Kohm)*10(uA)
Iocp=(Vtrip/Rdson)+((1/(2*L*f))*((Vin-Vout)*Vout)/Vin))
I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
DCBATOUT
DCBATOUT_51124
G71 Do Not Stuff
G69 Do Not Stuff
G68 Do Not Stuff
G67 Do Not Stuff
G70 Do Not Stuff
G72 Do Not Stuff
DY TC28 Do Not Stuff
TC29 SE68U25VM-3-GP
79.68612.30L
2nd = 79.68612.L01
20081117
2008/06/16
R279 Do Not Stuff
R284 Do Not Stuff
CPUCORE_ON 41,43
DY C531 Do Not Stuff
C532 SC1000P50V3JN-GP
5V_S5
R274 3D3R3J-L-GP
C525 SC4D7U10V5KX-1GP
C300 SC1U10V3KX-3GP
1D05V_PWR
1D8V_PWR
51124_VFB2
51124_VFB1
5124RGER_PG1
5124RGER_PG2
U46
R278 0R2J-2-GP
13,33,43 PM_SLP_S4#
DY BC2 Do Not Stuff
20080930
R277 0R2J-2-GP
13,33,39,43 PM_SLP_S3#
DY BC1 Do Not Stuff
SB 1121 modify R271,R272
20081121
51124_V5FILT
51124_EN1
51124_EN2
VFB1 VFB2 VO1 VO2 PGOOD1 PGOOD2
V5FILT V5IN EN1 EN2 GND GND PGND2 PGND1
DRVH1 LL1 DRVL1 DRVH2 LL2 DRVL2 TONSEL
TRIP1 TRIP2 VBST1 VBST2
TPS51124RGER-GPU1
74.51124.073
51124_DRVH1
51124_LL1
51124_DRVL1
51124_DRVH2
51124_LL2
51124_DRVL2
51124_TRIP1
51124_TRIP2
R271 19K6R3F-GP
R272 10KR2F-2-GP
C527 SCD1U16V2KX-3GP
C526 SCD1U16V2KX-3GP
51124_VBST1
51124_VBST2
R288 Do Not Stuff
DY R287 Do Not Stuff
51124_TONSEL
51124_V5FILT
DCBATOUT_51124
U24 SI4800BDY-T1
84.04800.D37
2nd = 84.08884.037
U25 SI4812BDY-T1-E3-GP
84.04812.A37
2nd = 84.08878.037
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
C511 SC10U25V6KX-1GP
C515 Do Not Stuff
DY
C297 Do Not Stuff
DY
Cyntec 10*10*4
DCR=4.2mohm, Irating=16A
Isat=33A
L17 IND-1D5UH-34-GP
68.1R510.10J
2nd = 68.1R51A.10A
R285 30KR2F-GP
C535 Do Not Stuff
DY
C282 Do Not Stuff
DY
TC10 SE330U2D5VDM-L-GP
R290 21K5R3F-GP
77.23371.L01
2nd = 77.C3371.10L
1D8V Iomax=10A
OCP>15A
1013 modify TC10 and add TC26
20081117
SB 1128 add TC26
1D8V_S3
TC26 SE330U2D5VM-3-GP
79.3971V.6AL
2nd = 79.3971V.E0L
1D8V_PWR
1D8V_S3
G28 Do Not Stuff
G25 Do Not Stuff
G21 Do Not Stuff
G22 Do Not Stuff
G19 Do Not Stuff
G20 Do Not Stuff
G18 Do Not Stuff
G26 Do Not Stuff
G29 Do Not Stuff
G27 Do Not Stuff
G24 Do Not Stuff
G23 Do Not Stuff
DCBATOUT_51124
U26 AOL1426-GP
84.01426.037
2nd = 84.07686.037
U27 AOL1712-GP
84.01712.037
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
C514 SC10U25V6KX-1GP
C510 Do Not Stuff
DY
C296 Do Not Stuff
DY
Cyntec 10*10*4
DCR=4.2mohm, Irating=16A
Isat=33A
SB 1121 modify L16,R286
L16 IND-D88UH-GP
1D05V_PWR
R286 11K8R2F-GP
C536 Do Not Stuff
DY
C284 Do Not Stuff
DY
TC9 ST330U2D5VDM-9GP
R289 30KR2F-GP
77.23371.13L
2nd = 77.C3371.10L
1D05V Iomax=14A
OCP>24A
SB 1127 modify U27
1D05V_PWR
1D05V_S0
G65 Do Not Stuff
G62 Do Not Stuff
G63 Do Not Stuff
G64 Do Not Stuff
G17 Do Not Stuff
G16 Do Not Stuff
G13 Do Not Stuff
G14 Do Not Stuff
G15 Do Not Stuff
G66 Do Not Stuff
20081117
1D05V_S0
TC25 Do Not Stuff
DY
SB 1128 add TC25
1017 add TC25
Do Not Stuff
2nd = 79.3971V.E0L
GND OPEN V5FILT
TONSEL 240k/CH1 300k/CH2 300k/CH1 360k/CH2 360k/CH2 420k/CH2
Vout=0.758V*(R1+R2)/R2 --> PWM mode
Vout=0.764V*(R1+R2)/R2 --> Skip Mode
UMA Two Phase 2
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
TPS51124_1D8V_1D05V
Size A3
Document Number
HM40-MV
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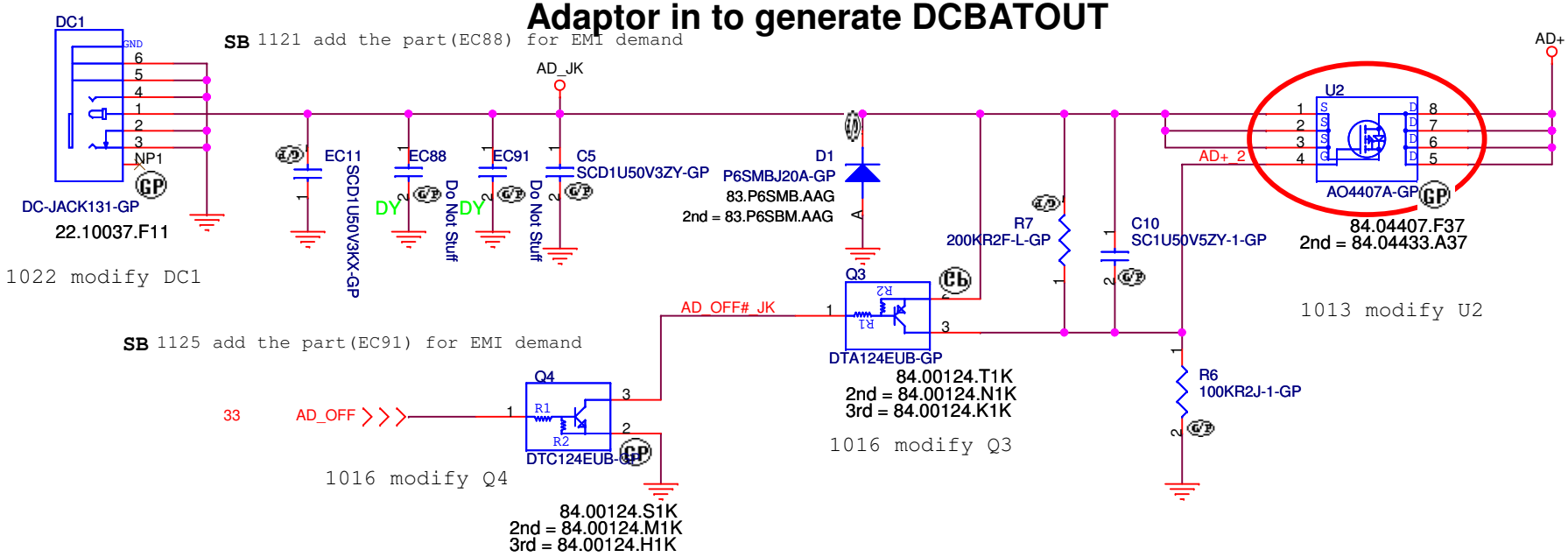
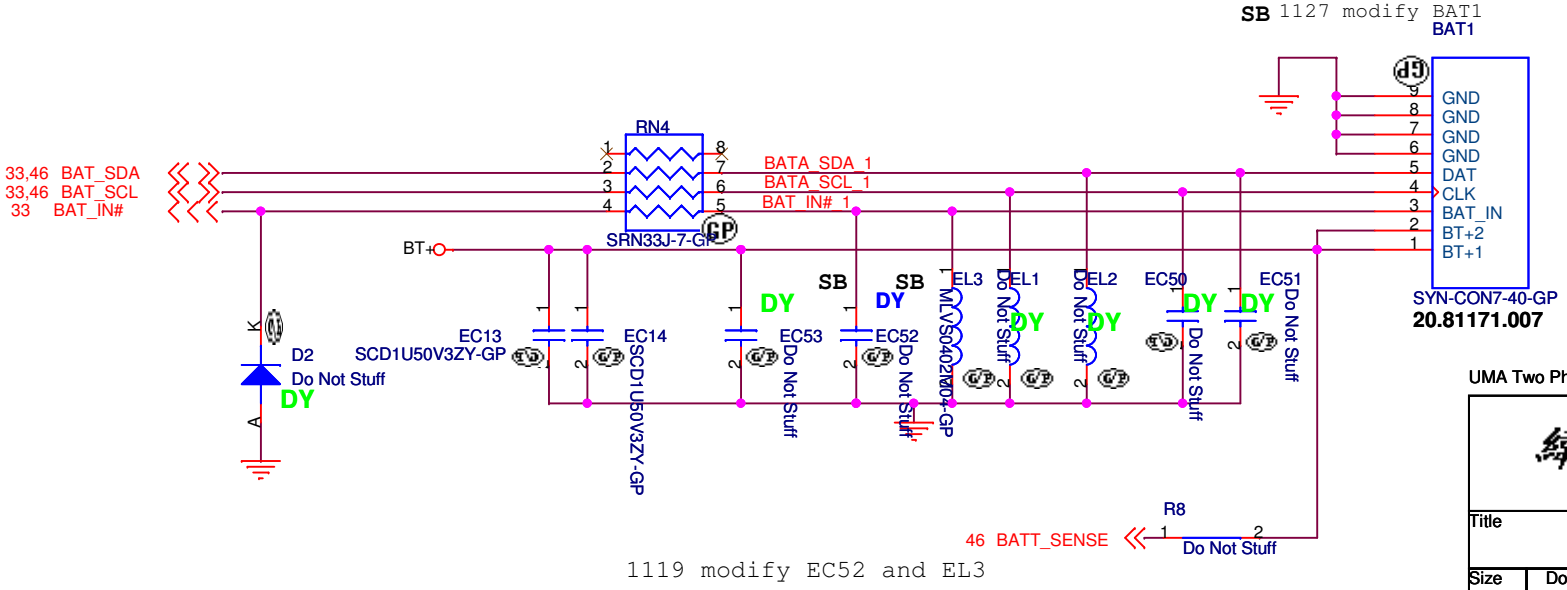
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



UMA Two Phase 2

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**AD/BATT CONN**	
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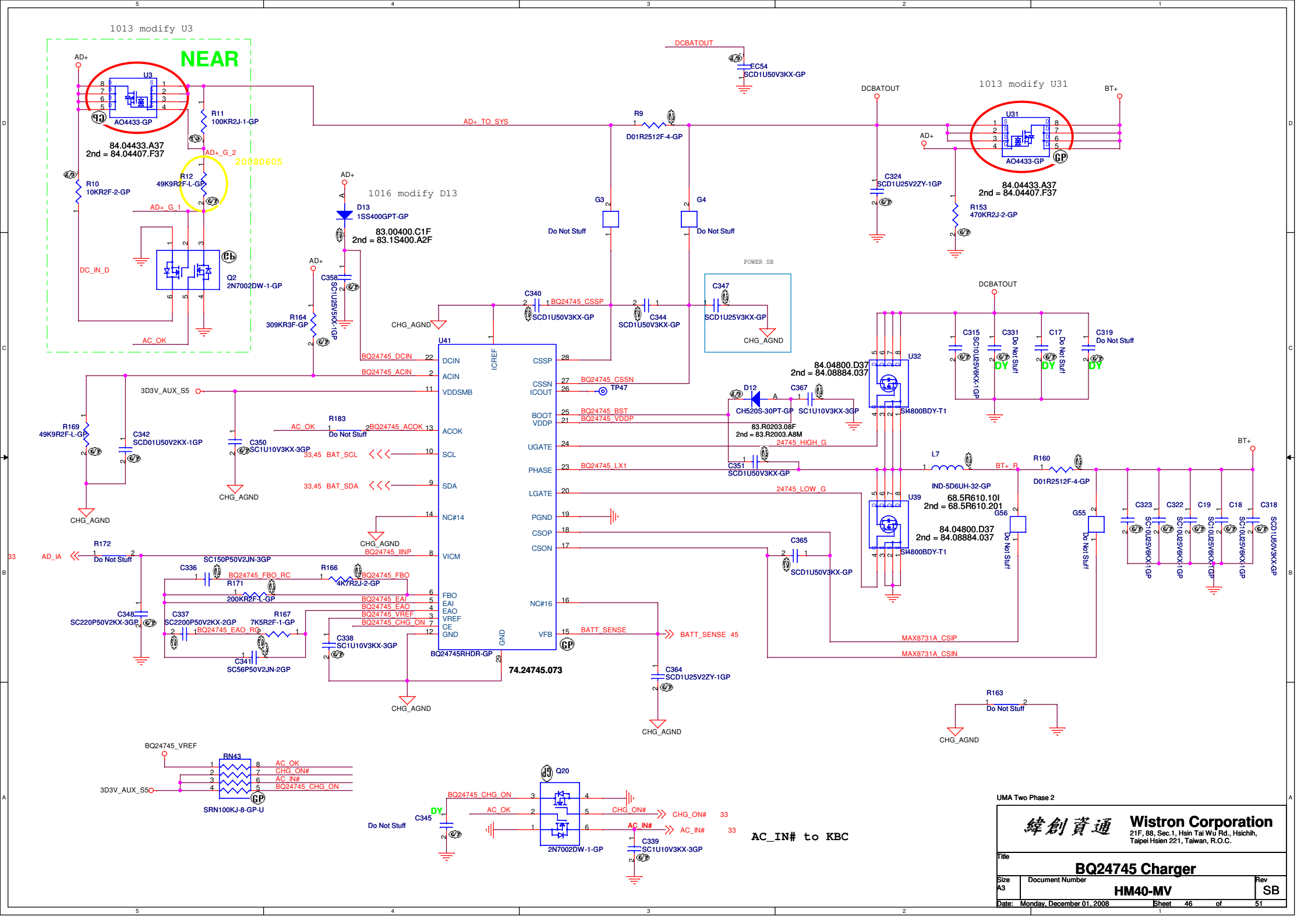
1013 modify U3
NEAR
AD+
U3
AO4433-GP
84.04433.A37
2nd = 84.04407.F37
R11
100KR2J-1-GP
AD+_G_2
20080605
R10
10KR2F-2-GP
R12
49K9R2F-L-GP
AD+_G_1
DC_IN_D
Q2
2N7002DW-1-GP
AC_OK
AD+
D13
1SS400GPT-GP
83.00400.C1F
2nd = 83.1S400.A2F
1016 modify D13
C358
SC1U25V3KX-1GP
R164
309KR3F-GP
CHG_AGND
DCBATOUT
EC54
SCD1U50V3KX-GP
AD+_TO_SYS
R9
D01R2512F-4-GP
G3
G4
Do Not Stuff
C340
BQ24745_CSSP
SCD1U50V3KX-GP
C344
SCD1U50V3KX-GP
POWER SB
C347
SCD1U25V3KX-GP
1013 modify U31
U31
AO4433-GP
84.04433.A37
2nd = 84.04407.F37
C324
SCD1U25V2ZY-1GP
R153
470KR2J-2-GP
BT+
U41
BQ24745RHDR-GP
74.24745.073
ICREF
GND
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
VICM
FBO
EAI
EAO
VREF
CE
GND
CSSP
CSSN
ICOUT
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
BQ24745_DCIN
BQ24745_ACIN
BQ24745_CSSN
TP47
BQ24745_BST
BQ24745_VDDP
24745_HIGH_G
BQ24745_LX1
24745_LOW_G
BQ24745_IINP
BQ24745_FBO_RC
BQ24745_FBO
BQ24745_EAI
BQ24745_EAO
BQ24745_VREF
BQ24745_CHG_ON
BQ24745_EAO_RC
BATT_SENSE
BATT_SENSE 45
MAX8731A_CSIP
MAX8731A_CSIN
3D3V_AUX_S5
AC_OK
R183
Do Not Stuff
BQ24745_ACOK
33,45 BAT_SCL
33,45 BAT_SDA
R169
49K9R2F-L-GP
C342
SCD01U50V2KX-1GP
C350
SC1U10V3KX-3GP
R172
Do Not Stuff
SC150P50V2JN-3GP
AD_IA
C336
R171
200KR2F-1-GP
R166
4K7R2J-2-GP
C348
SC220P50V2KX-3GP
C337
SC2200P50V2KX-2GP
R167
7K5R2F-1-GP
C341
SC56P50V2JN-2GP
C338
SC1U10V3KX-3GP
C364
SCD1U25V2ZY-1GP
C365
SCD1U50V3KX-GP
D12
CH520S-30PT-GP
C367
SC1U10V3KX-3GP
C351
SCD1U50V3KX-GP
83.R0203.08F
2nd = 83.R2003.A8M
U32
SI4800BDY-T1
U39
SI4800BDY-T1
84.04800.D37
2nd = 84.08884.037
68.5R610.10I
2nd = 68.5R610.201
L7
IND-5D6UH-32-GP
BT+_R
R160
D01R2512F-4-GP
C315
C331
C17
C319
Do Not Stuff
DY
C323
C322
C19
C18
C318
SCD1U50V3KX-GP
G55
G56
R163
Do Not Stuff
BQ24745_VREF
RN43
SRN100KJ-8-GP-U
AC_OK
CHG_ON#
AC_IN#
BQ24745_CHG_ON
Q20
2N7002DW-1-GP
C345
C339
SC1U10V3KX-3GP
CHG_ON#
AC_IN#
33
AC_IN# to KBC
UMA Two Phase 2
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BQ24745 Charger
Size
A3
Document Number
HM40-MV
Rev
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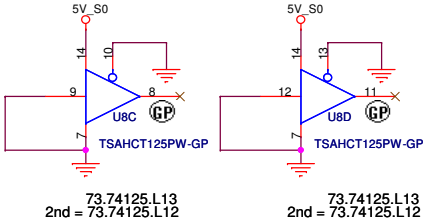
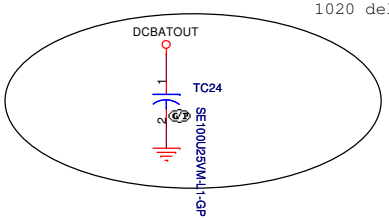


73.74125.L13
2nd = 73.74125.L12

73.74125.L13
2nd = 73.74125.L12

1020 delete TC14,TC15



SB

1117 delete TC19

79.10712.L02
2nd = 79.10112.3JL

1016 modify U32

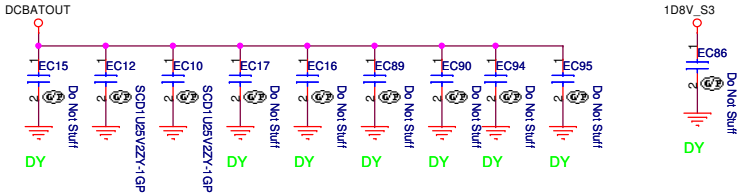
1017 add these parts(EC10,EC12,EC15~EC17,EC86) for EMI demand

1020 add the part(EC86) for EMI demand

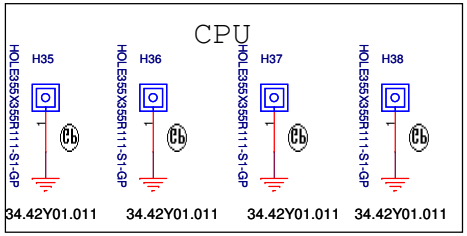
1125 add the part(EC90) for EMI demand

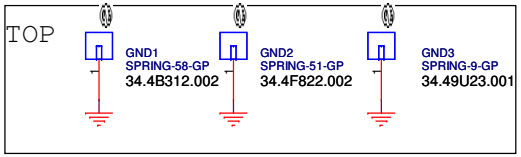
SB 1121 add the part(EC89) for EMI demand

1128 EC94,EC95 for EMI demand



1016 add GND1 and GND2 for EMI demand
1017 add GND3 and modify GND2 for EMI demand



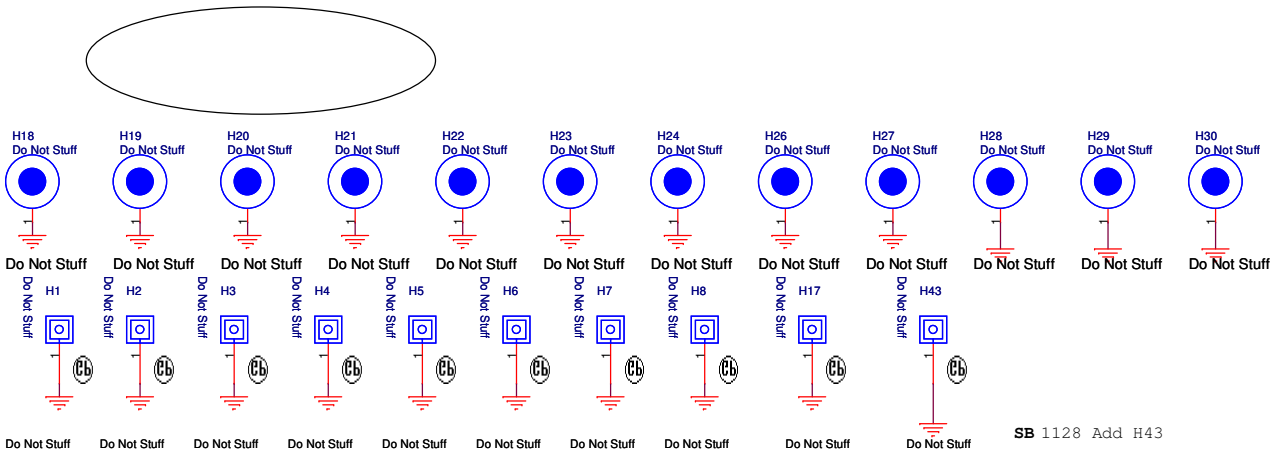


SB 1128 Add GND4,GND7,GND8

1016 modify H35~H38
1016 delete H9~H12

1016 modify H31 and H32

SB 1120 remove H31and H32



SB 1128 Add H43

UMA Two Phase 2

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: EMI/Spring/Boss

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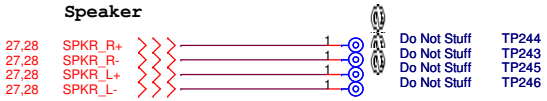
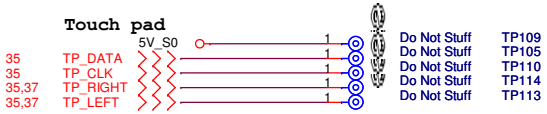
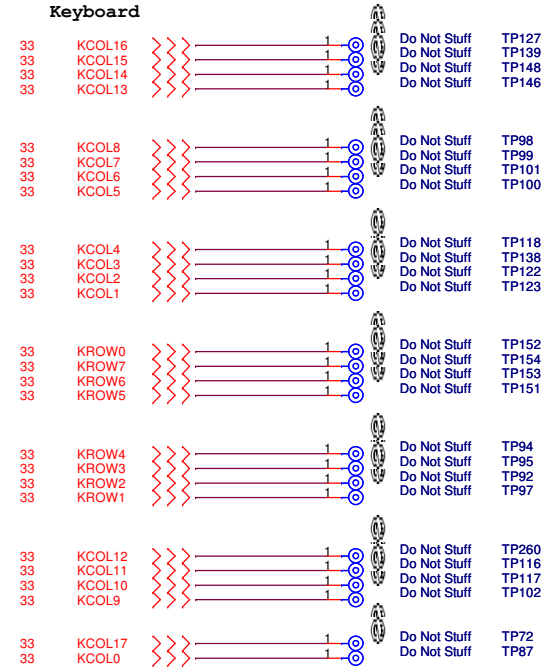
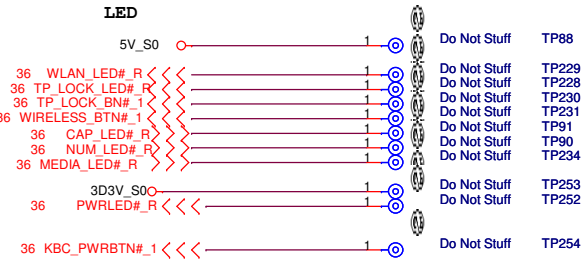




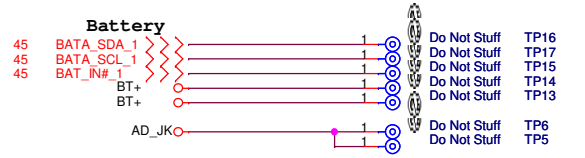


1017 modify USB signal connection

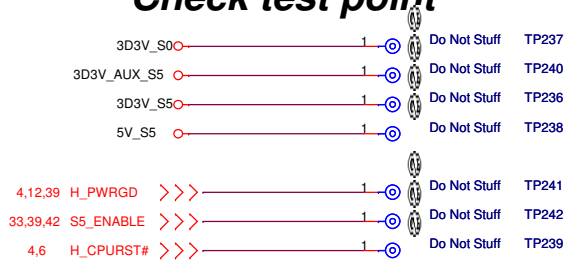


SB

1112 remove the signal(STDBY_LED#_R)



Check test point



Test Point放在Dimm Door打開可量測處

UMA Two Phase 2

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AFTE test point**

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0910 delete F4(Page 18)
0910 update footprint of U15(Page 30)
0910 delete RIGHT1 and LEFT1(Page 33)
0910 modify net names of TP_LEFT and TP_RIGHT(Page 36)
0910 modify test points of AFTE and TPAD
0911 modify net name from LPC_RST to PLT_RST1#(Page 24)
0911 add net name(RBIAS,LED_DUPLEX#,SMDATA,SMCLK)(Page 24)
0911 add net name(DVDD_1_8,ACZ_SDATAIN0_R,FLY_P,FLY_N,VREF_LO,VREF_HI)(Page 26)
0911 add net name(EAPD#_R)(Page 27)
0912 modify the schematic of Page 33
0912 delete GMCH_TXB*(Page 7& 18)
0912 add these parts for EMI demand(page 7,18,20,21,23,26,28,29,30,32,33,34,35)
0915 modify net name from 10M/100M/1G_LED# to 10M/100M_LED#(page24,25)
0915 delete these parts for EMI demand(page 30)
0915 add EC34 for EMI demand(page3)
0915 add EC73 for EMI demand(page 12)
0915 modify LEDs port
0916 move net(SPI_WP#) from U9 pin120 to pin25(page33)
0930 modify BLUE1(page22)
0930 add 2nd for SPK1, MIC1 and modify LOUT1 (page28)
0930 modify FAN1(page32)
0930 modify TPAD1(page35)
0930 modify KB1(page33)
0930 modify net name for BIOS demand(page33)
1001 delete these parts for EMI demand(ED1~8)
1009 modify net name for GND to AGND(page27)
1009 add R4,R5 for AC decopling(page27)
1009 add R96(page30)
1013 modify TPAD1(page35)
1013 modify U40 from 72.25X16.001 to 72.25X16.A01(page 34)
1013 modify TC11 and add TC12(page42)
1013 modify TC10 and add TC26(page44)
1013 modify U2(page45)
1013 modify U3 and U31(page 46)
1013 modify R161 and R162(page41)
1013 modify card1(page 30)
1014 modify these LEDs(LED11,LED12)(page38)
1014 modify these nets(page 26)
1014 modify R258 from 10k to 20k ohm(page26)
1014 add ER5 for EMI deamnd(page3)
1015 modify LCD1 pin define(page 18)
1015 modify the power from 3D3V_S5 to 5V_S5(page38)
1015 modify TPAD1(page35)
1015 modify RN57(page28)
1015 modify F1(page18)

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1016 modify L1,L2 and L3(page 19)
1016 modify XF1(page 25)
1016 modify RN53 and U10(page 24)
1016 modify U8(page19,47)
1016 modify U4(page 37)
1016 modify U23(page 43)
1016 modify X2(page12)
1016 modify X1(page 33)
1016 modify X3(page 3)
1016 modify D13(page 46)
1016 modify D23(page 20)
1016 modify D9(page 39)
1016 modify D4(page 19)
1016 modify Q3 and Q4(page45)
1016 modify Q18(page 36)
1016 modify Q15~Q17(page 36)
1016 modify Q27~Q30(page38)
1016 modify Q6 and Q14(page 32)
1016 modify Q8(PAGE 24)
1016 add GND1 nad GND2 for EMI demand(page 47)
1016 modify LCD1 pin define(page 18)
1016 delete H9~H12 and modify H35~H38,H31,H32(page 47)
1017 add these parts for EMI demand(page 47)
1017 delete these parts(EC208~EC210)(page 7)
1017 modify BLUE1(page 22)
1017 modify FAN1(page 32)
1017 modify R291 and R293(page 38)
1017 add U61,R52,EC23 and EC24(page 37)
1017 modify RN60(page37)
1017 add TC25(page 44)
1017 add GND3 and modify GND2 for EMI demand(page 47)
1017 modify USB signal connection(page13,18,22,23,30,31,48)
1020 delete C537 for Power demand(page42)
1020 add the part(EC86) for EMI demand(page 47)
1020 delete U61,R52,EC24 and EC23(page 37)
1020 delete TC14,TC15(page 47)
1021 modify TC16(page 31)
1021 delete TC23(page 23)
1021 modify TC5(page 20)
1021 modify and swap these parts(USB1 and USB2)(page 23)
1021 modify SATA1(page 20)
1022 modify DC1(page 45)

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1106 modify net connection of RN46 and RN44(page33) for layout demand
1106 modify LED11 and LED12(page38) for fixing issue
1106 modify LED power from 5V_S5 to 5V_AUX_S5(page38) for customer demand
1112 remove the signal(STDBY_LED#_FR)page38 for customer demand
1112 remove these signals(STDBY_LED#_FR and STDBY_LED#_R) and R131(page36) for customer demand
1112 remove the signal(STDBY_LED#_R)page36 for customer demand
1112 remove the signal(STDBY_LED#_R)and TP253(page48) for customer demand
1113 modify C103 and C106(page24) for crystal issue
1113 modify 2nd of U19(page26)
1113 modify 2nd of U43(page39)
1113 modify 2nd of U44(page10)
1113 modify U48(page22)
1117 delete MDC function(R231,R237,R232,R234)(page12)
1117 delete TC19(page 47) for ME deamnd
1118 modify PCB Ver. from SA to SB(page33)
1118 delete TC12(page42) for layout demand
1118 delete TC27(page9) for layout demand
1118 delete R107 and add L18 for cost down
1119 modify R130 and R133(page 36) for LED brightness
1119 modify EC52 and EL3(page45) for EMI demand
1119 modify SPK1(page 28) for ME deamnd
1119 add G84 for RTC reset demand
1120 modify EC78for EMI demand((page10)
1120 modify PowerCN1 pin3 and remove EC44(page36) fro LED function
1120 remove H31 and H32(page47)for ME demand
1120 add RN61 and RN62(page3) for layout demand
1120 swap these nets(CLK_MCH_3GPLL,CLK_MCH_3GPLL#, CLK_PCIE_MINI1,CLK_PCIE_MINI1#)(page3)for CLK REQ demand
1120 add the net(SATACLKREQ#)(page3,13)for CLK REQ demand
1120 move these nets (CLK_PCIE_MINI1,CLK_PCIE_MINI1#)(page3)for CLK REQ demand
1120 modify RN61 and RN62(page3)for CLK REQ demand
1121 add EC87 for EMI demand(page18)
1121 add the part(EC89) for EMI demand(page47)
1121 add the part(EC88) for EMI demand(page45)
1121 modify R18,C43(page41) for Power demand
1121 modify R275(page42)for Power demand
1121 modify R271,R272,R286 and L16(page44) for Power demand
1124 modify U42 and delete R182,R185 (page32) for thermal function
1124 modify these names of these nets(G7922_SGND2,G7922_SGND3...) (page32) for thermal function
1124 add R302(page3) for clock gen function
1125 add the part(EC90) for EMI demand(page47)
1125 add the part(EC91) for EMI demand(page45)
1125 modify R125,R126(page18) for LCD brightness control
1125 modify RN40 and delete RN42(page32) for layout demand
1125 add EC92 and EC93 for EMI demand(page 22)
1126 add these nets (PCIE_REQ_LAN#,PCIE_REQ_MINI#)(page3)for CLK REQ demand
1126 delete R230,R233,R235,R236 and RN63(page12) for removing MDC function
1126 add C541 and modify R101(page26) for codec function
1126 modify RN61 and RN62(page3) for layout demand
1126 modify EU1,EU2 and add EU3,EU4 for EMI demand(page28)
1127 modify CRT1(page19) for customer demand
1127 swap the nets of RN61 and RN62 for layout demand(page3)
1127 modify BAT1(page45) for ME demand
1127 modify U27(page44) for power demand
1127 modify C377(page32) for thermal function
1128 Add H43,GND4,GND7,GND8(page47) for EMI demand
1128 modify LCD1(page18) for cost down
1128 Add L19(page24) for vender demand
1128 add EC94,EC95 for EMI demand(page47)

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